1GB – 128Mx72 DDR2 SDRAM FBDIMM, ECC

FEATURES

■ 240-pin DDR2 fully buffered, dual in-line memory module (FBDIMM) with ECC to detect and report channel errors to the host memory controller.

■ Fast DDR2 DRAM data transfer rates: PC2-6400*, PC2-5300, and PC2-4300

■ 3.2 Gb/s and 4.0 Gb link transfer rates

■ High speed differential point-to-point link between host memory controller and the AMB using serial, dual-simplex bit lanes

- 10-pair southbound (data path to FBDIMM)
- 14-pair northbound (data path to FBDIMM)

■ Fault tolerant; can work around a bad bit lane in each direction

■ High density scaling with up to 8 dual-rank modules (288 DDR2 SDRAM devices) per channel

■ SMBus interface to AMB for configuration register access.

■ In-band and out-bank command access

■ Deterministic protocol

- Enables memory controller to optimize DRAM access for maximum performance
- Delivers precise control and repeatable memory behavior

■ Automatic DDR2 SDRAM bus and channel calibration

■ Transmitter de-emphasis to reduce ISI

■ MBIST and IBIST test functions

■ Transparent mode for DDR2 SDRAM test support

■ $V_{CC} = V_{CCQ} = +1.8V$ for DDR2 SDRAM

■ $V_{REF} = 0.9V$ SDRAM C/A termination

■ $V_{CC} = 1.5V$ for advanced memory buffer (AMB)

■ Serial Presence Detect (SPD) with EEPROM

■ Gold edge contacts

■ Dual rank

■ RoHS

DESCRIPTION

The W3HG128M72AEF is a 128Mx72 fully buffered 240-pin Double Data Rate 2 SDRAM memory module based on 512Mb DDR2 SDRAM components. The module consists of eighteen 128Mx4, in FBGA package and a AMB mounted on a 240 pin FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options

PERFORMANCE PARAMETERS

Speed Grade	Module Bandwidth	Peak Channel Throughput	Link Transfer Rate	Latency (CL-t_{RCD}-t_{RP})
665	PC2-5300	8.0 GB/s	4.0 GT/s	5-5-5
534	PC2-4200	6.4 GB/s	3.2 GT/s	4-4-4

* Consult factory for availability
Note: JEDEC has not yet adopted a final FBDIMM standard

PIN ASSIGNMENT – 240 PIN FBDIMM

| PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{DD}	61	PN9#	121	V_{DD}	181	SN9#
2	V_{DD}	62	V_{SS}	122	V_{DD}	182	V_{SS}
3	V_{DD}	63	PN10	123	V_{DD}	183	SN10
4	V_{SS}	64	PN10#	124	V_{SS}	184	SN10#
5	V_{DD}	65	V_{SS}	125	V_{DD}	185	V_{SS}
6	V_{DD}	66	PN11	126	V_{DD}	186	SN11
7	V_{DD}	67	PN11#	127	V_{DD}	187	SN11#
8	V_{SS}	68	V_{SS}	128	V_{SS}	188	V_{SS}
9	V_{CC}	69	V_{SS}	129	V_{CC}	189	V_{SS}
10	V_{CC}	70	PS0	130	V_{CC}	190	SS0
11	V_{SS}	71	PS0#	131	V_{SS}	191	SS0#
12	V_{CC}	72	V_{SS}	132	V_{CC}	192	V_{SS}
13	V_{CC}	73	PS1	133	V_{CC}	193	SS1
14	V_{SS}	74	PS1#	134	V_{SS}	194	SS1#
15	V_{TT}	75	V_{SS}	135	V_{TT}	195	V_{SS}
16	VID1	76	PS2	136	VID0	196	SS2
17	RESET#	77	PS2#	137	DNU/M_Test	197	SS2#
18	V_{SS}	78	V_{SS}	138	V_{SS}	198	V_{SS}
19	RFU²	79	PS3	139	RFU²	199	SS3
20	RFU²	80	PS3#	140	RFU²	200	SS3#
21	V_{SS}	81	V_{SS}	141	V_{SS}	201	V_{SS}
22	PN0	82	PS4	142	SN0	202	SS4
23	PN0#	83	PS4#	143	SN0#	203	SS4#
24	V_{SS}	84	V_{SS}	144	V_{SS}	204	V_{SS}
25	PN1	85	V_{SS}	145	SN1	205	V_{SS}
26	PN1#	86	RFU¹	146	SN1#	206	RFU¹
27	V_{SS}	87	RFU¹	147	V_{SS}	207	RFU¹
28	PN2	88	V_{SS}	148	SN2	208	V_{SS}
29	PN2#	89	V_{SS}	149	SN2#	209	V_{SS}
30	V_{SS}	90	PS9	150	V_{SS}	210	SS9
31	PN3	91	PS9#	151	SN3	211	SS9#
32	PN3#	92	V_{SS}	152	SN3#	212	V_{SS}
33	V_{SS}	93	PS5	153	V_{SS}	213	SS5
34	PN4	94	PS5#	154	SN4	214	SS5#
35	PN4#	95	V_{SS}	155	SN4#	215	V_{SS}
36	V_{SS}	96	PS6	156	V_{SS}	216	SS6
37	PN5	97	PS6#	157	SN5	217	SS6#
38	PN5#	98	V_{SS}	158	SN5#	218	V_{SS}
39	V_{SS}	99	PS7	159	V_{SS}	219	SS7
40	PN13	100	PS7#	160	SN13	220	SS7#
41	PN13#	101	V_{SS}	161	SN13#	221	V_{SS}
42	V_{SS}	102	PS8	162	V_{SS}	222	SS8
43	V_{SS}	103	PS8#	163	V_{SS}	223	SS8#
44	RFU	104	V_{SS}	164	RFU¹	224	V_{SS}
45	RFU	105	RFU²	165	RFU¹	225	RFU²
46	V_{SS}	106	RFU²	166	V_{SS}	226	RFU²
47	V_{SS}	107	V_{SS}	167	V_{SS}	227	V_{SS}
48	PN12	108	V_{DD}	168	SN12	228	SCK
49	PN12#	109	V_{DD}	169	SN12#	229	SCK#
50	V_{SS}	110	V_{SS}	170	V_{SS}	230	V_{SS}
51	PN6	111	V_{DD}	171	SN6	231	V_{DD}
52	PN6#	112	V_{DD}	172	SN6#	232	V_{DD}
53	V_{SS}	113	V_{DD}	173	V_{SS}	233	V_{DD}
54	PN7	114	V_{SS}	174	SN7	234	V_{SS}
55	PN7#	115	V_{DD}	175	SN7#	235	V_{DD}
56	V_{SS}	116	V_{DD}	176	V_{SS}	236	V_{DD}
57	PN8	117	V_{TT}	177	SN8	237	V_{TT}
58	PN8#	118	SA2	178	SN8#	238	V_{CC}SPD
59	V_{SS}	119	SDA	179	V_{SS}	239	SA0
60	PN9	120	SCL	180	SN9	240	SA1

PIN NAMES

Symbol	Descriptions
SCK	System Clock Input, positive line
SCK#	System Clock Input, negative line
PN0-PN13	Primary Northbound Data, positive lines
PN0#-PN13#	Primary Northbound Data, negative lines
PS0-PS9	Primary Southbound Data, positive lines
PS0#-PS9#	Primary Southbound Data, negative lines
SN0-SN13	Secondary Northbound Data, positive lines
SN0#-SN13#	Secondary Northbound Data, negative lines
SS0-SS9	Secondary Southbound Data, positive lines
SS0#-SS9#	Secondary Southbound Data, negative lines
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input/Output
SA0-SA2	SPD Address Inputs, also used to select the FBDIMM number in the AMB
VID0-VID1	Voltage ID: These pins must be unconnected for DDR2-based FBDIMMs. VID0 is V_{DD} value: OPEN=1.8V, GND=1.5V;VID1 is VCC value: OPEN=1.5V, GND=1.2V
RESET#	AMB reset signal
RFU	Reserved for Future Use
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5V)
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8V)
V_{TT}	DRAM Address/Command/Clock Termination Power ($V_{DD/2}$)
V_{CC}SPD	SPD Power
V_{SS}	Ground
DNU/M_TEST	Do Not Use

Note:
1. These pin positions are reserved for forwarded clocks to be used in future module implemenations
2. These pin positions are reserved for future architechture flexibility.
3. The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, PS9/PS9#, SS9/SS9#.
4. RFU = Reserved Future Use.

FUNCTIONAL BLOCK DIAGRAM
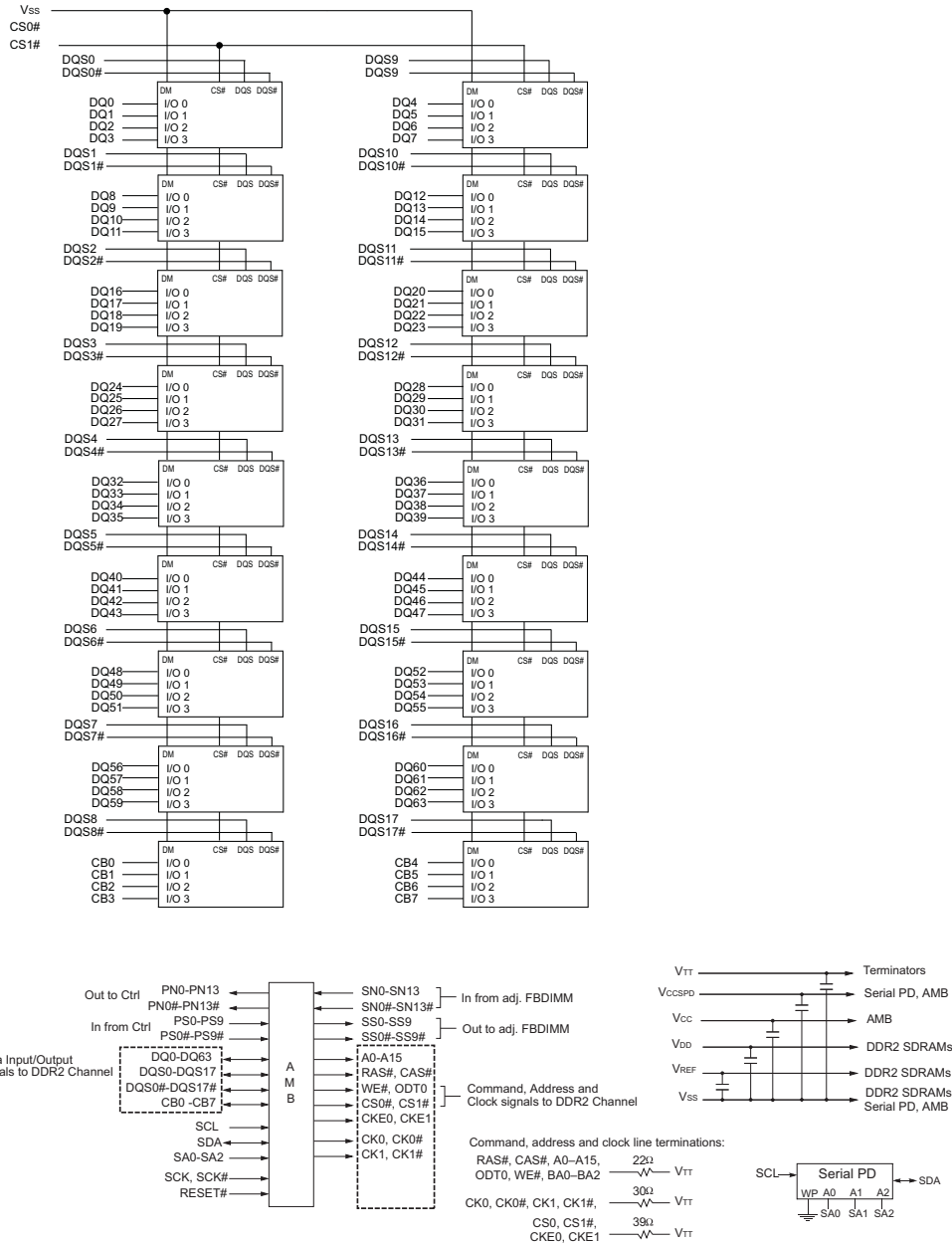
GENERAL DESCRIPTION

WEDC FBDIMM is a high-bandwidth, large-capacity-channel solution that has narrow host interface. FBDIMMs used DDR2 SDRAM devices isolated from the channel behind a buffer on the FBDIMM. Memory device capacity remains high and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 1, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase the reliability and availability of the memory subsystem.

WEDC FBDIMM features a novel architecture, including the AMB that isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and the DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, point-to-point, interface at 1.5V.

The AMB also allows buffering of memory traffic to support large memory capacities. All memory control for the DDR2 SDRAM devices resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The AMB interface is responsible for handling channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the memory channel.

FIGURE 1: FBDIMM Solution Block Diagram
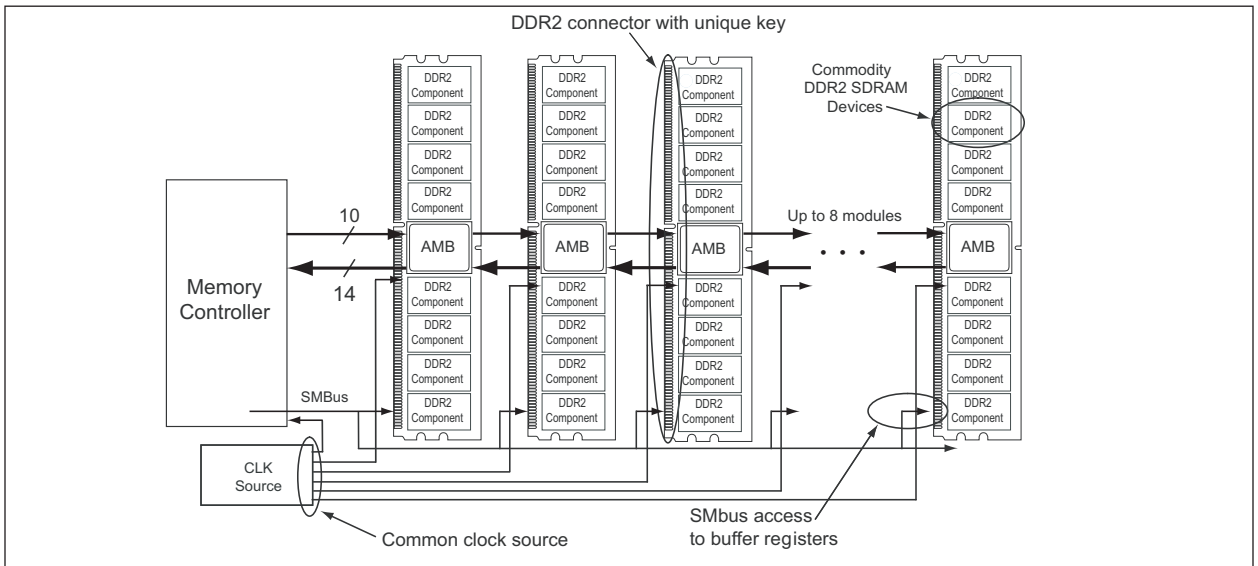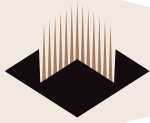
FUNCTIONAL DESCRIPTION

ADVANCED MEMORY BUFFER (AMB)

The AMB reference design complies with the "FBDIMM Architecture and Protocol Specification" (JEDEC standards, pending). It is expected that there will be multiple vendors for the AMB which will offer at least the minimum functionally as set forth in the industry specification. To achieve optimal operation and compatibility with DDR2 SDRAM device and host/controller offerings, each vendor's AMB will have a unique set of personality bytes contained in the SPD for setting up and fine tuning their device.

The FBDIMM specification defines a number of options to support the requirements of different applications. The capabilities of the AMB are communicated to the host during the initialization process in the TS2 training pattern and in bits readable in the features register in the AMB.

The AMB is responsible for handling FBDIMM channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the channel. A complete and detailed description of the AMB is contained in the proposed FBDIMM AMB Specification. The AMB is a memory interface that connects an array of DDR2 SDRAM devices to the FBDIMM channel. The AMB is a slave device on the channel responding to channel commands and forwarding channel commands to other AMB devices.

All memory control for the DDR2 SDRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power-management.

The AMB is expected to perform the following functions:

- Support channel initialization procedures as defined in the initialization chapter of the FBDIMM Architecture and Protocol Specification to align the clocks and the frame boundaries and verify channel connectivity

- Support the forwarding of southbound and northbound frames, servicing requests directed to a specific FBDIMM's AMB, as defined in the protocol chapter of the specification, and merging the return data into the northbound frames.

- Initialize northbound frames if the FBDIMM's AMB is the last, southern-most on the channel, initialize northbound frames.

- Detect errors on the channel and report them to the host memory controller

- Support the FBDIMM configuration register set as defined in the FBDIMM AMB specification register chapter of the specification

- Act as a DRAM memory buffer for all read, write, and configuration accesses addressed to a specific FBDIMM's AMB

- Provide a read and write buffer FIFO

- Supports an SMBus protocol interface for access to the AMB configuration registers

- Provide features to support MEMBIST and IBIST test functions

- Provide a register interface for the thermal sensor and status indicator

- Function as a repeater to extend the maximum length of FBDIMM Links

- Reconfigures FBDIMM inputs from differential high-speed link receivers to two single-ended, low-speed receivers (~200 MHz). These inputs directly control DDR2 command/address and input data that is replicated to all DDR2 SDRAMs devices.

- Bypass high-speed parallel serial circuitry and provide test results back to the tester, using low-speed FBDIMM outputs
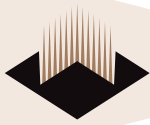
AMB INTERFACE

Figure 2: The AMB Interface Block Diagram illustrates the AMB and all of its interfaces. They consist of two FBDIMM links, one DDR2 channel and an SMBus interface. Each FBDIMM link connects the AMB to a host memory controller or an adjacent FBDIMM. The DDR2 channel supports direct connection to the DDR2 SDRAM on an FBDIMM.

The FBDIMM channel uses a daisy-chain topology to proved expansion from a single FBDIMM per channel to up to eight FBDIMMs per channel. The host sends data on the southbound link to the first FBDIMM, where it is received and redriven to the second FBDIMM. On the southbound data path, each FBDIMM receives the data and redrives the data to the next FBDIMM, until the last FBDIMM receives the data. The last FBDIMM in the chain initiates the transmission of northbound data in the direction of the host. On the northbound data path, each FBDIMM receives the data and redrives the data to the next FBDIMM until the host is reached.

FIGURE 2: AMB Interface Block Diagram

HIGH-SPEED, DIFFERENTIAL, POINT-TO-POINT LINK (AT 1.5V) INTERFACES

The AMB supports one FBDIMM channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide. It carries commands and write data from the host memory controller, or the adjacent FBDIMM in the host direction, to the next FBDIMM in the chain.
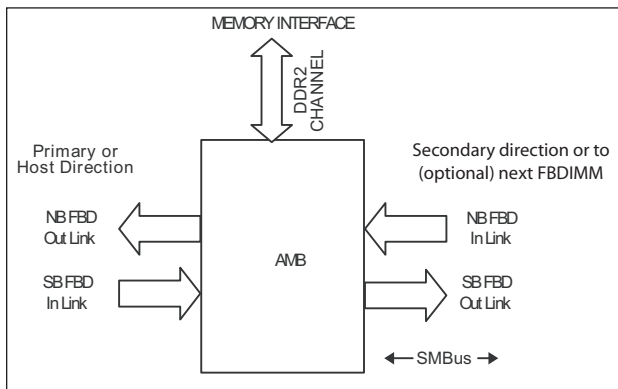
The northbound input link is 14 lanes wide. It carries read return data or status information from one FBDIMM to the next in the host direction and multiplexes in any internally generated READ return data or status information.

Data and commands sent to the DDR2 SDRAM devices travel southbound on 10 primary differential signal line pairs. Data and status information received from the DDR2 SDRAM devices travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent FBDIMM are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the upstream adjacent FBDIMM travel further northbound on 14 secondary differential parts.

DDR2 CHANNEL

The AMB DDR2 channel on the advanced memory buffer supports direct connection to DDR2 SDRAM devices. The DDR2 channel supports two ranks of eight banks with 16 row/column-request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support FBDIMM routing and electrical requirements. Four transfer burst are driven on the data and check-bit lines at 800 MHz.

Propagation delays can differ between read data/check-bit strobe lanes on a given channel. Each strobe can be calibrated by hardware state machines using WRITE/READ trial and error. Hardware aligns the read data and check-bits to a single core clock. The AMB provides four copies of the command clock phase reference (CLK[3:0]) and write data/check-bit strobes (DQS) for each DDR2 SDRAM device nibble.

SMBus SLAVE INTERFACE

The AMB supports a SMBus interface allows system access to configuration registers independent of the FBDIMM link. The AMB will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100KHz. SMBus access to the AMB may be a requirement to boot and to set link strength, frequency and other parameters needed to ensure robust configurations. It is also required for diagnostic

support when the high speed link is down. The SMBus address straps located on the FBDIMM connector are used to set the unique ID.

CHANNEL LATENCY

FBDIMM channel latency is measured from the time a read request is driven on the FBDIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.

When not using variable READ latency, the latency for a specific FBDIMM on a channel is always equal to the latency for any other FBDIMM on that channel. However, the latency for each FBDIMM in a specific configuration with some number of FBDIMMs installed may not be equal to the latency for each FBDIMM in a configuration with some different number of FBDIMMs installed. As more FBDIMMs are added to the channel, additional latency is required to read from each FBDIMM on the channel.

Because the channel is based on point-to-point interconnection of buffer components between FBDIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a four-FBDIMM channel configuration will have greater idle READ latency compared to a one FBDIMM channel configuration.

The variable READ latency capability can be used to reduce latency for FBDIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

PEAK THEORETICAL THROUGHPUT

An FBDIMM channel transfers READ completion data on the northbound data connection; 144 bits of data are transferred for every northbound data frame. This matches the 18-byte data transfer of an ECC DDR2 SDRAM device in a single DDR2 SDRAM command clock. A DDR2 SDRAM device burst of eight from a single channel, or burst of four from two lock-step channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). The AMB frame rate matches the

DDR2 SDRAM command clock because of the fixed 6:1 ratio of the FBDIMM channel clock to the DDR2 SDRAM command clock. Therefore, the northbound data connection will exhibit the same peak theoretical throughput as a single DDR2 SDRAM channel. For example, when using DDR2 533 componente, the peak theoretical bandwidth of the northbound data connection is 4.267 GB/sec.

Write data is transferred on the southbound command and data connection, via Command + Wdata frames; 72 bits of data are transferred per frame. Two Command + Wdata frames match the 18-byte data transfer of an ECC DDR2 SDRAM in a single DDR2 SDRAM command clock.

A DDR2 SDRAM burst of eight transfers from a single channel, or a burst of four from two lock-step channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). When the FBDIMM frame rate matches the DDR2 SDRAM command clock, the southbound command and data connection will exhibit one half the peak theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2-533 SDRAMs, the peak theoretical bandwidth of the southbound command and data connection is 2.133 GB/sec.

The total peak-theoretical throughput for a single FBDIMM channel is defined as the sum of the peak-theoretical throughput of the northbound data connection and the southbound command and data connection. When the FBDIMM frame rate matches the DDR2 SDRAM command clock, it equals 1.5 times the peak-theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2-533 SDRAMs, the peak theoretical throughput of a DDR2-533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBDIMM-533 channel would be 6.4 GB/sec.

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to V_{SS}

Symbol	Parameter	Min	Max	Units	Notes
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3	1.75	V	
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}	-0.3	1.75	V	
V_{DD}	Voltage V_{CC} pin relative to V_{SS}	-0.5	2.3	V	
V_{TT}	Voltage on V_{TT} pin relative to V_{SS}	-0.5	2.3	V	
T_{STG}	Storage temperature	-55	100	°C	
T_{CASE}	DDR2 SDRAM device operating temperature (Ambient)	0	95	°C	1, 2
	AMB device operating temperature (Ambient)	0	110	°C	

Stresses greater than those listed in absolute maximum rating table may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

NOTES:
1. T_{CASE} is specified at 95°C only when using 2X refresh timing ($^{t}REFI$ = 7.8μs at or below 85°C; $^{t}REFI$ = 3.9μs above 85°C);.DDR2 SDRAM component datasheet, though the FBDIMM does not have an IT option.
2. See applicable DDR2 SDRAM component datasheet for $^{t}REFI$ and extended mode register setting. The $^{t}REFI_{IT}$ parameter is used to specify the doubled refresh interval neccasary to sustain 95°C operation; however, the FBDIMM does not have an IT option.

INPUT DC VOLTAGE AND OPERATING CONDITIONS

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CC}	AMB supply voltage	1.455	1.50	1.575	V	
V_{DD}	DDR2 SDRAM supply voltage	1.7	1.8	1.9	V	
V_{TT}	Termination voltage	0.48 x V_{DD}	0.50 x V_{DD}	0.52 x V_{DD}	V	
V_{DDSPD}	SPD supply voltage	3.0	3.3	3.6	V	
$V_{IH(DC)}$	SPD Input HIGH (logic 1) voltage	2.1		V_{DDSPD}	V	1
$V_{IL(DC)}$	SPD Input LOW (logic 0) voltage			0.8	V	1
$V_{IH(DC)}$	RESET Input HIGH (logic 1) voltage	1.0			V	2
$V_{IL(DC)}$	RESET Input LOW (logic 0) voltage			0.5	V	1
I_L	Leakage Current (RESET)	-90		90	μA	2
I_L	Leakage Current (link)	-5		5	μA	3

NOTES:
1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal RESET#.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.

Timing Parameters

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EI assertion pass-through timing	^{t}EI Propagate			4	CK	
EI de assertion pass-through timing	^{t}EID			Bitlock	CK	2
EI assertion duration	^{t}EI	100			CK	1, 2
FBD command to DDR2 clock out that latches command			8.1		ns	3
FBD command to DDR2 WRITE			TBD		ns	
DDR2 READ to FBD (last FBDIMM)			5.0		ns	4
Resample pass-through time			1.075		ns	
Resynch pass-through time			2.075		ns	
Bitlock interval	^{t}Bitlock			119	frames	1
Framelock interval	^{t}Framelock			154	frames	1

Note: 1. Defined in FBDIMM architecture and protocol specification.

2. Clocks defined as core clocks - 2x SCK input

3. For DDR2-667 (PC2-5300), this is measured from the beginning of the frame at the southbound input to the DDR2 clock output that latches the first command of a frame to the DDR2 SDRAM devices

4. For DDR2-667 (PC2-5300), this is measured from the latest DQS input to the AMB to the start of the matching data frame at the northbound FBDIMM outputs.

AMB I$_{DD}$ SPECIFICATIONS AND CONDITIONS

Symbol	Condition		806	665	534	Units
Idd_Idle_0	Idle Current, single or last DIMM, LO state, idle (0 BW), Primary channel enabled, Secondary Channel disabled , CKE high. Command and address lines stable. DRAM clock active	@1.5v	TBD	2.6	2.2	A
		@1.8v	TBD	0.9	0.9	A
Idd_Idle_1	Idle Current, first DIMM, LO state, idle (0 BW), Primary and Secondary channels enabled CKE high, Command and address lines stable. DRAM clock active.	@1.5v	TBD	3.4	3.0	A
		@1.8v	TBD	0.9	0.9	A
Idd_Active_1	Active Power, LO state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5v	TBD	3.9	3.4	A
		@1.8v	TBD	1.7	1.7	A
Idd_Active_2	Active Power, LO state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5v	TBD	3.7	3.2	A
		@1.8v	TBD	0.9	0.9	A
Idd_Training	Training, Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5v	TBD	4.0	3.5	A
		@1.8v	TBD	0.9	0.9	A

V_TT CURRENTS

Parameter	Symbol	Typ	Max	Unit
Idle current, DDR2 SDRAM device power down	ITT1	500	700	mA
Active power, 50% DDR2 BW	ITT2	500	700	mA

REFERENCE CLOCK INPUT SPECIFICATIONS

Parameter	Symbol	Values		Unit	Notes
		Min	Max		
Reference clock frequency	f_{SCK}	133.33	200	MHz	1, 2
Rise time, fall time	$T_{SCK-RISE}$, $T_{SCK-FALL}$	175	700	ps	3
Voltage high	$V_{SCK-HIGH}$	600	850	mV	
Voltage low	$V_{SCK-LOW}$	-150		mV	
Absolute crossing point	$V_{CROSS-ABS}$	250	550	mV	4
Relative crossing point	$V_{CROSS-REL}$	calculated	calculated		4, 5
Percent mismatch between rise and fall times	$T_{SCK-RISE-FALL-MATCH}$	-	10	%	
Duty cycle of reference clock	$T_{SCK-DUTYCYCLE}$	40	60	%	
Clock leakage current	I_{I-CK}	-10	10	µA	6, 7
Clock input capacitance	C_{I-CK}	0.5	2	pF	7
Clock input capacitance delta	$C_{I\_CK (D)}$	-0.25	0.25	pF	8
Transport delay	T1		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}		Periods	11
Reference clock jitter, filtered	$T_{REF-JITTER}$		40	ps	12, 13
Reference clock deterministic jitter	T_{REF-DJ}		TBD	ps	

NOTES:

1. 133 MHz for PC2-4200 and 166MHZ for PC2-5300
2. Measured with SSC disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. $V_{CROSS\_REL\ (MIN)}$ and $V_{CROSS\_REL\ (MAX)}$ are derived using the following calculations: Min = 0.5 (V_{havg} -0.710) + 0.250; and Max = 0.5 (V_{havg} - 0.710) + 0.550, where V_{havg} is the average of $V_{SCK-HIGHM}$.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and SCK#.
8. Difference between SCK and SCK# input.
9. T1 = |Tdatapath - Tclockpath| (excluding PLL loop delays). This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter $T_{REF-JITTER}$.

10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX , to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the sampling point. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 10^{16} periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and total jitter at 10^{16} samples extrapolated from an estimated of the sigma of the random jitter components.
12. Measured with SSC enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal -Min parameters.

DIFFERENTIAL TRANSMITTER OUTPUT SPECIFICATIONS

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFF}$ p-p_L	900	1,300	mV	EQ 1, Note 1
Differential peak-to-peak output voltage for regular voltage swing	$V_{TX-DIFF}$ p-p_R	800		mV	EQ 1, Note 1
Differential peak-to-peak output voltage for small voltage swing	$V_{TX-DIFF}$ p-p_S	520		mV	EQ 1, Note 1
DC common code output voltage for large voltage swing	V_{TX-CM_L}		375	mV	EQ 2, Note 1
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	EQ 2, Note 1, 2
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	$V_{TX-CM-3.5-Ratio}$	-3.0	-4.0	dB	1, 3, 4
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	$V_{TX-CM-6.0-Ratio}$	-5.0	-7.0	dB	1, 3, 4
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-AC}$ p-p-L		90	mV	EQ3, Note 1, 5
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-AC}$ p-p-R		80	mV	EQ3, Note 1, 5
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-AC}$ p-p-S		70	mV	EQ3, Note 1, 5
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-SE}$		50	mV	6
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-DC}$		20	mV	6
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-DIFF}$ p-p		40	mV	
Single-ended voltage (w.r.t. V_{SS}) ON D+/D-	V_{TX-SE}	-75	750	mV	1, 7
Minimum TX eye width, 3.2 and 4.0 Gb/s	$T_{TX-EYE-MIN}$	0.7		UI	1, 8
Minimum TX eye width 4.8 Gb/s	$T_{TX-EYE-MIN\ 4.8}$	TBD		UI	1, 8
Maximum TX deterministic jitter, 3.2 and 4.8 Gb/s	$T_{TX-DJ-DD}$		0.2	UI	1, 8, 9
Maximum TX eye width 4.8 Gb/s	$T_{TX-DJ-DD-4.8}$		TBD	UI	1, 8, 9
Instantaneous pulse width	$T_{TX-PULSE}$	0.85		UI	10
Differential TX outout rise/fall time	$T_{TX-RISE}\ T_{TX-FALL}$	30	90	ps	20-80% voltage, Note 1
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$		20	ps	
Differential return loss	$RL_{TX-DIFF}$	8		dB	1GHz - 2.4GHz Note 11
Common mode return loss	RL_{TX-CM}	6		dB	1GHz - 2.4GHz Note 11
Transmitter termination impender	R_{TX}	41	55	Ω	12
D+/D- TX Impedance difference	$R_{TX-MATCH\ -DC}$		4	%	EQ; 4 Boundaries are applied separately to high and low output voltage states
Lane-to lane skew at Tx	$L_{TX-SKEW\ 1}$		100 + 3UI	ps	13, 15
Lane-to lane skew at TX	$L_{TX-SKEW\ 2}$		100 + 2UI	ps	14, 15

DIFFERENTIAL TRANSMITTER OUTPUT SPECIFICATIONS

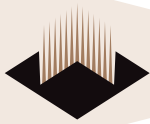| Parameter	Symbol	Values		Units	Comments
		Min	Max		
Maximum TX Drift (resync mode)	$T_{TX-DRIFT-RESYNC}$	—	240	ps	16
Maximum TX Drift (resample mode only)	$T_{TX-DRIFT-RESAMPLE}$	—	120	ps	16
Bit Error Ratio	BER	10^{-12}	—	—	17

NOTES:

1. Specified at the package pins into a timing and voltage compliance test load as shown in Figure 4-2 and in steps outlined in 4.1.2.1 of the JEDEC specification. Common-mode measurements to be performed using a 101010 pattern.
2. The transmitter designer should not artificially elevate the common mode in order to meet this specification.
3. This is the ration of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
4. De-emphasis shall be disabled in the calibration state.
5. Includes all sources of AC common mode noise.
6. Sinlge-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
7. The maximum value is specified to be at least (VTX-DIFFp-pL/4) + (VTX-CM-ACp-p2).
8. This number does not include the effects of SSC or reference clock jitter.
9. Defined as the expected maximum jitter for the given probability as measured in the system (JJ), less the unbounded jitter

10. Pulse width measure at 0V differential.
11. One of the components that contribute to the deterioration of the return loss is the ESB structure which needs to be carefully designed.
12. The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed +/- 5 W with regard to the average of the values measured at 100 mV and 400 mV for that pin.
13. Lane to Lane skew at the Transmitter pins for an end component.
14. Lane to Lane skew at the Transmitter pins or an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
15. This is a static skew. An FBDIMM component is not allowed to change its lane to lane phase relationship after initialization.
16. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate change is significantly below the tracking capability of the receiver.
17. BER per differential lane.

$$V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}| \qquad \text{(EQ 1)}$$
$$V_{TX-CM} = DC_{(avg)} \text{ of } (|V_{TX-D+} + V_{TX-D-}|/2) \qquad \text{(EQ 2)}$$
$$V_{TX-CM-AC} = ((Max|V_{TX-D+} + V_{TX-D-}|)/2) - (Min |V_{TX-D+} + V_{TX-D-}|)/2) \qquad \text{(EQ 3)}$$
$$R_{TX-MATCH-DC} = 2 \times ((|R_{TX-D+} - R_{TX-D-}|)/(R_{TX-D+} + R_{TX-D-}|)) \qquad \text{(EQ 4)}$$

DIFFERENTIAL RECEIVER INPUT SPECIFICATIONS

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFF}$ p-p	170	TBD	mV	EQ 5, Note 1
Maximum single-ended voltage in EI condition	$V_{RX-IDLE-SE}$	—	75	mV	2, 3
Maximum single-ended voltage in EI condition (DC only)	$V_{RX-IDLE-SE-DC}$	—	50	mV	2, 3
Maximum peak-to-peak differential voltage in EI condition	$V_{RX-IDLE-DIFF}$ p-p	—	65	mV	3
Sinlge-ended voltage (w.r.t. V_{SS} on D+/D-	V_{RX-SE}	-300	900	mV	4
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85	—	mV	4, 5
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$	—	TBD	—	4, 6
Maximum RX inherent timing error, 3.2 and 4.0 Gb/s	$T_{RX-TJ-MAX}$	—	0.4	UI	4, 7, 8
Maximum RX inherent deterministic timing error, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX\ 4.8}$	—	TBD	UI	4, 7, 8
Single-pulse width as zero-voltage crossing	$V_{RX-DJ-DD}$	—	0.3	UI	4, 7, 8, 9
Single-pulse width at minimum-level crossing	$V_{RX-DJ-DD-4.8}$	—	TBD	UI	4, 7, 8, 9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55	—	UI	4, 5
Common mode of the input voltage	$T_{RX-PW-ML}$	0.2	—	UI	4, 5
Differential RX outout rise/fall time	$T_{RX-RISE}\ T_{RX-FALL}$	50	—	ps	20-80% voltage
Common mode of input voltage	V_{RX-CM}	120	400	mV	EQ6, Note1, 10
AC peak-to-peak common mode of input voltage	$V_{RX-CM-H-AC}$ p-p	—	270	mV	EQ7, Note1
Ratio of $V_{RX-CM-AC}$p-p to minimum $V_{RX-DIFF}$p-p	$V_{RX-CM-EH-RATOP}$	—	45	%	11
Differential return loss	$RL_{RX-DIFF}$	9	—	dB	Meas. 0.1-2.4GHz, Note 12
Common mode return loss	RL_{RX-CM}	6	—	dB	Meas. 0.1-2.4GHz, Note 12
RX termination impedance	R_{RX}	41	55	Ω	13
D+/D- RX Impedance difference	$R_{RX-MATCH-DC}$	—	4	%	EQ 8
Lane-to lane PCB skew at RX	$L_{RX-PCB-SKEW}$	—	6	UI	Lane-to-lane skew at the receiver that must be tolerated. Note 14
Minimum RX drift tolerance	$T_{RX-DRIFT}$	400	—	ps	15
Minim data tracking 3dB bandwidth	F_{TRK}	0.2	—	MHz	16
Electrical idle entry detect time	$T_{EI-ENTRY-DETECT}$	—	60	ns	17
Electrical idle exit detect time	$T_{EI-EXIT-DETECT}$	—	30	ns	—
Bit Error Ratio	BER	—	10^{-12}	—	18

NOTES:

1. Specified at the package pins into a timing and voltage compliance test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst- case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.

4.. Specific at the package pins into a timing and voltage compliance test setup
5. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask .
6. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
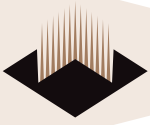
7. This number does not include the effects of SSC or reference clock jitter.

8. This number includes setup and hold of the RX sampling flop.

9. Defined as the dual-dirac deterministic timing error.

10. Allows for 15mV DC offset between transmit and receive devices.

11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if VRX-DIFFp-p is 200mV, the maximum AC peak-to-peak common mode is the lesser of (200mV x 0.45=90mV) and VRX-CM-AC-p-p.

12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.

13. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shell not exceed +/- 5W with regard to the average of the values measured at 100mV and at 400mV for that pin.

14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.

15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.

16. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI.

17. The specified time includes the time required to forward the EI entry condition.

18. BER per differential lane.

$$V_{RX-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}| \qquad \text{(EQ 5)}$$

$$V_{RX-CM} = DC_{(avg)} \text{ of } (|V_{RX-D+} + V_{RX-D-}|/(2)) \qquad \text{(EQ 6)}$$

$$V_{RX-CD-AC} = ((\text{Max}|V_{RX-D+} + V_{RX-D-}|)/(2)) - ((\text{Min }|V_{RX-D+}+V_{RX-D-}|)/2) \qquad \text{(EQ 7)}$$

$$R_{RX-MATCH-DC} = 2x \left((|R_{RX-D+} - R_{RX-D-}|)/(|R_{R-D+}+R_{RX-D-}|)\right) \qquad \text{(EQ 8)}$$

ORDERING INFORMATION FOR F1 (FmHS) Full metal Heat Spreader

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
W3HG128M72AEF806F1xxG**	400MHz/800Mb/s	6	6	6	30.35 (1.20") NOM
W3HG128M72AEF665F1xxG	333MHz/667Mb/s	5	5	5	30.35 (1.20") NOM
W3HG128M72AEF534F1xxG	266MHz/533Mb/s	4	4	4	30.35 (1.20") NOM

** Consult factory for availability

NOTES:

• G = RoHS Compliant
• Vendor specific part numbers are used to provide memory components for source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
• For the AMB, a specific character is used to provide component source control. The place holder for this is shown as lower case "x" (next to the G) in the part number above.
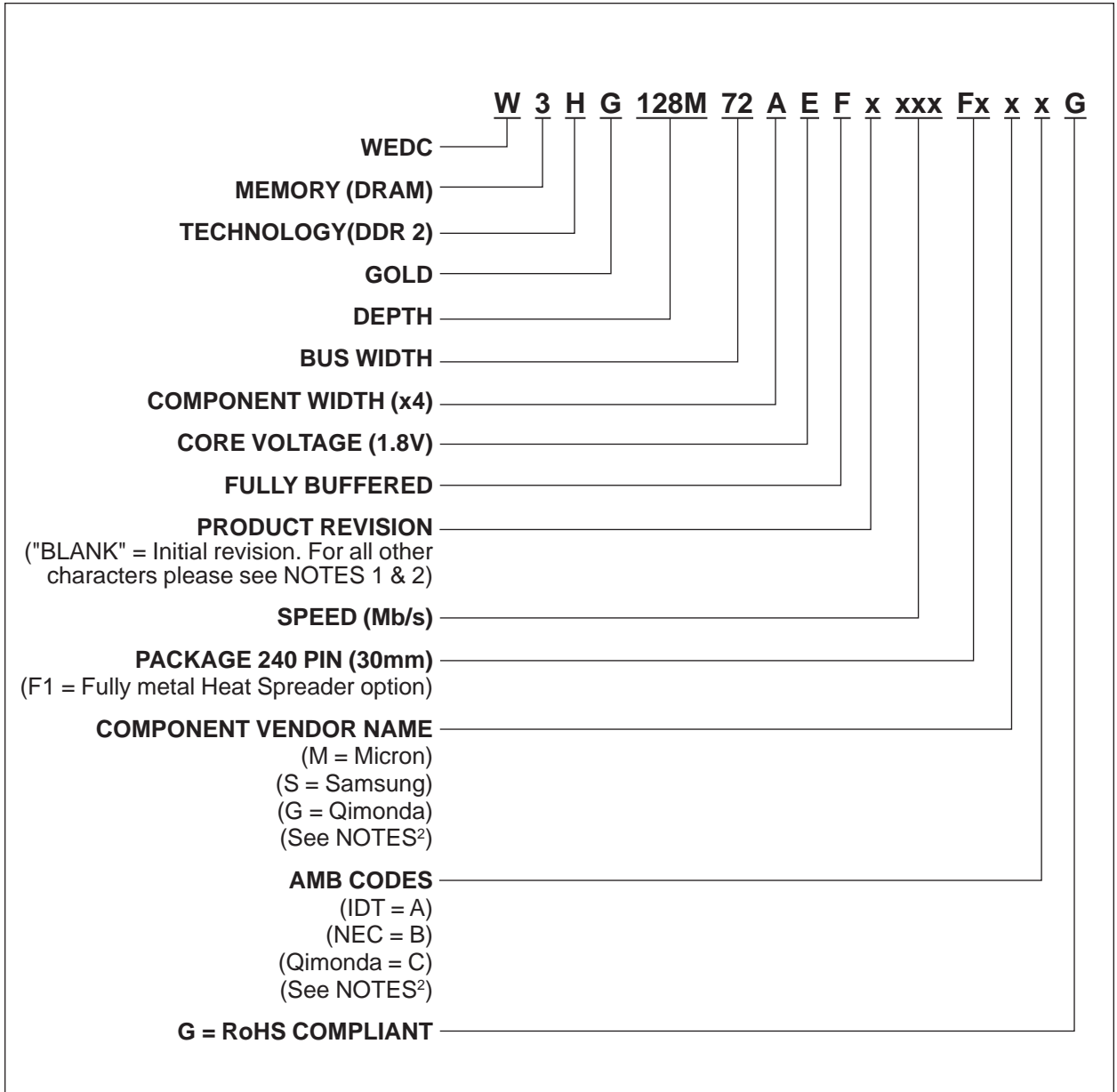
PACKAGE DIMENSIONS FOR F1 (FmHS) Full metal Heat Spreader

FRONT VIEW WITH HEAT SPREADER

BACK VIEW WITH HEAT SPREADER
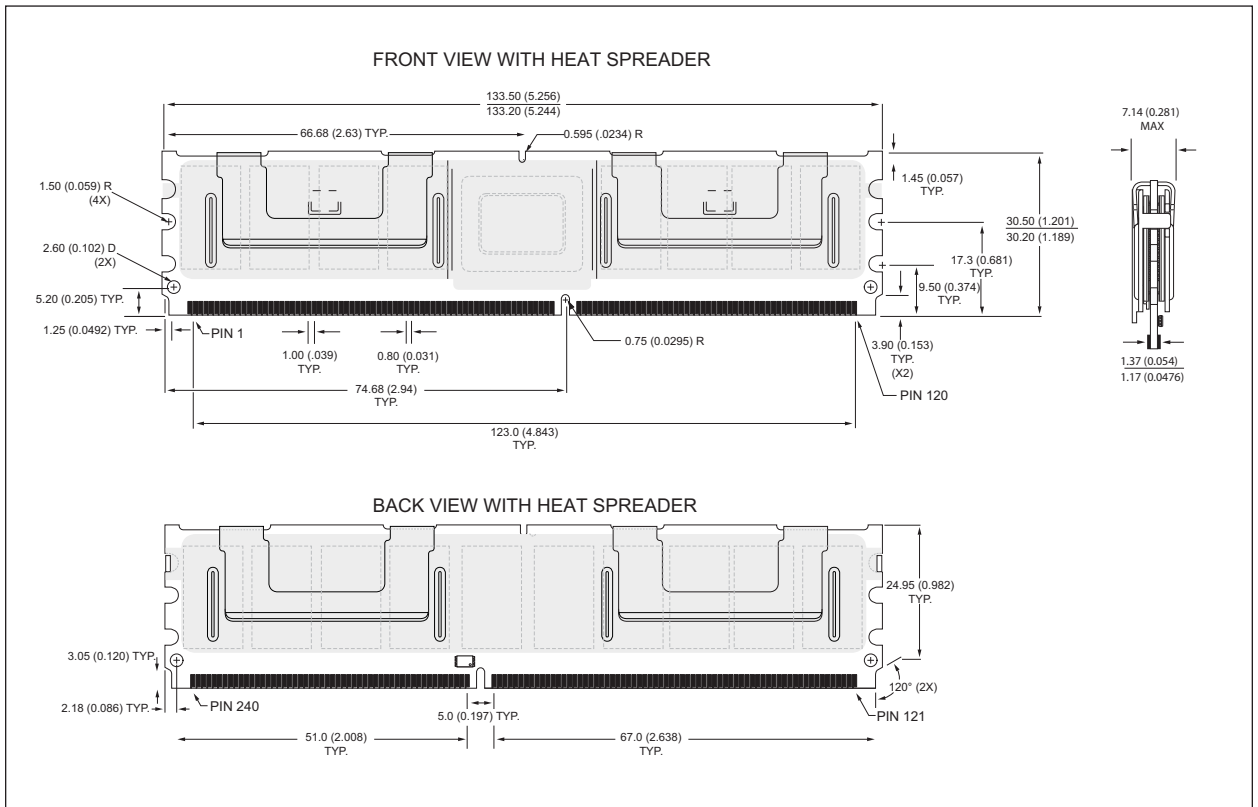
* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE

W 3 H G 128M 72 A E F x xxx Fx x x G

WEDC ——

MEMORY (DRAM) ——

TECHNOLOGY(DDR 2) ——

GOLD ——

DEPTH ——

BUS WIDTH ——

COMPONENT WIDTH (x4) ——

CORE VOLTAGE (1.8V) ——

FULLY BUFFERED ——

PRODUCT REVISION
("BLANK" = Initial revision. For all other
characters please see NOTES 1 & 2)

SPEED (Mb/s) ——

PACKAGE 240 PIN (30mm)
(F1 = Fully metal Heat Spreader option)

COMPONENT VENDOR NAME
(M = Micron)
(S = Samsung)
(G = Qimonda)
(See NOTES[2])

AMB CODES
(IDT = A)
(NEC = B)
(Qimonda = C)
(See NOTES[2])

G = RoHS COMPLIANT ——
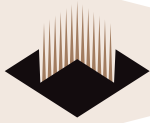
NOTE[1]: This character represents the general product revision that is used to control and record any changes in the AMB and
memory die revision, as well as any other design changes.

NOTE[2]: In order to obtain the most current revision, please contact the factory.

Document Title

1GB – 128Mx72 DDR2 SDRAM FBDIMM

DRAM Options:

- SAMSUNG: C = DIE
- MICRON: D = DIE
- QIMONDA: F = DIE

AMB OPTION:

- IDT = REV. A5
- NEC = REV. K (B5+)
- QIMONDA: TBD

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	September 2006	Concept
Rev 1	1.0 Update to part number guide	September 2006	Concept
Rev 2	2.0 Corrected Package Spec 2.1 Updated Part Numbering Guide	October 2006	Concept
Rev 3	3.0 Update DC voltage and operating conditions 3.1 Updated DDR2 I_{DD} specs 3.2 Moved from concept to advanced	September 2007	Advanced