LS73 LS76 LS107 LS112 LS113 — Dual J-K Negative-Edge-Triggered Flip-Flops

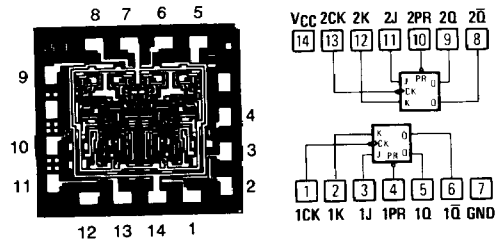
•Pin-for-Pin and functional equivalents to 5473, 5476, 54107, 54S112, 54S113

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

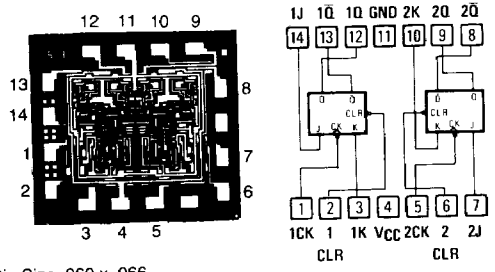
PIN-OUT DIAGRAMS

LS113



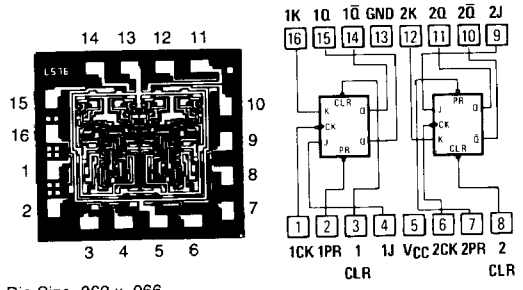
Die Size .060 x .066

LS73



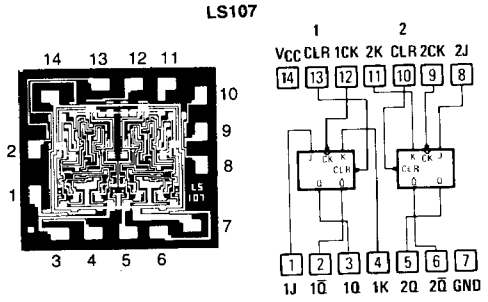
Die Size .060 x .066

LS76



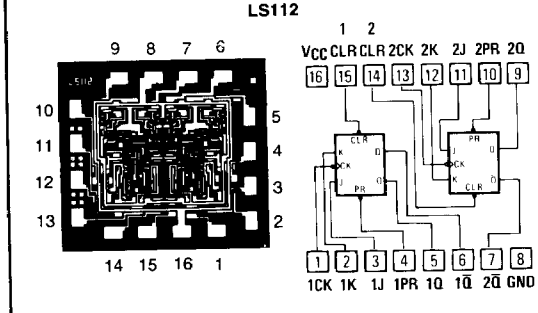
Die Size .060 x .066

LS107



Die Size .060 x .066

LS112



Die Size .060 x .066

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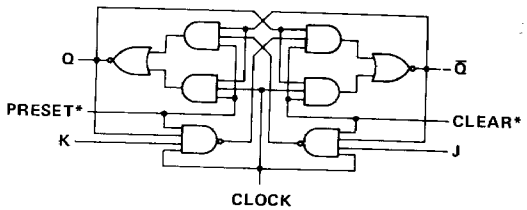
LOGIC DIAGRAM (½)



	PRESET	CLEAR
LS73		X
LS76	X	X
LS107		X
LS112	X	X
LS113	X	

LS73, LS107
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

LS113
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

LS76, LS112
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Dual J-K Negative-Edge-Triggered Flip-Flops

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		15			15			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time, t_{setup}		15			15			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0	0	70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the falling edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the falling edge of the clock in order to insure recognition. These devices require no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.50	
I_I	J or K					0.1			0.1	mA
	Clock	V_{CC}=MAX, V_I=7V				0.4			0.4	
	Preset or Clear					0.3			0.3	
I_{IH}	J or K					20			20	μA
	Clock	V_{CC}=MAX, V_I=2.7V				80			80	
	Preset or Clear					60			60	
I_{IL}	J or K					-0.4			-0.4	mA
	Clock	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	
	Preset or Clear					-0.8			-0.8	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX, See Note 1			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5V; then with clock, J, K, and preset grounded and clear at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
f_{max}				35	50					MHz
t_{PLH} CLR,PR		8	12		8	12		11	15	ns
t_{PHL} CLR,PR		14	19		11	17		13	18	ns
t_{PLH} CK		8	12		8	12		10	14	ns
t_{PHL} CK		13	18		11	16		11	16	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
f_{max}										MHz
t_{PLH} CLR,PR		10	14		10	15		13	17	ns
t_{PHL} CLR,PR		19	24		17	22		18	23	ns
t_{PLH} CK		10	14		10	14		14	18	ns
t_{PHL} CK		18	23		15	20		15	20	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.