AMERICAN MICROSYSTEMS, INC.

FS6058-01

LVPECL to HCSL/LVTTL Motherboard Clock Driver IC

November 2000

Preliminary Information

1.0 Features

- Distributes one differential LVPECL reference clock to six differential HCSL clock pairs and two single-ended LVTTL MREF clocks
- HCSL current levels controlled by IREF current reference and MULT_0:1 current multiplier pins
- Host clock frequency division selected via the SEL_A, SEL_B, and SEL_U input signals
- Active-low PWR_DWN# signal disables all outputs
- Tristate output control via SEL_T facilitates board testing
- Available in a 48-pin SSOP and TSSOP

Figure 1: Block Diagram

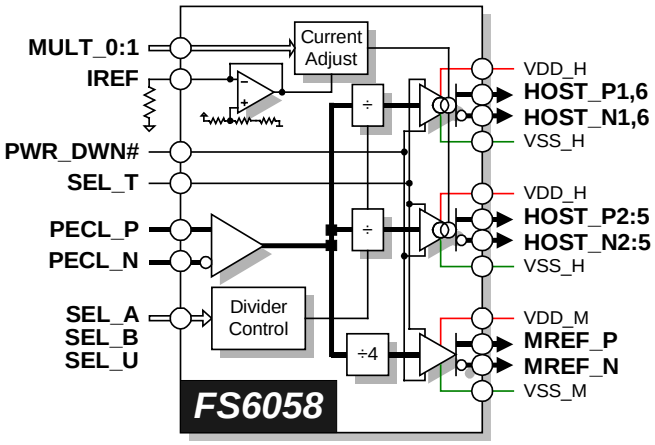


Figure 2: Pin Configuration

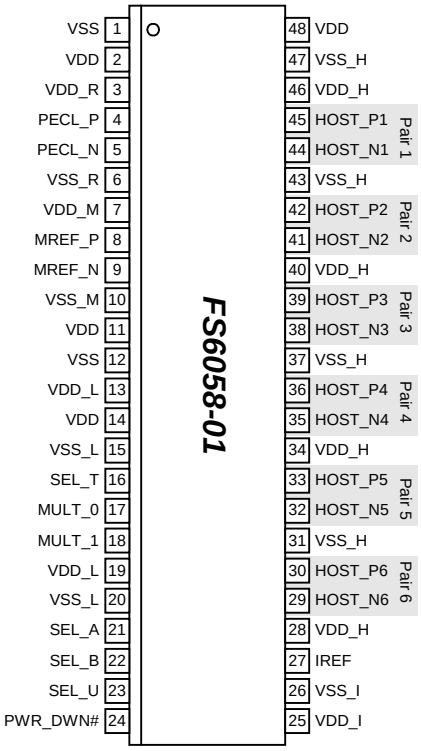


Table 1: Divider and Power-Down Control

CONTROL INPUTS					CLOCK OUTPUTS (MHz)						
PWR_ DWN#	SEL_ T	SEL_ A	SEL_ B	SEL_ U	HOST_P1 HOST_N1	HOST_P2 HOST_N2	HOST_P3 HOST_N3	HOST_P4 HOST_N4	HOST_P5 HOST_N5	HOST_P6 HOST_N6	MREF_P MREF_N
1	0	0	0	0	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 4
1	0	0	0	1	tristate	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	tristate	PECL ÷ 4
1	0	0	1	0	PECL ÷ 4	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 4	PECL ÷ 4
1	0	0	1	1	PECL ÷ 4	PECL ÷ 4	PECL ÷ 4	PECL ÷ 4	PECL ÷ 4	PECL ÷ 4	PECL ÷ 4
1	0	1	0	0	PECL	PECL	PECL	PECL	PECL	PECL	PECL ÷ 4
1	0	1	0	1	tristate	PECL	PECL	PECL	PECL	tristate	PECL ÷ 4
1	0	1	1	0	PECL ÷ 2	PECL	PECL	PECL	PECL	PECL ÷ 2	PECL ÷ 4
1	0	1	1	1	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2	PECL ÷ 2
1	1	X	X	X	tristate	tristate	tristate	tristate	tristate	tristate	tristate
0	X	X	X	X	HOST_P1 = 2× IREF	HOST_P2 = 2× IREF	HOST_P3 = 2× IREF	HOST_P4 = 2× IREF	HOST_P5 = 2× IREF	HOST_P6 = 2× IREF	MREF_P = high
					HOST_N1 = tristate	HOST_N2 = tristate	HOST_N3 = tristate	HOST_N4 = tristate	HOST_N5 = tristate	HOST_N6 = tristate	MREF_N = low

Table 2: Pin Descriptions

AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION			SUPPLY
44	AO	HOST_N1	Differential output pair 1	Outside Pair	Current-steering differential current-mode (HCSL) outputs provided for clocking the CPU. The output drive current is established via a reference current at IREF and a multiplying factor set by MULT_0:1	VDD_H
45		HOST_P1				
41	AO	HOST_N2	Differential output pair 2	Inside Pairs		
42		HOST_P2				
38	AO	HOST_N3	Differential output pair 3			
39		HOST_P3				
35	AO	HOST_N4	Differential output pair 4			
36		HOST_P4				
32	AO	HOST_N5	Differential output pair 5			
33		HOST_P5				
29	AO	HOST_N6	Differential output pair 6	Outside Pair		
30		HOST_P6				
27	AI	IREF	A fixed precision resistor from this pin to ground provides a reference current used for the differential current-mode HOST clock outputs			VDD_I
9	DO	MREF_N	Single-ended clock (180° out of phase with MREF_P) provided as a reference clock to a memory clock driver			VDD_M
8	DO	MREF_P	Single-ended clock in a pair of outputs reference clock to a memory clock driver			
17, 18	DI	MULT_0 MULT_1	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs			VDD_L
5	AI	PECL_N	Differential Input	LVPECL input (complementary)		VDD_R
4		PECL_P		LVPECL input (true)		
24	DI	PWR_DWN#	Asynchronous active-low LVTTL power-down signal forces MREF outputs low, tristates HOST_N outputs, and drives HOST_P output currents to 2xIREF			VDD_I
21	DI	SEL_A	Used in conjunction with SEL_B and SEL_U to select desired output frequencies			VDD_L
22	DI	SEL_B	Used in conjunction with SEL_A and SEL_U to select desired output frequencies			
16	DI	SEL_T	Active high input tristates all outputs			
23	DI	SEL_U	Used in conjunction with SEL_A and SEL_B to select desired output frequencies			
2, 11, 14, 48	P	VDD	3.3V core power supply			-
28, 34, 40, 46	P	VDD_H	3.3V power supply for the differential HOST clock outputs			
25	P	VDD_I	3.3V power supply for IREF current reference input			
13, 19	P	VDD_L	3.3V power supply for logic input pins			
7	P	VDD_M	3.3V power supply for MREF clock outputs			
3	P	VDD_R	3.3V power supply for PECL reference clock inputs			
1, 12	P	VSS	Core ground			
31, 37, 43, 47	P	VSS_H	Ground for the differential HOST clock outputs			
26	P	VSS_I	Ground for IREF current reference input			
15, 20	P	VDD_L	Ground for logic input pins			
10	P	VSS_M	Ground for the MREF clock outputs			
6	P	VSS_R	Ground for PECL inputs			

2.0 HOST Buffer Current Control

The current supplied at the HOST outputs is controlled by two parameters: (1) the value of the programming resistor from the IREF pin to ground (VSS), and (2) the multiplier factor determined by the logic setting of the MULT_0 and MULT_1 pins.

The HOST output current is a mirrored and scaled copy of the reference current flowing through the programming resistor on the IREF pin. The voltage that appears at the IREF pin is one-third of the voltage at the VDD_I pin. Therefore, the reference current is

$$I_{REF} = \frac{\left(\frac{1}{3} \times \text{VDD\_I}\right)}{R_{IREF}}.$$

The mirrored reference current can be increased by adding one or more copies of the mirror current together. The additional current is controlled by the logic settings on the MULT_0 and MULT_1 pins.

Table 3: Current Multiplier

MULT_0	MULT_1	MULTPLIER
0	0	$I_O = 5 \times I_{REF}$
0	1	$I_O = 6 \times I_{REF}$
1	0	$I_O = 4 \times I_{REF}$
1	1	$I_O = 7 \times I_{REF}$

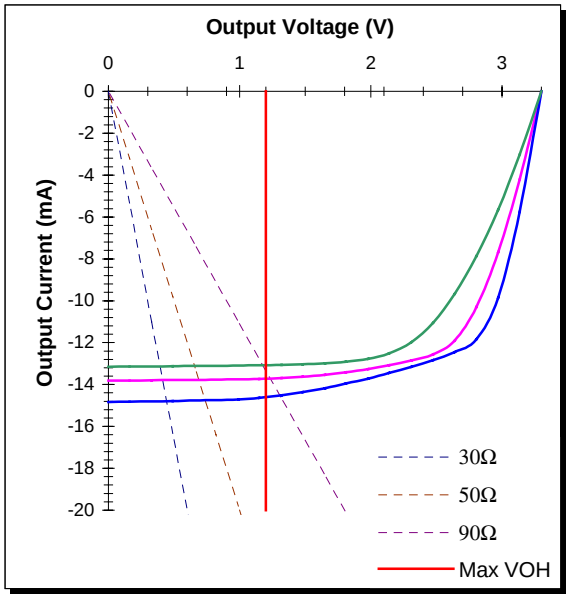
Table 4: HOST Current Selection

PROGRAM RESISTOR	REFERENCE CURRENT	CURRENT MULTIPLIER	TRACE IMPEDANCE	OUTPUT VOLTAGE
475Ω (1%)	2.32mA	$I_O = 5 \times I_{REF}$	60Ω	0.71V
			50Ω	0.59V
475Ω (1%)	2.32mA	$I_O = 6 \times I_{REF}$	60Ω	0.85V
			50Ω	0.71V
475Ω (1%)	2.32mA	$I_O = 4 \times I_{REF}$	60Ω	0.56V
			50Ω	0.47V
475Ω (1%)	2.32mA	$I_O = 7 \times I_{REF}$	60Ω	0.99V
			50Ω	0.82V
221Ω (1%)	5mA	$I_O = 5 \times I_{REF}$	30Ω	0.75V
			25Ω	0.62V
221Ω (1%)	5mA	$I_O = 6 \times I_{REF}$	30Ω	0.90V
			25Ω	0.75V
221Ω (1%)	5mA	$I_O = 4 \times I_{REF}$	30Ω	0.60V
			25Ω	0.50V
221Ω (1%)	5mA	$I_O = 7 \times I_{REF}$	30Ω	1.05V
			25Ω	0.84V

NOTE: Shaded row indicates the Primary System Configuration

Table 5: HOST Buffer Clock Outputs

Output Voltage (V)	HIGH DRIVE CURRENT (mA) AT PRIMARY SYSTEM CONFIGURATION		
	MIN.	TYP.	MAX.
3.30	0.00	0.00	0.00
3.14	-3.03	-4.22	-5.76
2.97	-5.66	-7.68	-9.86
2.81	-7.87	-10.30	-11.85
2.64	-9.67	-11.91	-12.45
2.48	-11.05	-12.56	-12.84
2.31	-11.98	-12.85	-13.16
2.14	-12.52	-13.07	-13.45
1.98	-12.77	-13.26	-13.72
1.81	-12.91	-13.42	-13.96
1.65	-12.99	-13.54	-14.17
1.48	-13.04	-13.64	-14.36
1.32	-13.07	-13.70	-14.52
1.15	-13.08	-13.73	-14.64
0.99	-13.09	-13.75	-14.71
0.82	-13.11	-13.76	-14.74
0.66	-13.12	-13.78	-14.76
0.49	-13.13	-13.79	-14.78
0.33	-13.13	-13.80	-14.80
0.16	-13.14	-13.81	-14.82
0.00	-13.15	-13.82	-14.83



Data in this table represents nominal characterization data only

3.0 Electrical Specifications

Table 6: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 7: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	Core (VDD)	3.135	3.3	3.465	V
		Clock Buffers (VDD_H, VDD_I, VDD_M, VDD_R, VDD_L)	3.135	3.3	3.465	V
Operating Temperature Range	T_A		0		70	°C
Reference Frequency Range						MHz
Input Rise/Fall Time				200		ps
Input Duty Cycle			40		60	%
Input High-Level Voltage		Required LVPECL signalling parameters	2.135		2.420	V
Input Low-Level Voltage			1.490		1.825	V
Load Capacitance	C_L	MREF_P, MREF_N	10		30	pF
Load Resistance	R_L	HOST_P1 to HOST_P6, HOST_N1 to HOST_N6	20		105	Ω

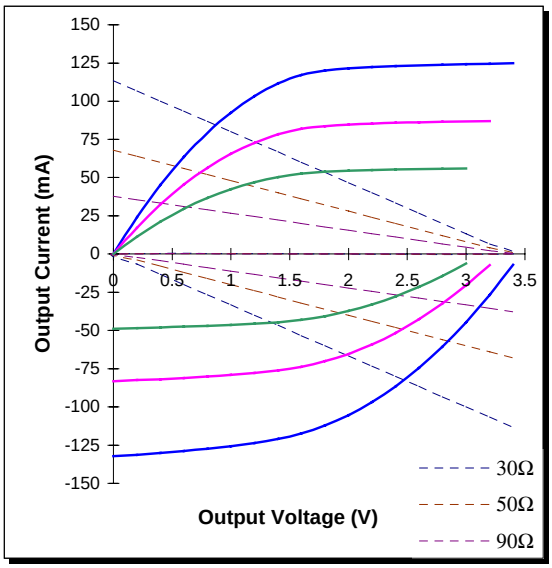
Table 8: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{HOST} = 133MHz; all supplies = 3.465V, R_{IREF}= 475Ω, $I_{OH} = 6 \times I_{REF}$				mA
Supply Current, Static	I_{DDs}	PWR_DWN# low, all supplies = 3.465V, R_{IREF}= 475Ω, $I_{OH} = 6 \times I_{REF}$				µA
LVTTL Digital Inputs (PWR_DWN#, MULT_0, MULT_1, SEL_U, SEL_A, SEL_B, SEL_T)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_{IL}		-5		+5	µA
PECL Reference Inputs (PECL_P, PECL_N)						
High-Level Input Voltage	V_{IH}					
Low-Level Input Voltage	V_{IL}					
Input Leakage Current	I_{IL}					
Current Reference (IREF)						
Bias Voltage	V_{OH}	no load		1.1		V
Short Circuit Output Source Current	I_{OH}	V_O = 0V				mA
MREF_P, MREF_N Clock Outputs (Type 5 Clock Driver)						
High Level Output Source Current	$I_{OH\ min}$	VDD_M, VDD_R, VDD_66 = 3.135V, V_O = 1.0V	-33			mA
	$I_{OH\ max}$	VDD_M, VDD_R, VDD_66 = 3.465V, V_O = 3.135V			-33	
Low Level Output Sink Current	$I_{OL\ min}$	VDD_M, VDD_R, VDD_66 = 3.135V, V_O = 1.95V	30			mA
	$I_{OL\ max}$	VDD_M, VDD_R, VDD_66 = 3.465V, V_O = 0.4V			38	
Output Impedance	z_{OL}	Measured at 1.65V, output driving low	12		55	Ω
	z_{OH}	Measured at 1.65V, output driving high	12		55	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_O = 0V; shorted for 30s, max.		-51		mA
Short Circuit Output Sink Current	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		62		mA
HOST_P1:4, HOST_N1:4 Clock Outputs (Type X1 Clock Buffer)						
Crossover Voltage	V_X	R_S = 33.2Ω, R_P = 49.9Ω, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$	45		55	$\%V_{OH}$
High-Level Output Source Current	I_{OH}	V_O = 0.65V, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$	12.9			mA
		V_O = 0.74V, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$			14.9	
Output Source Current Tolerance	ΔI_{OH}	V_{DD} = 3.30V, over settings in Table 4	-7		+7	$\%I_{OH}$
		VDD_I=3.3V±5%, over settings in Table 4	-12		+12	
Output Impedance	z_{OH}	$\Delta V_O/\Delta I_O$, where V_{O1} = 1.0V, $V_{O2} = V_{SS}$, R_{IREF} = 475Ω, $I_{OH} = 6 \times I_{REF}$	3000			Ω
Tristate Output Current	I_{OZ}		-10		10	µA

Table 9: MCLK_P, MCLK_N Clock Outputs

Voltage (V)	High Drive Current (mA)			Voltage (V)	Low Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-49	-83	-132
0.2	11	17	24	0.2	-48	-83	-131
0.4	21	32	45	0.4	-48	-82	-130
0.6	30	45	64	0.6	-47	-81	-129
0.8	37	56	79	0.8	-47	-80	-127
1.0	43	65	92	1.0	-46	-79	-126
1.2	47	73	103	1.2	-46	-78	-124
1.4	50	78	112	1.4	-45	-76	-121
1.6	53	82	117	1.6	-43	-74	-117
1.8	54	84	120	1.8	-41	-70	-112
2.0	55	85	121	2.0	-37	-65	-105
2.2	55	85	122	2.2	-33	-59	-97
2.4	55	86	123	2.4	-28	-52	-87
2.6	56	86	123	2.6	-22	-43	-74
2.8	56	86	124	2.8	-14	-32	-60
3.0	56	87	124	3.0	-6	-20	-45
3.2		87	124	3.2		-7	-27
3.4			125	3.4			-7



Data in this table represents nominal characterization data only

Table 10: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Tristate Enable Delay *	t_{DZL}, t_{DZH}	SEL_A:B=00, SEL133/100#=0	1.0		10	ns
Tristate Disable Delay *	t_{DLZ}, t_{DHZ}	SEL_A:B=11, SEL133/100#=0	1.0		10	ns
Clock Stabilization (on power-up) *	t_{STB}	via PWR_DWN#			3.0	ms
HOST_P1:6, HOST_N1:6 Clock Outputs						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period at V_X, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}, R_S=33.2Ω, R_P=49.9Ω	45		55	%
Clock Skew *	$t_{sk(o)}$	HOST pair to HOST pair @ V_X, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}, R_S = 33.2Ω, R_P = 49.9Ω			100	ps
Jitter, Additive Period (peak-peak) *	$t_{j(\Delta P)}$	Rising edge to rising edge at V_X, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}, R_S = 33.2Ω, R_P = 49.9Ω			$t_{J(IN)}$+ 100	ps
Rise Time *	t_r	Rising edge to rising edge at V_X, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}, R_S = 33.2Ω, R_P = 49.9Ω	175		450	ps
Rise/Fall Time Matching*		Rising edge to rising edge at V_X, R_{IREF} = 475Ω, I_{OH} = 6× I_{REF}, R_S = 33.2Ω, R_P = 49.9Ω			20	%
MREF_P, MREF_N Clock Outputs						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.5V	45		55	%
Jitter, Additive Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to rising edge at 1.5V, C_L=30pF			$t_{J(IN)}$+ 100	ps
Rise Time *	$t_{r\ min}$	Measured @ 0.4V – 2.4V; C_L=10pF	0.4			ns
	$t_{r\ max}$	Measured @ 0.4V – 2.4V; C_L=30pF			1.6	
Fall Time *	$t_{f\ min}$	Measured @ 2.4V – 0.4V; C_L=10pF	0.4			ns
	$t_{f\ max}$	Measured @ 2.4V – 0.4V; C_L=30pF			1.6	

4.0 Package Information

Table 11: 48-pin SSOP (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.095	0.110	2.41	2.79
A_1	0.008	0.016	0.20	0.41
b	0.008	0.0135	0.20	0.34
c	0.005	0.010	0.13	0.25
D	0.620	0.630	15.75	16.00
E	0.395	0.420	10.03	10.67
E_1	0.291	0.299	7.39	7.59
e	0.025 BSC		0.64 BSC	
h	0.015	0.025	0.38	0.64
L	0.020	0.040	0.51	1.01
θ	0°	8°	0°	8°

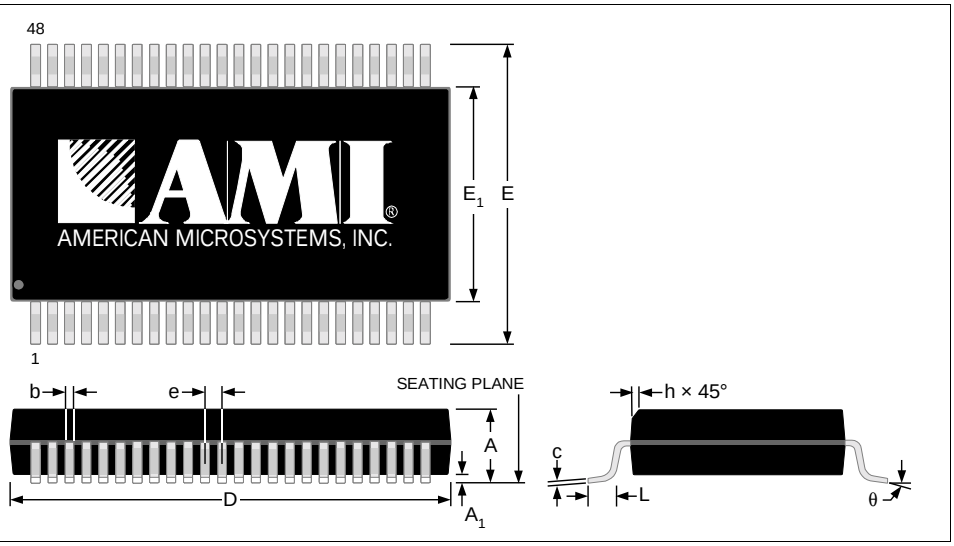


Table 12: 48-pin SSOP (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	93	°C/W
Lead Inductance, Self	L_{11}	Longest lead	5.5	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	3.0	nH
	L_{13}	Longest lead to any 2nd adjacent lead	2.1	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.94	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.46	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.05	

Table 13: 48-pin TSSOP (6.1mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A_1	0.002	0.006	0.05	0.15
b	0.0067	0.011	0.17	0.27
c	0.0035	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E	0.318 BSC		8.10 BSC	
E_1	0.236	0.244	6.00	6.20
e	0.019 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
S	0.008	-	0.20	-
θ_1	0°	8°	0°	8°
θ_2	12° REF		12° REF	
θ_3	12° REF		12° REF	

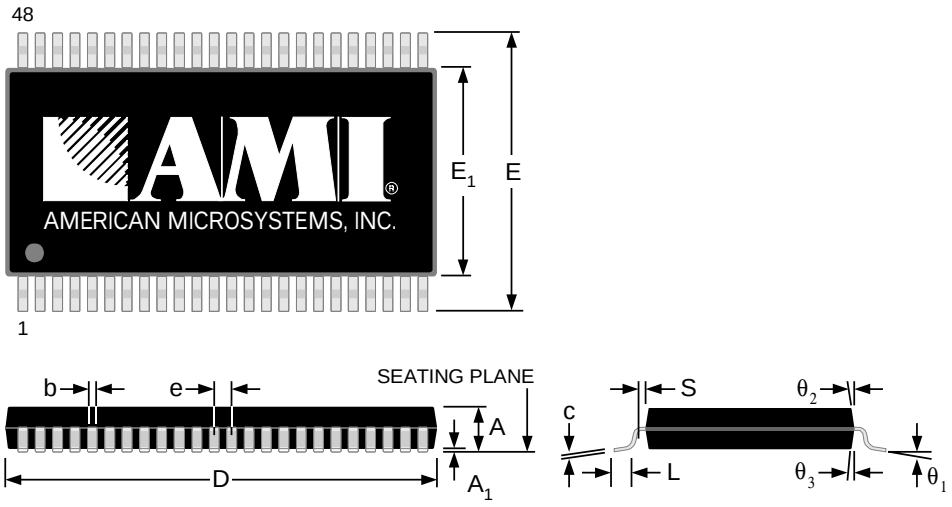


Table 14: 48-pin TSSOP (6.1mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	89	°C/W
Lead Inductance, Self	L_{11}	Longest lead	3.50	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	1.82	nH
	L_{13}	Longest lead to any 2nd adjacent lead	1.17	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.63	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.30	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.03	

5.0 Ordering Information

Table 15: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6058-01	11915-802	48-pin (0.300") SSOP	0° C to 70° C (Commercial)	Tape and Reel
	11915-202	48-pin (6.1mm) TSSOP	0° C to 70° C (Commercial)	Tape and Reel

6.0 Revision Information

DATE	PAGE	DESCRIPTION
8/4/00	-	This document contains information on a new product. Specifications and information herein are subject to change without notice.

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