OKI Semiconductor

PEDL9204-02
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ML9204-xx

Preliminary

5 × 7 Dot Character × 24-Digit × 2-Line Display Controller/Driver with Character RAM (Built-in Key Scan)

GENERAL DESCRIPTION

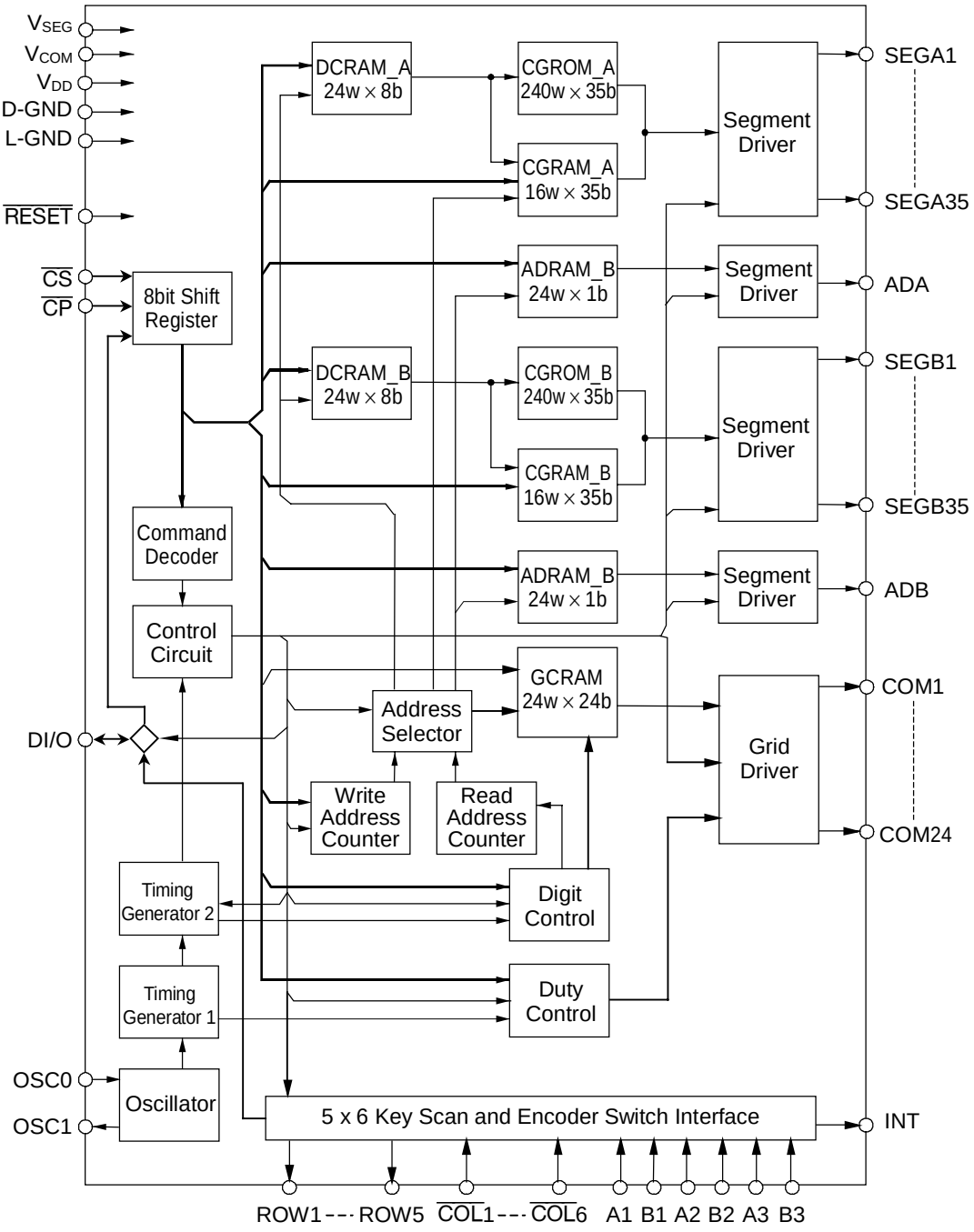
The ML9204-xx is a 5 × 7 dot matrix type vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols of a maximum of 24 digits × 2 lines.
Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller. A display system is easily realized by internal ROM and RAM for character display.
Built-in key scan for 3-channel encoder type rotary switch and 5 × 6 matrix key switch allow the user to receive each switch input.
The ML9204-xx has low power consumption since it is made by CMOS process technology.
–01 is available as a general-purpose code.
Custom codes are provided on customer's request.

FEATURES

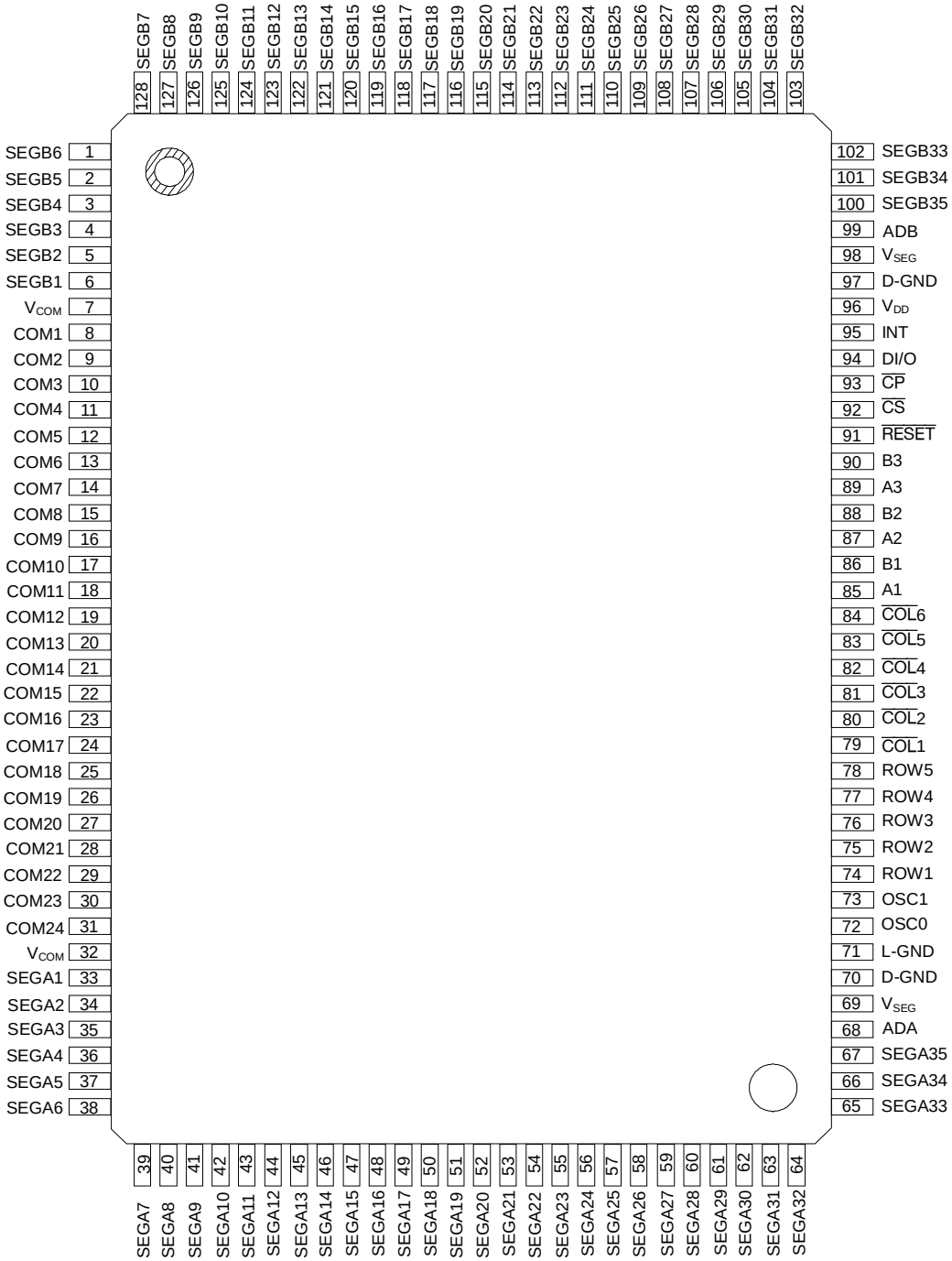
- Logic power supply (V_{DD}) : 3.3 V±10% or 5.0 V±10%
- VFD tube drive power supply (V_{SEG}, V_{COM}) : 20 to 60 V
- VFD driver output current
  (VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.)
  - Segment driver (SEGA1 to A35, SEGB1 to B35)
    Only one driver output is high : –5 mA (V_{SEG} = 60 V)
    All the driver outputs are high : –350 mA (V_{SEG} = 60 V)
  - Segment driver (ADA, ADB) : –15 mA (V_{SEG} = 60 V)
  - Grid driver (COM1 to 24) : –25 mA (V_{COM} = 60 V)
- Content of display
  SEGA1 to SEGA35 and ADA
  - CGROM_A : 5 × 7 dots 240 types (character data)
  - CGRAM_A : 5 × 7 dots 16 types (character data)
  - ADRAM_A : 24 (display digit)× 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_A : 24 (display digit) × 8 bits (register for character data display)

  SEGB1 to SEGB35 and ADB
  - CGROM_B : 5 × 7 dots 240 types (character data)
  - CGRAM_B : 5 × 7 dots 16 types (character data)
  - ADRAM_B : 24 (display digit)× 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_B : 24 (display digit) × 8 bits (register for character data display)
- Display control function
  - GCRAM : Simultaneous output of COM1 to 24 can be set in 1 grid.
  - Display digits : 1 to 24 digits (9- to 24-bit arbitrary setting)
  - Display duty (brightness adjustment) : 0/1024 to 960/1024 stages
  - All lights ON/OFF
- 5 interfaces with microcontroller:DI/O, $\overline{CS}$, $\overline{CP}$, $\overline{RESET}$, INT
- Built-in key scan circuit for 5 × 6 matrix key switch
- Built-in key scan circuit for 3-channel encoder type rotary switch
- Built-in oscillation circuit
  Crystal oscillation or ceramic oscillation: 4.0 MHz (Typ)
- Standby function
  Inhibiting the oscillator circuit provides low power consumption.
- Package options:
  128-pin plastic QFP (QFP128-P-1420-0.50-K) (ML9204-xxGA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Connects to	Description
33 to 67	SEGA1 to A35	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} < –5 mA
1 to 6 100 to 128	SEGB1 to B35			
8 to 31	COM1 to 24	O	VFD tube grid electrode	VFD tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} < –25 mA
68	ADA	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} < –15 mA
99	ADB			
96	V_{DD}	—	Power supply	V_{DD}-L-GND are power supplies for internal logic. V_{COM}-D-GND are power supplies for driving VFD tube grid. V_{COM}-D-GND are power supplies for driving VFD tube anode. Use the same power supply for L-GND and D-GND.
71	L-GND			
7,32	V_{COM}			
69,98	V_{SEG}			
70,97	D-GND			
94	DI/O	I/O	Micro controller	Serial data input-output (positive logic). Data is input and output to sift register synchronized with the rise of shift clock. When Inputting data input from the LSB.
93	$\overline{CP}$	I	Micro controller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
92	$\overline{CS}$	I	Micro controller	Chip select input. Serial data transfer is disabled when $\overline{CS}$ pin is “H” level.
95	INT	O	Micro controller	Output pin for interrupt signal to micro controller. When depression or release of key matrix switch is detected, key scanning starts and when 1 cycle is completed, this pin becomes high level. Upon receiving encoder type rotary switch input, this pin becomes high level. The INT pin remains at high level until the key scan stop mode is selected..
85,86 87,88 89,90	A1,B1 A2,B2 A3,B3	I	Rotary switch	Encoder type rotary switch input pins. All inputs possess chattering absorption function of 256us period. Those inputs must be tied to ground when they are not used.
79 to 84	$\overline{COL}$1 to 6	I	Key matrix	Input pins for return signal from key matrix with built-in pull-up resister. When input is low level, the key matrix switch is regarded as being pressed. Dose not have chattering absorption function.

<table>
<tr><td>74 to 78</td><td>ROW1 to 5</td><td>O</td><td>Key matrix</td><td>Key matrix scan signal output pins.
Normally low level is output.
Key scanning starts by detecting depression or release of key matrix switch and continues until selection of key scan stop mode.
When key scan stop mode is selected, all outputs of ROW1 to 5 return to low level.</td></tr>
<tr><td>91</td><td>$\overline{\text{RESET}}$</td><td>I</td><td>Micro controller</td><td>Reset input.
“Low” initializes all the functions.
Initial status is as follows.
• Address of each RAM ..... address “00”H
• Data of each RAM ..... Content is undefined
• Display digit..... 24 digits
• Brightness adjustment 0/1024
• All lights ON or OFF ..... OFF mode
• ROW1 to 5 ..... becomes low level
• INT ..... becomes low level</td></tr>
<tr><td>72</td><td>OSC0</td><td>I</td><td rowspan="2">Crystal or ceramic resonator</td><td rowspan="2">Pins for self-oscillation.
(Do not apply external clocks to these pins.)
Connect these pins to the crystal and capacitors or to the ceramic resonator and capacitors.
The target oscillation frequency is 4.0MHz.
(The device has an internal feedback resister.)
<table><tr><td>V_{DD}</td><td>Typical</td></tr><tr><td>3.3V</td><td>1Mohm</td></tr><tr><td>5.0V</td><td>0.4Mohm</td></tr></table>* For information regarding the oscillator contact the manufacturer of the oscillator.
* As regards the circuit, refer to the Application Circuit.</td></tr>
<tr><td>73</td><td>OSC1</td><td>O</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	—	–0.3 to +6.5	V
Supply Voltage (2)	V_{SEG}	—	–0.3 to +70	V
	V_{COM}	—	–0.3 to +70	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta ≤ 85°C	470 *1)	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C
Output Current	I_{O1}	COM1 to COM24	–50 to +2.0	mA
	I_{O2}	ADA, ADB	–30 to +2.0	mA
	I_{O3}	SEGA1 to SEGA35, SEGB1 to SEGB35	–10 to +2.0	mA
	I_{O4}	ROW1 to 5 / INT	–2.0 to +2.0	mA

*1) When use two or more COM, be careful of the following things.
The junction temperature which can be found by the following formula does not exceed 120.
Tj = (Px 85°C /W)+Ta (P is the maximum power consumption of IC.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	When the power supply voltage is 5.0 V (typ.)	4.5	5.0	5.5	V
		When the power supply voltage is 3.3 V (typ.)	3.0	3.3	3.6	V
Supply Voltage (2)	V_{SEG}	—	20	—	60	V
	V_{COM}	—	20	—	60	V
Operating Frequency	f_{OSC}	Oscillation	3.5	4.0	4.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 24, oscillation	142	163	183	Hz
Operating Temperature	T_{OP}	—	–40	—	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 5.0 V±10%)

(V_{DD} = 5.0 V±10%, V_{SEG} and V_{COM} = 20 to 60 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1	V_{DD} = 5.0 V±10%		0.7 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	*1	V_{DD} = 5.0 V±10%		—	0.3 V_{DD}	V
High Level Input Current	I_{IH}	*1	V_{IH} = V_{DD}		–1.0	+1.0	µA
Low Level Input Current	I_{IL1}	*2	V_{IL} = 0.0 V		–1.0	+1.0	µA
	I_{IL2}	COL1 to 6	V_{DD} = 5.0 V±10%, V_{IL} = 0.0 V		–450	–100	µA
High Level Output Voltage	V_{OH1}	COM1 to 24	V_{COM} = 60 V, I_{OH1} = –25 mA		V_{COM} – 2.0	—	V
	V_{OH2}	ADA, ADB	V_{SEG} = 60 V, I_{OH2} = –15 mA		V_{SEG} – 2.0	—	V
	V_{OH3}	SEGA1 to A35 SEGB1 to B35	V_{SEG} = 60 V, I_{OH3} = –5 mA		V_{SEG} – 2.0	—	V
	V_{OH4}	INT, ROW1 to 5	V_{DD} = 5.0 V±10%, I_{OH4} = –450 µA		V_{DD} – 0.2	—	V
Low Level Output Voltage	V_{OL1}	*3	—		—	1.0	V
	V_{OL2}	INT, ROW1 to 5	V_{DD} =5.0 V±10%, I_{OL2} = 450 µA		—	0.2	V
Supply Current (1)	I_{DD1}	V_{DD}	V_{DD} = 5.0 V±10%, f_{OSC} = 4.0 MHz		—	6.0	mA
	I_{DISP1}	V_{SEG}, V_{COM}	f_{OSC} = 4.0 MHz, no load	All output lights ON	—	1.0	mA
	I_{DISP2}			All output lights OFF	—	200	µA
Supply Current (2)	I_{DDS}	V_{DD}	In standby mode		—	1.0	µA
	I_{DISPS}	V_{SEG}, V_{COM}			—	20.0	µA

*1) $\overline{CS}$, $\overline{CP}$, DI/O, $\overline{RESET}$, $\overline{COL}$1 to 6
*2) $\overline{CS}$, $\overline{CP}$, DI/O, $\overline{RESET}$
*3) SEGA1 to A35, SEGB1 to B35, ADA, ADB, COM1 to 24

DC Characteristics (V_{DD} = 3.3 V±10%)

(V_{DD} = 3.3 V±10%, V_{SEG} and V_{COM} = 20 to 60 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1	V_{DD} = 3.3 V±10%		0.8 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	*1	V_{DD} = 3.3 V±10%		—	0.2 V_{DD}	V
High Level Input Current	I_{IH}	*1	V_{IH} = V_{DD}		–1.0	+1.0	µA
Low Level Input Current	I_{IL1}	*2	V_{IL} = 0.0 V		–1.0	+1.0	µA
	I_{IL3}	COL1 to 6	V_{DD} = 3.3 V±10%, V_{IL} = 0.0 V		–120	–25	µA
High Level Output Voltage	V_{OH1}	COM1 to 24	V_{COM} = 60 V, I_{OH1} = –25 mA		V_{COM} – 2.0	—	V
	V_{OH2}	ADA, ADB	V_{SEG} = 60 V, I_{OH2} = –15 mA		V_{SEG} – 2.0	—	V
	V_{OH3}	SEGA1 to A35 SEGB1 to B35	V_{SEG} = 60 V, I_{OH3} = –5 mA		V_{SEG} – 2.0	—	V
	V_{OH5}	INT, ROW1 to 5	V_{DD} = 3.3 V±10%, I_{OH5} = –120 µA		V_{DD} – 0.2	—	V
Low Level Output Voltage	V_{OL1}	*3	—		—	1.0	V
	V_{OL2}	INT, ROW1 to 5	V_{DD} = 3.3 V±10%, I_{OL3} = 120 µA		—	0.2	V
Supply Current (1)	I_{DD2}	V_{DD}	V_{DD} = 3.3 V±10%, f_{OSC} = 4.0 MHz		—	4.0	mA
	I_{DISP1}	V_{SEG}, V_{COM}	f_{OSC} = 4.0 MHz, no load	All output lights ON	—	1.0	mA
	I_{DISP2}			All output lights OFF	—	200	µA
Supply Current (2)	I_{DDS}	V_{DD}	In standby mode		—	1.0	µA
	I_{DISPS}	V_{SEG}, V_{COM}			—	20.0	µA

*1) $\overline{CS}$, $\overline{CP}$, DI/O, $\overline{RESET}$, $\overline{COL}$1 to 6
*2) $\overline{CS}$, $\overline{CP}$, DI/O, $\overline{RESET}$
*3) SEGA1 to A35, SEGB1 to B35, ADA, ADB, COM1 to 24

AC Characteristics

(V_{DD} = 5.0 V±10%, or V_{DD} = 3.3 V±10%,V_{SEG} and V_{COM} = 20 to 60 V, Ta = –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		200	—	ns
D/A Setup Time	t_{DS}	—		200	—	ns
D/A Hold Time	t_{DH}	—		200	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		200	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	Oscillating state		8	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		200	—	ns
Data Processing Time	t_{DOFF}	Oscillating state		4	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		200	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		t_{OSCON}	—	
D/A Wait Time	t_{RSOFF}	—		200	—	ns
All Output Slew Rate	t_R	C_l = 100 pF	t_R = 20 to 80%	—	2.0	µs
	t_F		t_F = 80 to 20%	—	2.0	µs
OSC Duty Ratio	du_{OSC}	—		40	60	%
Oscillation Rise Time	t_{OSCON}	—		*1		

*1 t_{OSCON} (oscillation rise time) differs with the oscillator pin used.
As regards oscillation rise time, refer to the data of oscillator used.

Key Scan Characteristics

(V_{DD} = 5.0V±10%, or V_{DD} = 3.3V±10%, V_{SEG} and V_{COM} = 20 to 60 V, Ta = –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Key Scan Time	t_{SCAN}	f_{OSC} = 3.5 to 4.5 MHz	142.2	160	182.8	µs
Key Scan Pulse Width	t_{WSCAN}		28.4	32	36.6	µs

Rotary Switch Characteristics

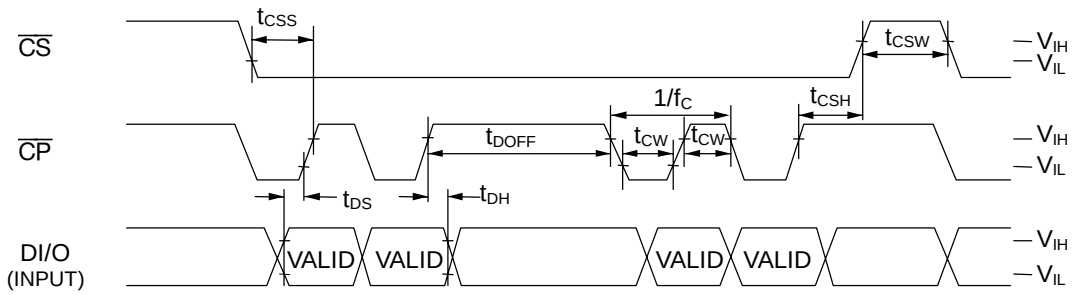
(V_{DD} = 5.0V±10%, or V_{DD} = 3.3V±10%, V_{SEG} and V_{COM} = 20 to 60 V, Ta = –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Phase Input Time	t_{ABW}	f_{OSC} = 3.5 to 4.5 MHz	1.2	—	—	ms
Phase Input Fixed Time	t_{ABH}					

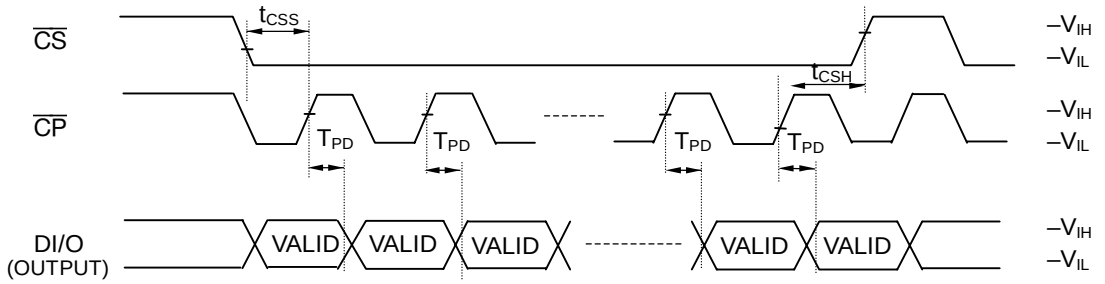
TIMING DIAGRAMS

Symbol	V_{DD} = 5.0 V ±10%	V_{DD} = 3.0 V ±10%
V_{IH}	0.7 V_{DD}	0.8 V_{DD}
V_{IL}	0.3 V_{DD}	0.2 V_{DD}

Data Input Timing

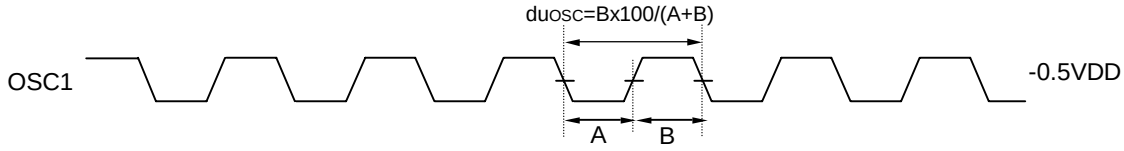


Data Output Timing

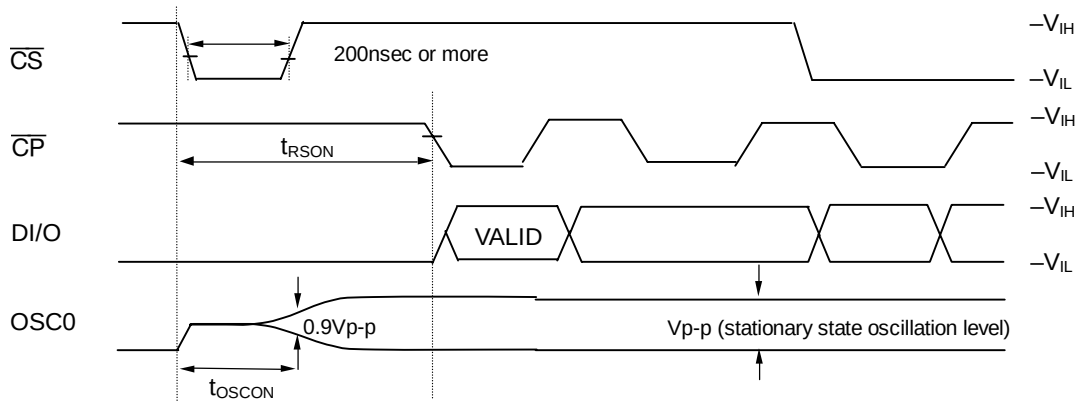


Output Timing

OSC Timing

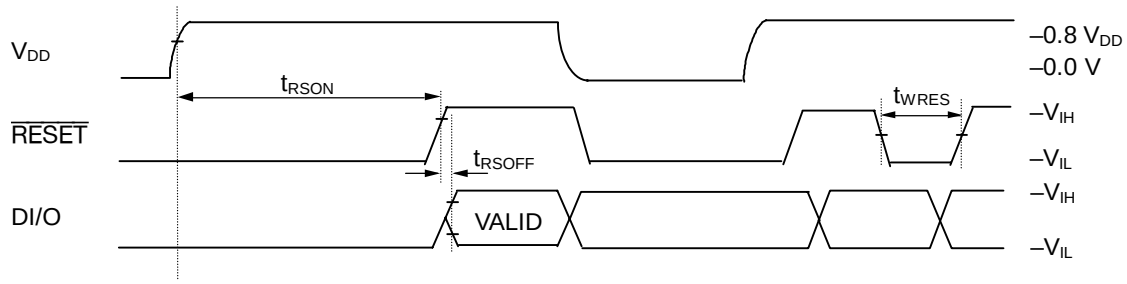


Standby Mode Release Timing

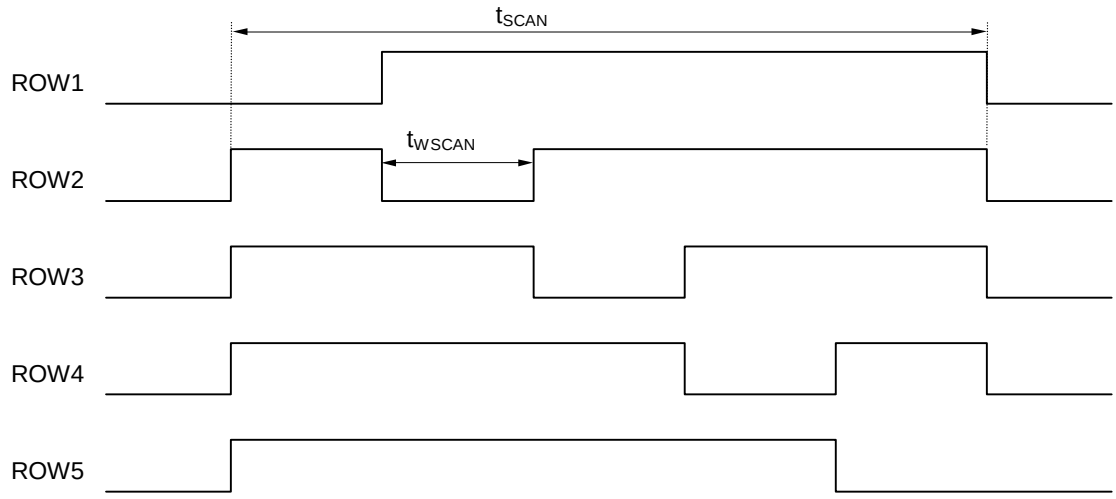


Reset Timing

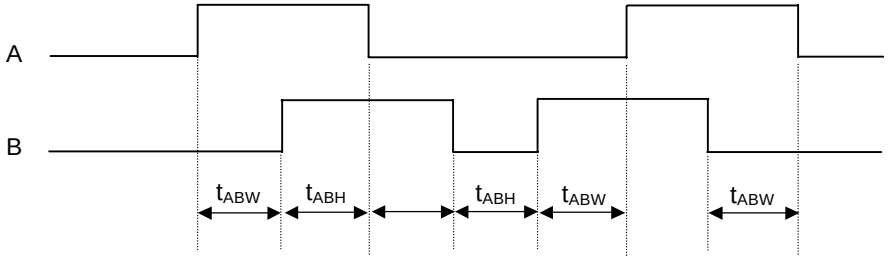
*** After a VDD injection should surely input a reset signal.**



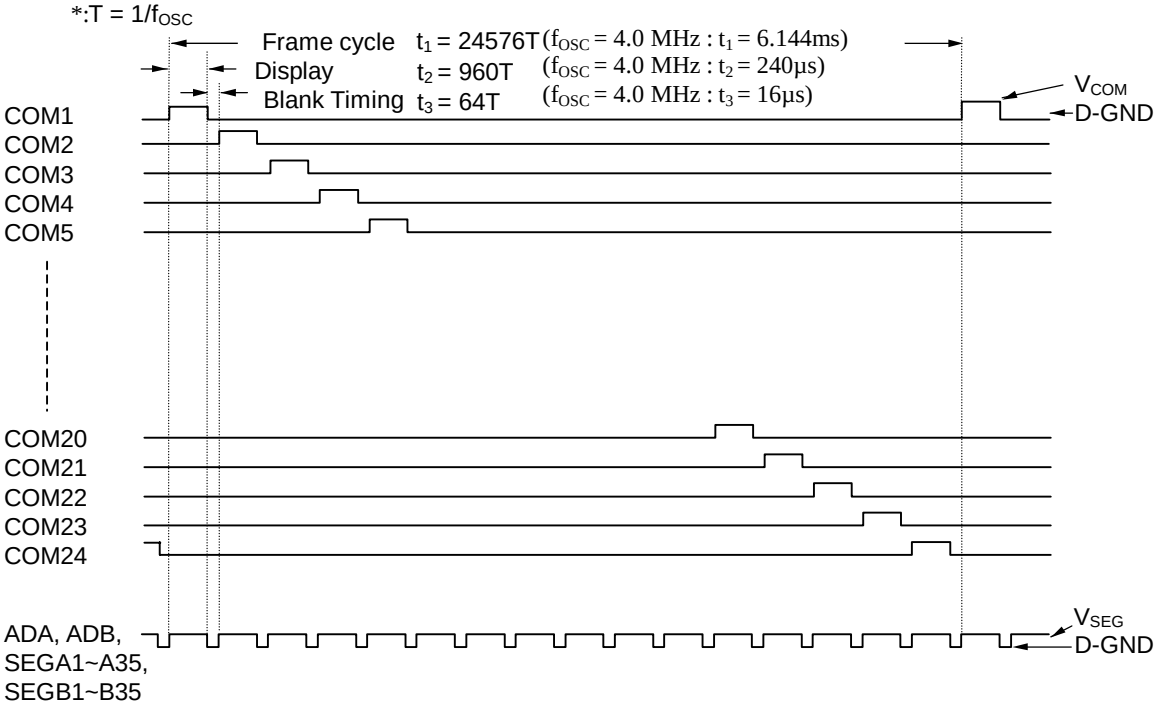
Key Scan Timing



Rotary Switch Input Timing



Digit Output Timing (24-Digit,960/1024-Duty)



FUNCTIONAL DESCRIPTION

Commands List

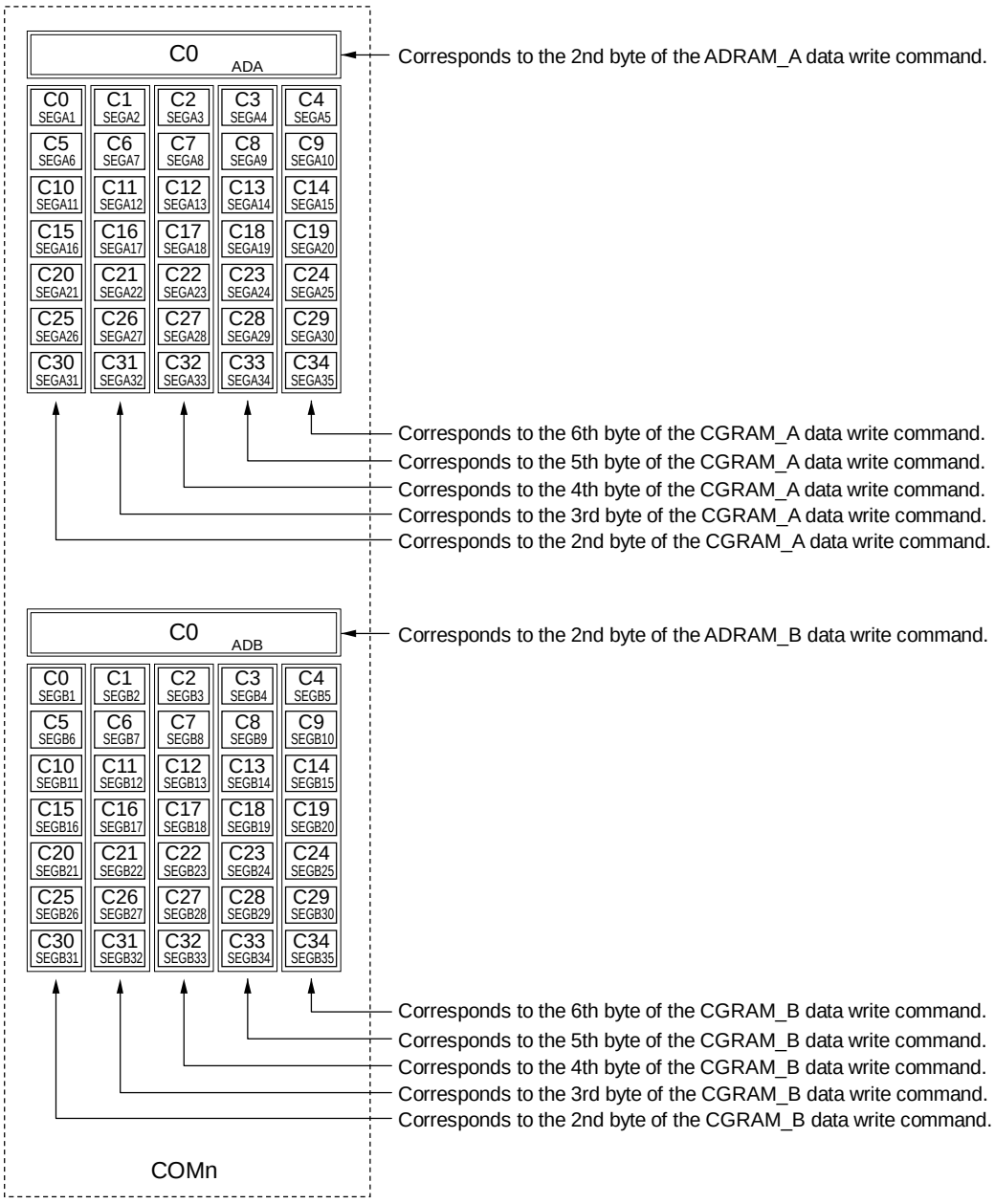
	Command	LSB MSB 1st byte								LSB MSB 2nd byte								
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM_A data write	*	*	*	*	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM_A data write	0	0	0	0	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
3	ADRAM_A data write	*	*	*	*	1	1	0	0	C0	*	*	*	*	*	*	*	
4	GCRAM data write	*	*	*	*	0	0	1	0	C0	C1	C2	C3	C4	C5	C6	C7	
										C8	C9	C10	C11	C12	C13	C14	C15	
										C16	C17	C18	C19	C20	C21	C22	C23	
5	Display duty set	D0	D1	*	*	1	0	1	0	D2	D3	D4	D5	D6	D7	D8	D9	
6	Number of digits set	K0	K1	K2	K3	0	1	1	0									
7	All lights ON/OFF	L	H	*	*	1	1	1	0									
9	DCRAM_B data write	*	*	*	*	1	0	0	1	C0	C1	C2	C3	C4	C5	C6	C7	
A	CGRAM_B data write	0	0	0	0	0	1	0	1	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
B	ADRAM_B data write	*	*	*	*	1	1	0	1	C0	*	*	*	*	*	*	*	
C	Key scan stop	*	*	*	*	0	0	1	1									
D	Key data output	*	*	*	*	1	0	1	1	Refer to item D of command and function description.								
F	Standby mode	*	*	*	*	1	1	1	1									
0	Test Mode(Note)					0	0	0	0									

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
Dn : Display duty specification
Kn : Number of digits specification
H : All lights ON instruction
L : All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM, and GCRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note: The test mode is used for inspection before shipment. It is not a user function. The user cannot use this command. Enter commands 1 to 7, 9 to D, and F alone in the way described on the next page and the following pages. (The operation of this device cannot be guaranteed if other commands are used.

Positional Relationship Between SEGn and ADn (one digit)

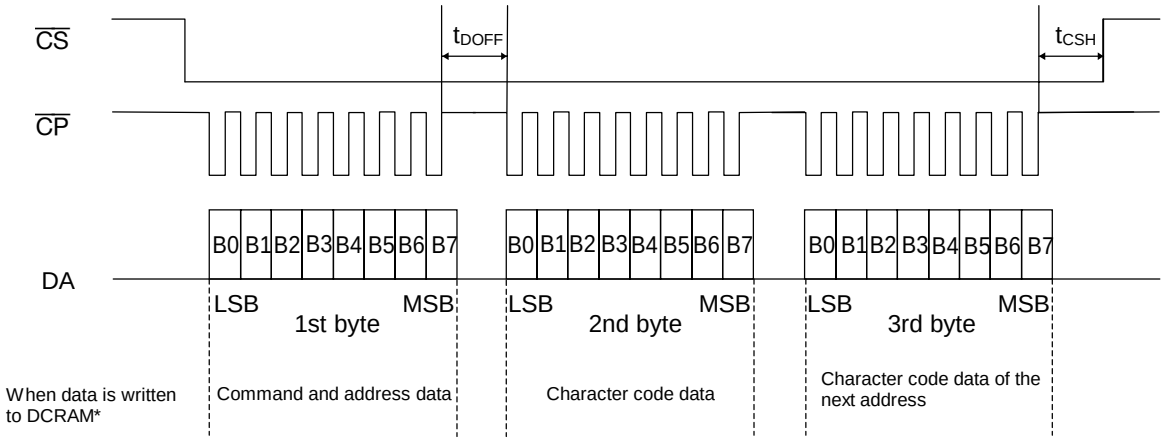


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DI/O pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.

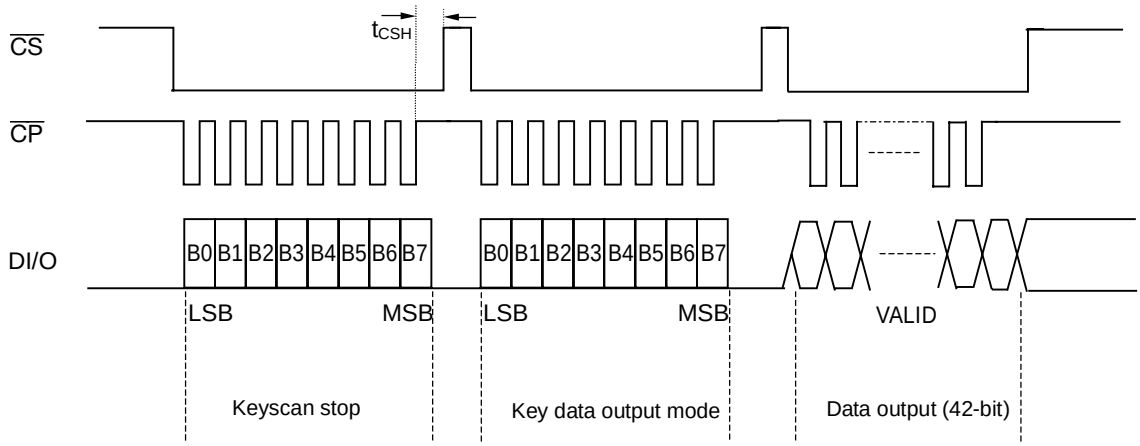


* When data is written to RAM (DCRAM, ADRAM, CGRAM, GCRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Data Outputting and Command Writing

In an operation to read key scan data, when $\overline{CS}$ goes "Low" after Key Data Output Mode is entered, the DI/O pin changes modes to OUTPUT and key data is output in synchronization with the rise of Shift Lock.

The waveforms to read key data are shown blow.
The DI/O pin enters the INPUT mode when the $\overline{CS}$ pin is set to "High" after key data is output.



Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example) and initializes all functions.
Initial status is as follows.

- Address of each RAM..... address "00"H
- Data of each RAM..... All contents are undefined
- Display digit..... 24 digits
- Brightness adjustment..... 0/1024
- All display lights ON or OFF..... OFF mode
- Segment output..... All segment outputs go "Low"
- AD output..... All AD outputs go "Low"
- ROW1 to 5..... All ROW outputs go "Low"
- INT..... INT goes "Low."

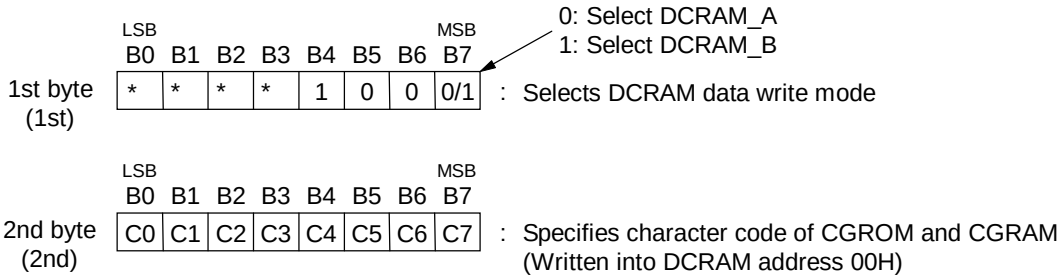
Be sure to execute the reset operation when turning power on and set again according to "Setting Flowchart" after reset.

Description of Commands and Functions

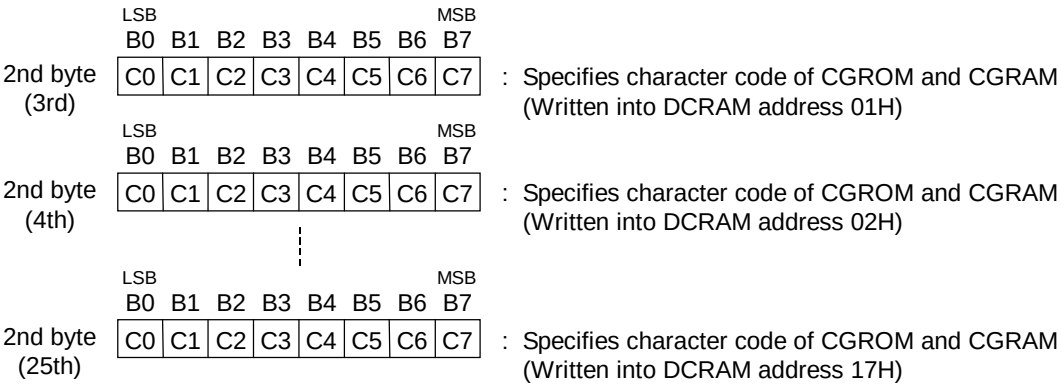
1,9. DCRAM data write
(Writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 5-bit address to store character code of CGROM and CGRAM.
The character code specified by DCRAM is converted to a 5 × 7 dot matrix character pattern via CGROM or CGRAM.
(The DCRAM can store 24 characters.)

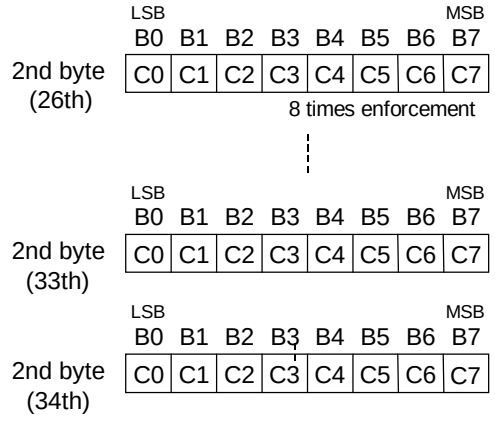
[Command format]



To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.



A character code setup of CGROM to 24-Digit and CGRAM is completion in the above work.
Furthermore, you have to specify the character codes of a dummy to be DCRAM and 18H-1FH to perform a character code setup from DCRAM address 00H continuously.
(In order to carry out the increment of the address of DCRAM automatically and to set a DCRAM address to 00H.)



: CGROM of a dummy and the character code of CGRAM are specified.
(It is not written in a DCRAM address.)

: CGROM of a dummy and the character code of CGRAM are specified.
(It is not written in a DCRAM address.)

: Character code of CGROM and CGRAM is specified.
(DCRAM address 00H are rewritten.)

C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 characters)
* : Don't Care

[COM positions and set DCRAM addresses]

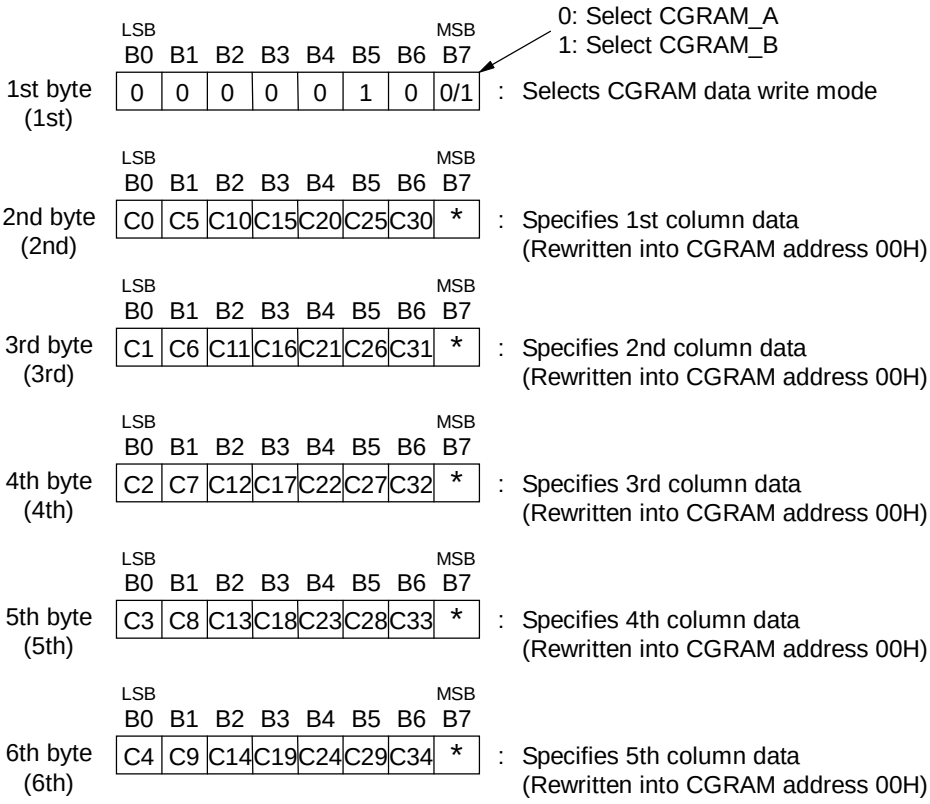
DCRAM address (HEX)	COM	DCRAM address (HEX)	COM	DCRAM address (HEX)	COM
00	COM1	0C	COM13	18	Dummy
01	COM2	0D	COM14	19	Dummy
02	COM3	0E	COM15	1A	Dummy
03	COM4	0F	COM16	1B	Dummy
04	COM5	10	COM17	1C	Dummy
05	COM6	11	COM18	1D	Dummy
06	COM7	12	COM19	1E	Dummy
07	COM8	13	COM20	1F	Dummy
08	COM9	14	COM21		
09	COM10	15	COM22		
0A	COM11	16	COM23		
0B	COM12	17	COM24		

Dummy is put in to set up a DCRAM address from 00H continuously.

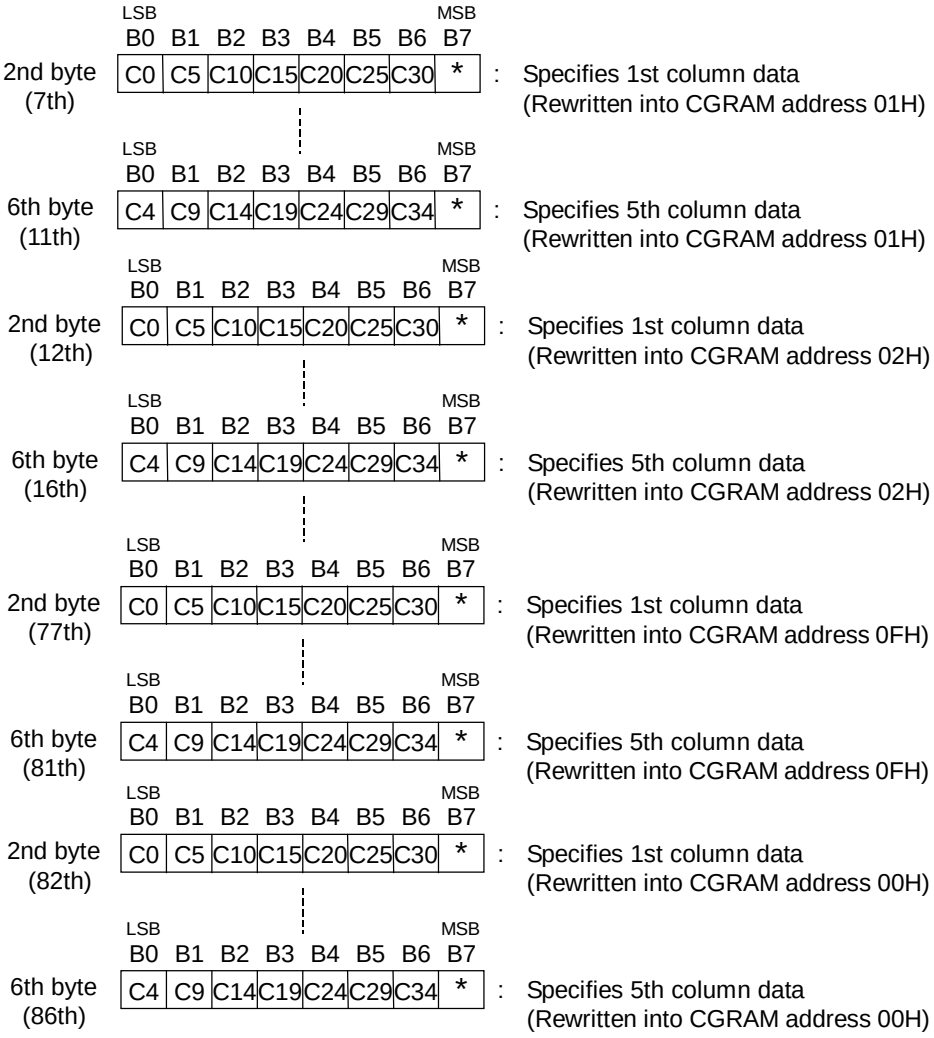
2,A. CGRAM data write
(CGRAM writes character pattern data.)

CGRAM (Character Generator RAM) has a 4-bit address to store 5x 7 dot matrix character patterns.
A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCROM.
The address of CGRAM is assigned to 00H to 0FH. (All the other addresses are the CGROM addresses.)
(The CGRAM can store 16 types of character patterns.)

[Command format]



To specify character pattern data continuously to the next address, specify only character pattern data as follows.
The addresses of CGRAM are automatically incremented. Specification of an address is unnecessary.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 200 ns is sufficient for t_{DOFF} time between bytes.



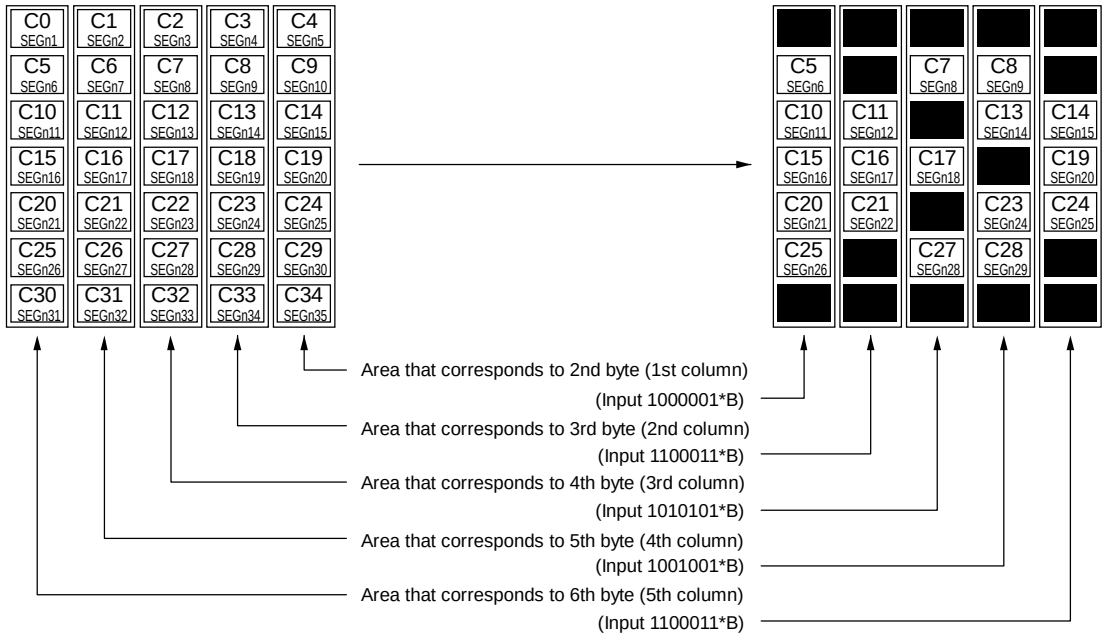
X0 (LSB) to X3 (MSB) : CGRAM addresses (4 bits: 16 characters)
C0 (LSB) to C34 (MSB) : Character pattern data (35 bits: 35 outputs per digit)
* : Don't care

[CGROM addresses and set CGRAM addresses]

Refer to ROM code tables.

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
00	0	0	0	0	RAM00 (00000000B)	08	0	0	0	1	RAM08 (00001000B)
01	1	0	0	0	RAM01 (00000001B)	09	1	0	0	1	RAM09 (00001001B)
02	0	1	0	0	RAM02 (00000010B)	0A	0	1	0	1	RAM0A (00001010B)
03	1	1	0	0	RAM03 (00000011B)	0B	1	1	0	1	RAM0B (00001011B)
04	0	0	1	0	RAM04 (00000100B)	0C	0	0	1	1	RAM0C (00001100B)
05	1	0	1	0	RAM05 (00000101B)	0D	1	0	1	1	RAM0D (00001101B)
06	0	1	1	0	RAM06 (00000110B)	0E	0	1	1	1	RAM0E (00001110B)
07	1	1	1	0	RAM07 (00000111B)	0F	1	1	1	1	RAM0F (00001111B)

Positional relationship between the output area of CGRAM

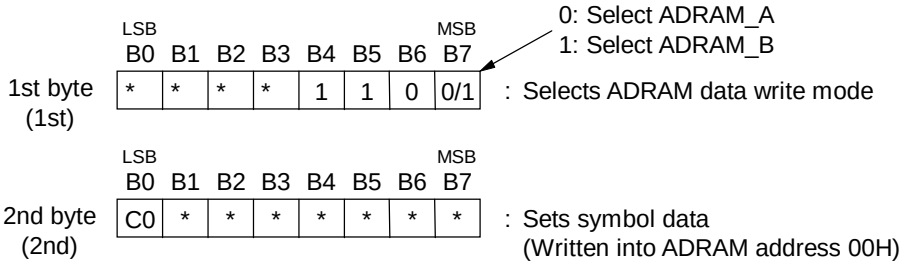


Note: CGROM_A and CGROM_B (Character Generator ROM A, B) have an 8-bit address to generate 5 x 7 dot matrix character patterns.
Each of CGROM_A and CGROM_B can store 240 types of character patterns.
The contents of CGROM_A and CGROM_B can be set separately.
General-purpose code -01 is available (see ROM code tables) and custom codes are provided on customer's request.

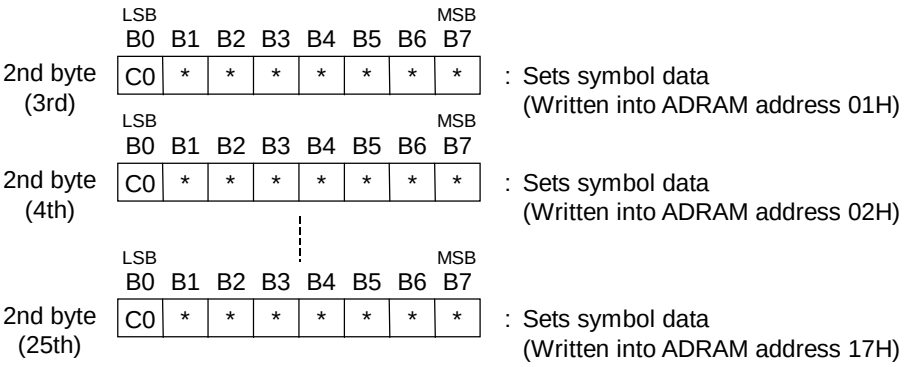
3,B. ADRAM data write
(ADRAM writes symbol data)

ADRAM (Additional Data RAM) has a 1-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store 1 type of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

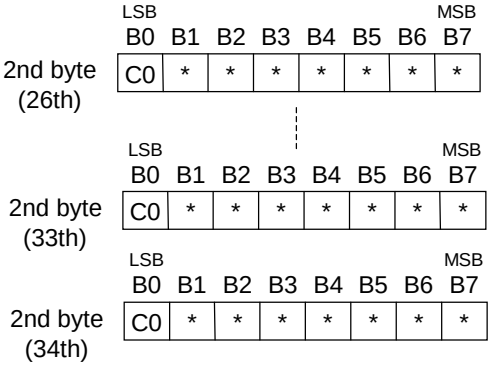
[Command format]



To specify symbol data continuously to the next address, specify only character data as follows.
The address of ADRAM is automatically incremented. Specification of addresses is unnecessary.



A character code setup of 24-Digit is completion in the above work.
Furthermore, you have to specify the character codes of a dummy to be ADRAM and 18H-1FH to perform a character code setup from ADRAM address 00H continuously.
(In order to carry out the increment of the address of ADRAM automatically and to set a ADRAM address to 00H.)



C0 : Symbol data (1 bit: 1-symbol data per digit)
* : Don't care

[COM positions and ADRAM addresses]

ADRAM address (HEX)	COM	ADRAM address (HEX)	COM	ADRAM address (HEX)	COM
00	COM1	0C	COM13	18	Dammy
01	COM2	0D	COM14	19	Dammy
02	COM3	0E	COM15	1A	Dammy
03	COM4	0F	COM16	1B	Dammy
04	COM5	10	COM17	1C	Dammy
05	COM6	11	COM18	1D	Dammy
06	COM7	12	COM19	1E	Dammy
07	COM8	13	COM20	1F	Dammy
08	COM9	14	COM21		
09	COM10	15	COM22		
0A	COM11	16	COM23		
0B	COM12	17	COM24		

Dummy is put in to set up a ADRAM address from 00H continuously.

4. GCRAM data write
(writes data by the number of COM outputs for digits)

GCRAM (Grid Control RAM) has a 5-bit address to control the number of COM outputs for digits.
GCRAM outputs specified data directly to COMn, allowing COM outputs to be controlled arbitrarily.
It is also possible to supply a large current by connecting a plurality of COMs outside the ML9204.
For example, when COM23 and COM24 are connected, the ML9204 has 23 display digits. In this case, the user specifies “23” as the number of display digits.
Write grid data at GCRAM addresses 00H and later.
Carry out this mode before putting-out-lights mode release.
Refer to a “setting operation flow chart” about the details of a setup.
Write COM data"0" in the GCRAM address which is not used for incorrect display prevention.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	*	*	*	*	0	0	1	0	:	Selects a GCRAM data write mode.
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	:	Specifies COM data. (Written into GCRAM address 00H)
3rd byte (3rd)	C8	C9	C10	C11	C12	C13	C14	C15	:	Specifies COM data. (Written into GCRAM address 00H)
4th byte (4th)	C16	C17	C18	C19	C20	C21	C22	C23	:	Specifies COM data. (Written into GCRAM address 00H)

C0 (LSB) to C23 (MSB): Grid control data (24 bits)
*: Don’t Care

Note: To specify additional grid control data, specify the grid control data as shown below. The GCRAM addresses are automatically incremented.
The second byte to the fourth byte (for grid data) are treated as a single piece of element and the byte-byte t_{DOFF} can be 200 ns.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
2nd byte (5th)	C0	C1	C2	C3	C4	C5	C6	C7	:	Specifies COM data. (Written into GCRAM address 01H)
4th byte (7th)	C16	C17	C18	C19	C20	C21	C22	C23	:	Specifies COM data. (Written into GCRAM address 01H)
2nd byte (71st)	C0	C1	C2	C3	C4	C5	C6	C7	:	Specifies COM data. (Written into GCRAM address 17H)
4th byte (73rd)	C16	C17	C18	C19	C20	C21	C22	C23	:	Specifies COM data. (Written into GCRAM address 17H)

With the above operations, COM data of up to 24 digits are set. To set other COM data at GCRAM addresses 00H and later, specify dummy symbol data at GCRAM addresses 18H to 1FH (to automatically increment the GCRAM address and set the GCRAM address to 00H).

[GCRAM addresses (digit positions) and COM positions]

GCRAM address (HEX)	1(00)	2(01)	3(02)	.....	22(15)	23(16)	24(17)
COM1	C0	C1	C2		C21	C22	C23
COM2	C0	C1	C2		C21	C22	C23
COM3	C0	C1	C2		C21	C22	C23
COM4	C0	C1	C2		C21	C22	C23
COM5	C0	C1	C2		C21	C22	C23
COM20	C0	C1	C2		C21	C22	C23
COM21	C0	C1	C2		C21	C22	C23
COM22	C0	C1	C2		C21	C22	C23
COM23	C0	C1	C2		C21	C22	C23
COM24	C0	C1	C2		C21	C22	C23

[GCRAM output example]

1. When 4-digit of the 9-digit display requires an output current of 40 mA

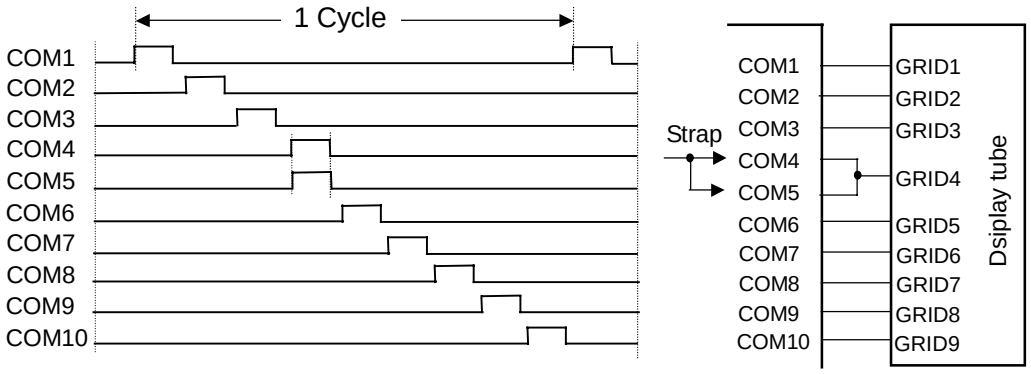
<Setup>

Number setup of display beams: 9-digit

GCRAM setup:4-digit of COM4 and COM5

* Write "0" also in the beam which is not used.

GCRAM address (HEX)	1(00)	2(01)	3(02)	4(03)	5(04)	6(05)	7(08)	8(07)	9(08)	11(09)	11(0A)	……	23(16)	24(17)
COM1	1	0	0	0	0	0	0	0	0	0	0		0	0
COM2	0	1	0	0	0	0	0	0	0	0	0		0	0
COM3	0	0	1	0	0	0	0	0	0	0	0		0	0
COM4	0	0	0	1	0	0	0	0	0	0	0	……	0	0
COM5	0	0	0	1	0	0	0	0	0	0	0		0	0
COM6	0	0	0	0	1	0	0	0	0	0	0		0	0
COM7	0	0	0	0	0	1	0	0	0	0	0		0	0
COM8	0	0	0	0	0	0	1	0	0	0	0		0	0
COM9	0	0	0	0	0	0	0	1	0	0	0		0	0
COM10	0	0	0	0	0	0	0	0	1	0	0		0	0



* Strapping COM4 and COM5 brings display digits to 9 digits, and a current of 50 mA can be supplied.

2. When only one digit of the 22-digit display requires an output current of 60 mA

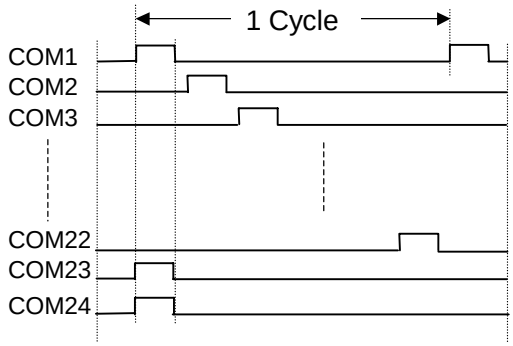
<Setup>

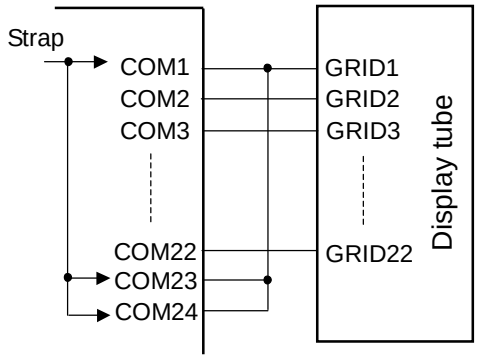
Number setup of display beams:22-digit

GCRAM setup:1-digit of COM1 and COM23 and COM24

* Write "0" also in the beam which is not used.

GCRAM address (HEX)	1(00)	2(01)	3(02)	4(03)	5(04)	6(05)	7(08)	8(07)	9(08)	11(09)	……	22(15)	23(16)	24(17)
COM1	1	0	0	0	0	0	0	0	0	0		0	0	0
COM2	0	1	0	0	0	0	0	0	0	0		0	0	0
COM3	0	0	1	0	0	0	0	0	0	0		0	0	0
⋮					⋮						……		⋮	
COM22	0	0	0	0	0	0	0	0	0	0		1	0	0
COM23	1	0	0	0	0	0	0	0	0	0		0	0	0
COM24	1	0	0	0	0	0	0	0	0	0		0	0	0





* Strapping COM1, COM23 and COM24 brings display digits to 22 digits, and a current of 75 mA can be supplied.

5. Display duty set
(writes display duty value to duty cycle register)

Display duty adjusts brightness in 1024 stages using 10-bit data.
When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	D0	D1	*	*	1	0	1	0	: Selects display duty set mode and sets duty value (lower 2 bits)
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (2nd)	D2	D3	D4	D5	D6	D7	D8	D9	: sets duty value (upper 8 bits)

D0 (LSB) to D9 (MSB) : Display duty data (10 bits: 1024 stages)
* : Don't care

[Relation between setup data and controlled COM duty]

HEX	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	COM duty
000	0	0	0	0	0	0	0	0	0	0	0/1024
001	1	0	0	0	0	0	0	0	0	0	1/1024
002	0	1	0	0	0	0	0	0	0	0	2/1024
⋮											⋮
3BE	0	1	1	1	1	1	0	1	1	1	958/1024
3BF	1	1	1	1	1	1	0	1	1	1	959/1024
3C0	0	0	0	0	0	0	1	1	1	1	960/1024
3C1	1	0	0	0	0	0	1	1	1	1	960/1024
⋮											⋮
3FF	1	1	1	1	1	1	1	1	1	1	960/1024

The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.

6. Number of digits set
(writes the number of display digits to the display digit register)

The number of digits set can display 9 to 24 digits using 4-bit data.
When power is turned on or when a $\overline{\text{RESET}}$ signal is input, the number of digit register value is "0". Always execute this instruction to change the number of digits before turning the display on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	0	1	1	0	: selects the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB) : Number of digit data (4 bits: 24 digits)
* : Don't care

[Relation between setup data and controlled COM]

* When the number of COM is one at 1 digit

HEX	K0	K1	K2	K3	Number of digits of COM	HEX	K0	K1	K2	K3	Number of digits of COM
0	0	0	0	0	1-24(COM1 to 24)	0	0	0	0	1	1-16(COM1 to 16)
1	1	0	0	0	1-9(COM1 to 9)	1	1	0	0	1	1-17(COM1 to 17)
2	0	1	0	0	1-10(COM1 to 10)	2	0	1	0	1	1-18(COM1 to 18)
3	1	1	0	0	1-11(COM1 to 11)	3	1	1	0	1	1-19(COM1 to 19)
4	0	0	1	0	1-12(COM1 to 12)	4	0	0	1	1	1-20(COM1 to 20)
5	1	0	1	0	1-13(COM1 to 13)	5	1	0	1	1	1-21(COM1 to 21)
6	0	1	1	0	1-14(COM1 to 14)	6	0	1	1	1	1-22(COM1 to 22)
7	1	1	1	0	1-15(COM1 to 15)	7	1	1	1	1	1-23(COM1 to 23)

→ The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.

7. All display lights ON/OFF set
(turns all display lights ON or OFF)

All display lights ON is used primarily for display testing.
All display lights OFF is primarily used for display blink and to prevent malfunction when power is turned on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	1	1	1	0	: Selects all display lights ON or OFF mode

L, H : Display operation data
* : Don't care

[Set data and display state of SEG and AD]

L	H	Display state of SEG and AD
0	0	Normal display
1	0	Sets all outputs to Low
0	1	Sets all outputs to High
1	1	Sets all outputs to High

* Priority is given to an all-points light command.

C. Key scan stop
This command stops key scanning and makes ROW1 to ROW5 outputs “Low” and the INT output “Low”.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	*	*	*	*	0	0	1	1	: stops key scanning.

*: Don’t Care

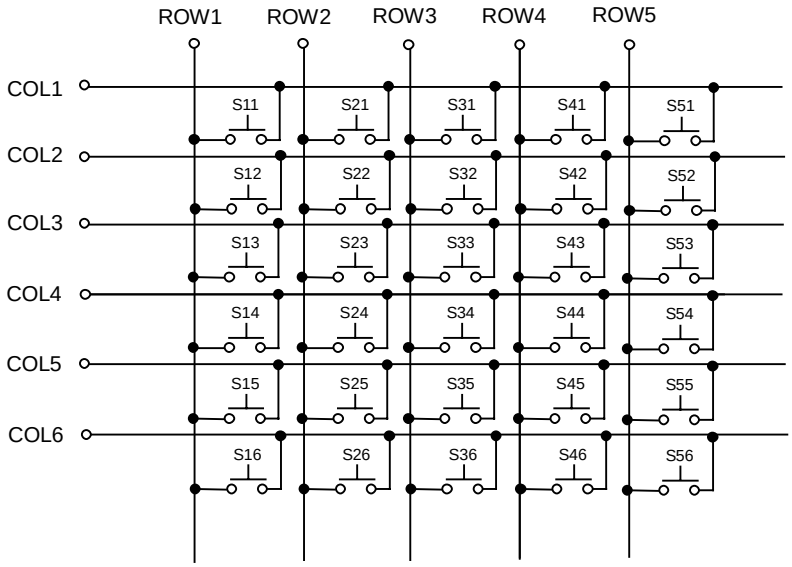
D. Key data output
This command puts the pin in the output mode and causes the pin to output the scanned switch data.
The DI/O pin outputs 42-bit switch data at the rise of a clock.
When the $\overline{CS}$ pin goes high, the DI/O pin enters the output mode.
“R1, R2, R3 = 0” means turning a control knob clockwise.
“R1, R2, R3 = 1” means turning a control knob counterclockwise.
Contact count bits are Q11(LSB) to Q13(MSB), Q21(LSB) to Q23(MSB), and Q31(LSB) to Q33(MSB).

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	*	*	*	*	1	0	1	1	: outputs key data.

*: Don’t Care

[COL input and ROW output key-switch matrix]



[Output Data Format]
Output data: 42 bits
5 × 6 push switch data: 30 bits
Encoder switch data: 12 bits

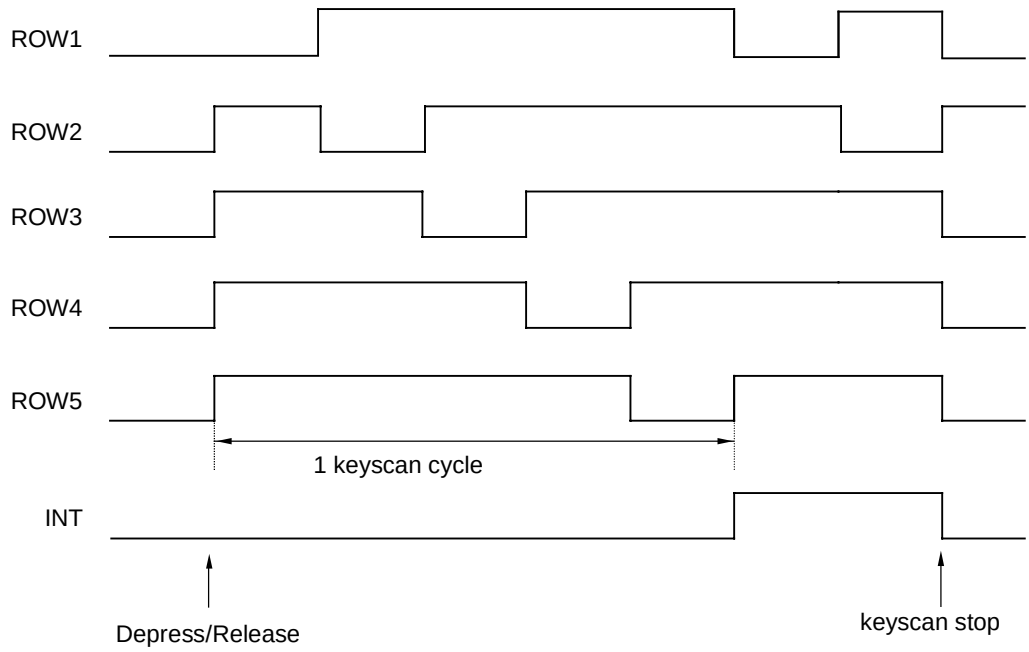
Bit	1	2	3	4	5	6	7	8	9	10	11	12
Output Data	S11	S12	S13	S14	S15	S16	S21	S22	S23	S24	S25	S26
Bit	13	14	15	16	17	18	19	20	21	22	23	24
Output Data	S31	S32	S33	S34	S35	S36	S41	S42	S43	S44	S45	S46
Bit	25	26	27	28	29	30	31	32	33	34	35	36
Output Data	S51	S52	S53	S54	S55	S56	R1	Q11	Q12	Q13	R2	Q21
Bit	37	38	39	40	41	42						
Output Data	Q22	Q23	R3	Q31	Q32	Q33						

Sij: i = ROW1 to 5; j = COL1 to 6
Sij = 1: switch ON
Sij = 0: switch OFF

Keyscan

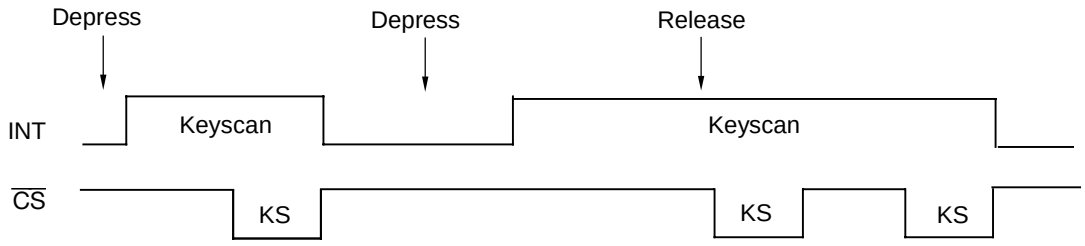
Keyscanning is started only when depression or release of any key is detected in order to minimize noise caused by scanning signal. Then, keyscanning is continued until the keyscan stop mode is sent from a microcomputer. The INT pin goes to the high level at the completion of 1-cycle scanning after the keyscan start, so the (high level) signal sent from the INT pin can be used as an interrupt signal.

[Keyscan Timing and Cycles]



Keyscanning cannot be stopped by selecting the keyscan stop mode only once if:
- keyscanning is started after depression or release of any key is detected, and then
- a key is depressed or released again before the keyscan stop mode is selected.

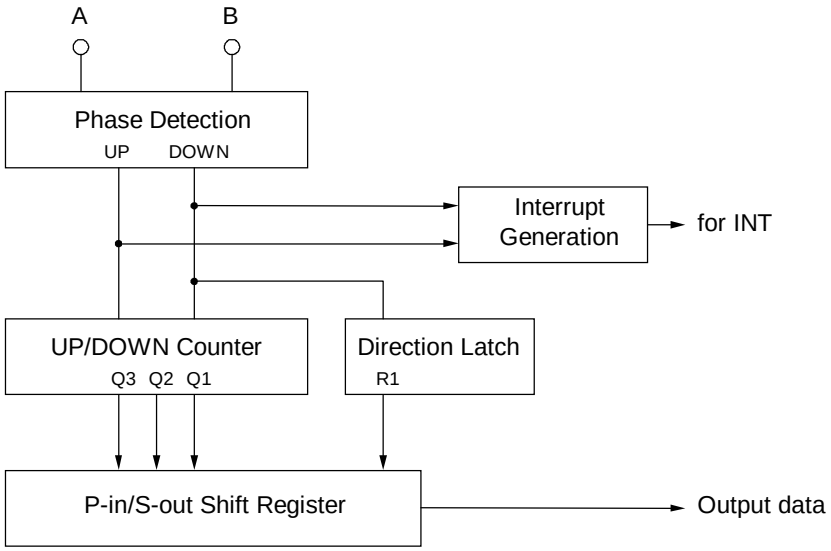
To stop keyscanning, it is required to select the keyscan stop mode once again.



KS: Keyscan stop mode

The rotary encoder switch function

As Figure 1 shows, the rotary encoder switch circuit is consisted of Phase detection, Interrupt generation, Up/down counter, Direction latch and Parallel-in serial-out shift register.

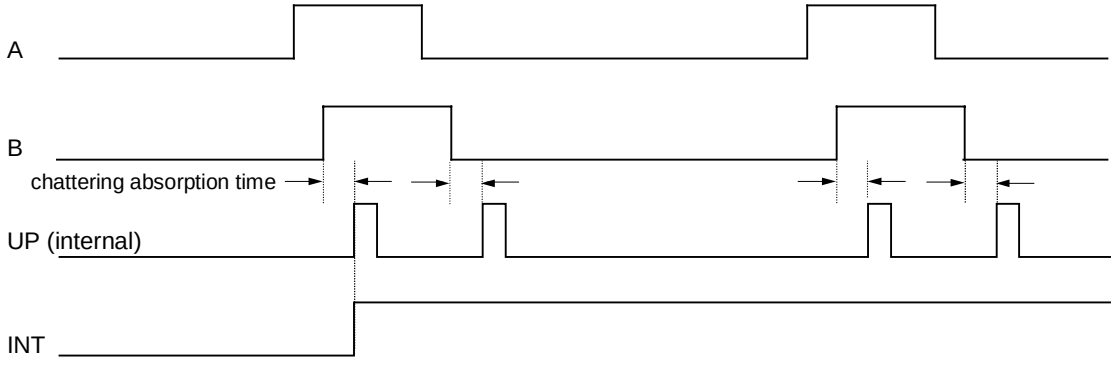


The Rotary Encoder Switch Circuit

1. Phase detection

1-1. Clockwise rotation

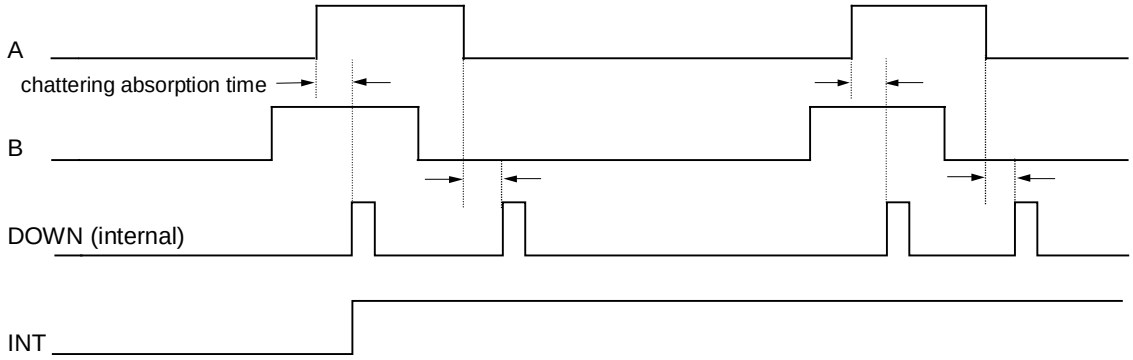
The input A and B have a chattering absorption circuit of 256 µs period. When signal A and B input as shown below, the phase detection circuit outputs UP signal after the chattering absorption period. At this time, the output INT also goes to high level, so this signal can be used as an interrupt. The INT stays High level until the keyscan stop mode is selected.



The Input and Output Timing in the Case of Clockwise Rotation

1-2. Counterclockwise rotation

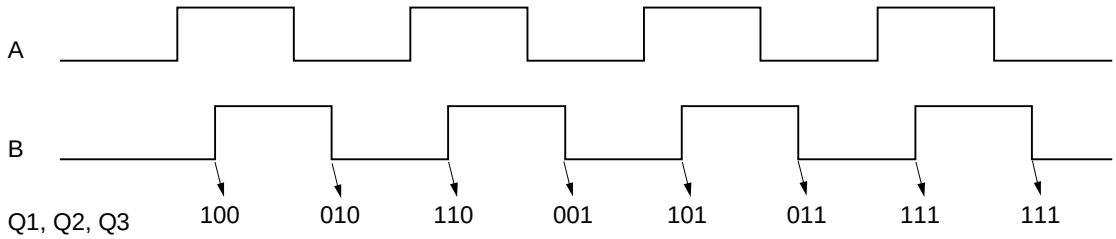
When signal A and B input as shown below, the phase detection circuit outputs Down signal after the chattering absorption period. At this time, the output INT also goes to High level. The INT stays High level until the keyscan stop mode is selected.



The Input and Output Timing in the Case of Counterclockwise Rotation

2. UP/DOWN COUNTER

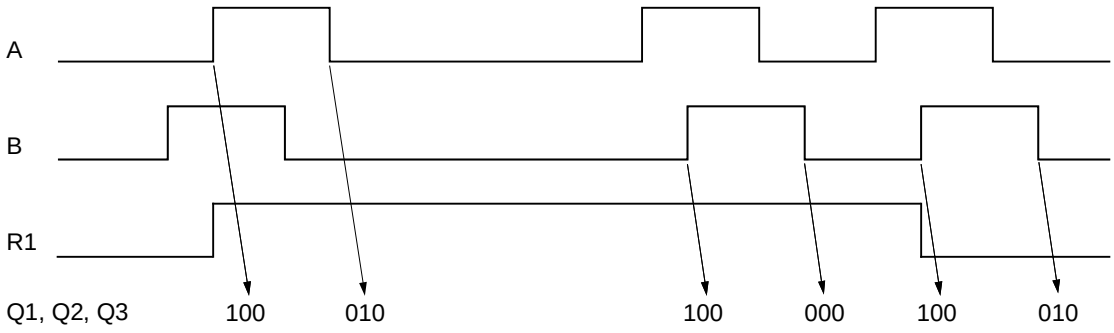
When the UP/DOWN COUNTER is input UP, it counts up and when it is input DOWN, it counts down. But if the UP/DOWN COUNTER is incremented beyond “111”, it stays “111”.



Counter Overflow

3. Direction latch

When the Direction latch is input DOWN the output R1 goes “1”. But if the UP pulse is input and the count value changes to a positive value, the output R1 goes to “0”.



Direction Latch

F. Standby mode set
(Display all switched off and an oscillation stopped)

Standby mode realizes low power consumption of VDD, VSEG, and VCOM by all switching off a display, stopping an oscillation of an external (COM is fixed to Low) oscillation child, and stopping internal operation completely. All display lights OFF is primarily used for display blink and to prevent malfunction when power is turned on.

* If a $\overline{\text{RESET}}$ signal is inputted during standby mode execution, standby mode is canceled, and keep in mind it that all states will be initialized.

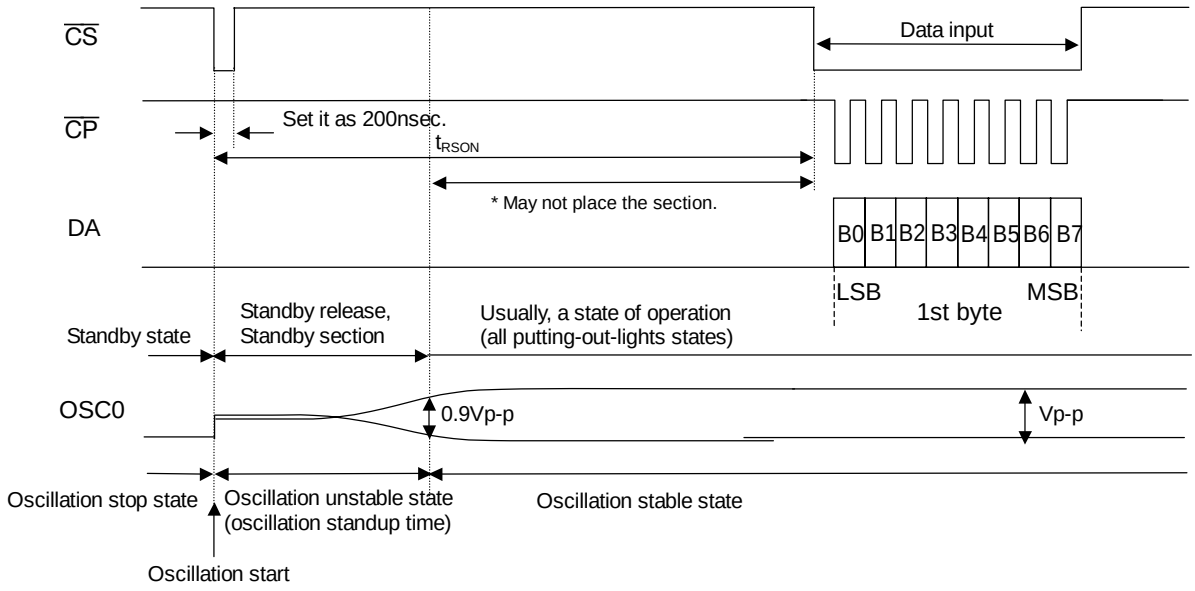
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	*	*	*	*	1	1	1	1	: Standby mode is specified.

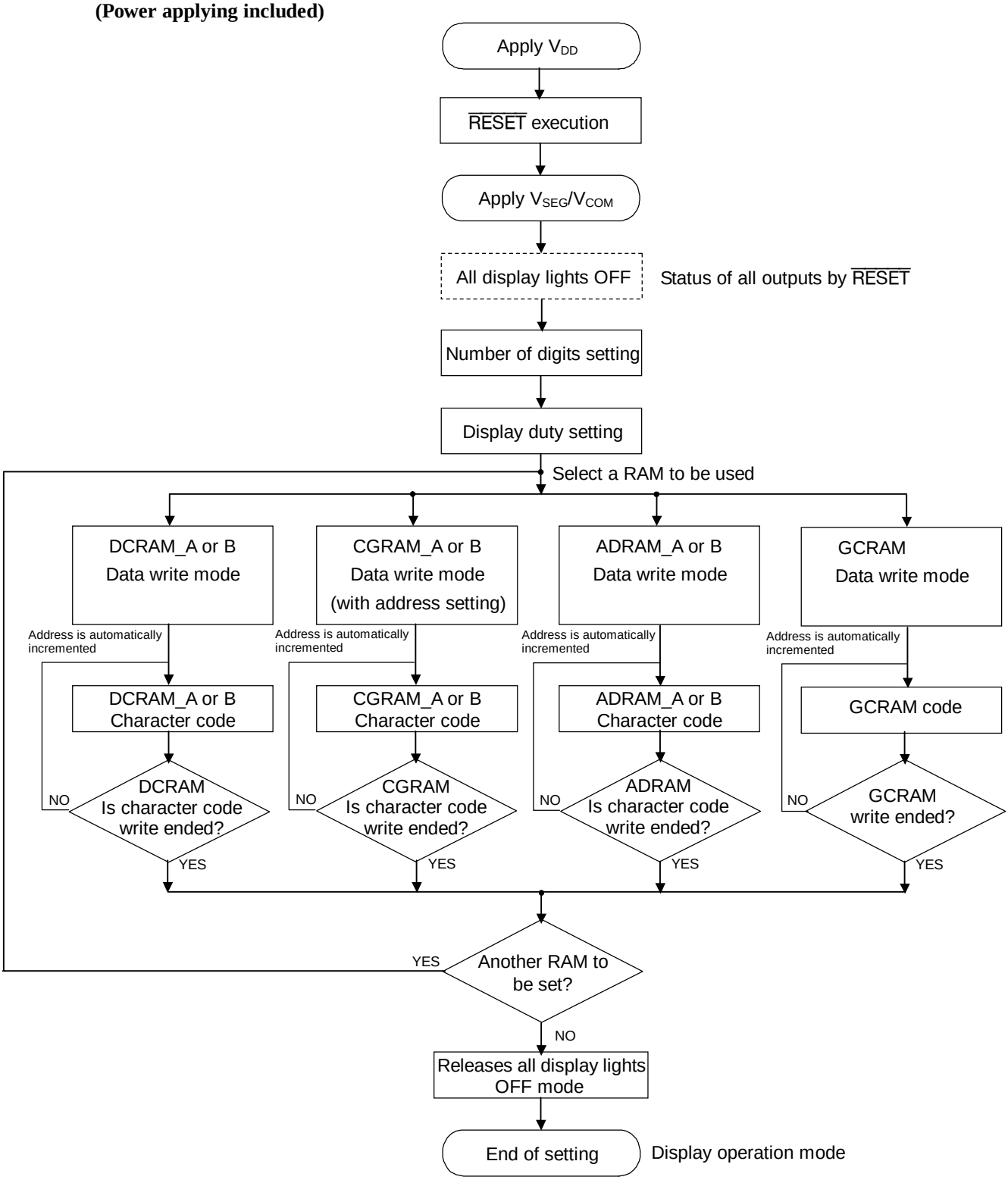
* : Don't care

[Release standby mode]
Release in standby mode is performed in falling of $\overline{\text{CS}}$. (An oscillation child's oscillation is started)
Data input will become possible if an oscillation is stabilized. (Please return brought-down $\overline{\text{CS}}$ high-level before data input)
When you display after standby mode release since it is all putting out lights although the setting state is held, please cancel all putting-out-lights modes (in usual mode).

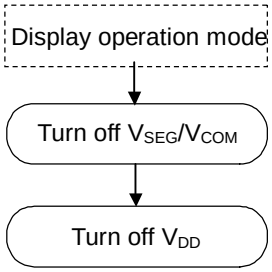
* Please do not input a shift clock into $\overline{\text{CP}}$ until an oscillation is stabilized. (Data will be given)
tRSON (oscillation standup time) changes with oscillation children who use it. Please make reference an oscillation child's data to be used.



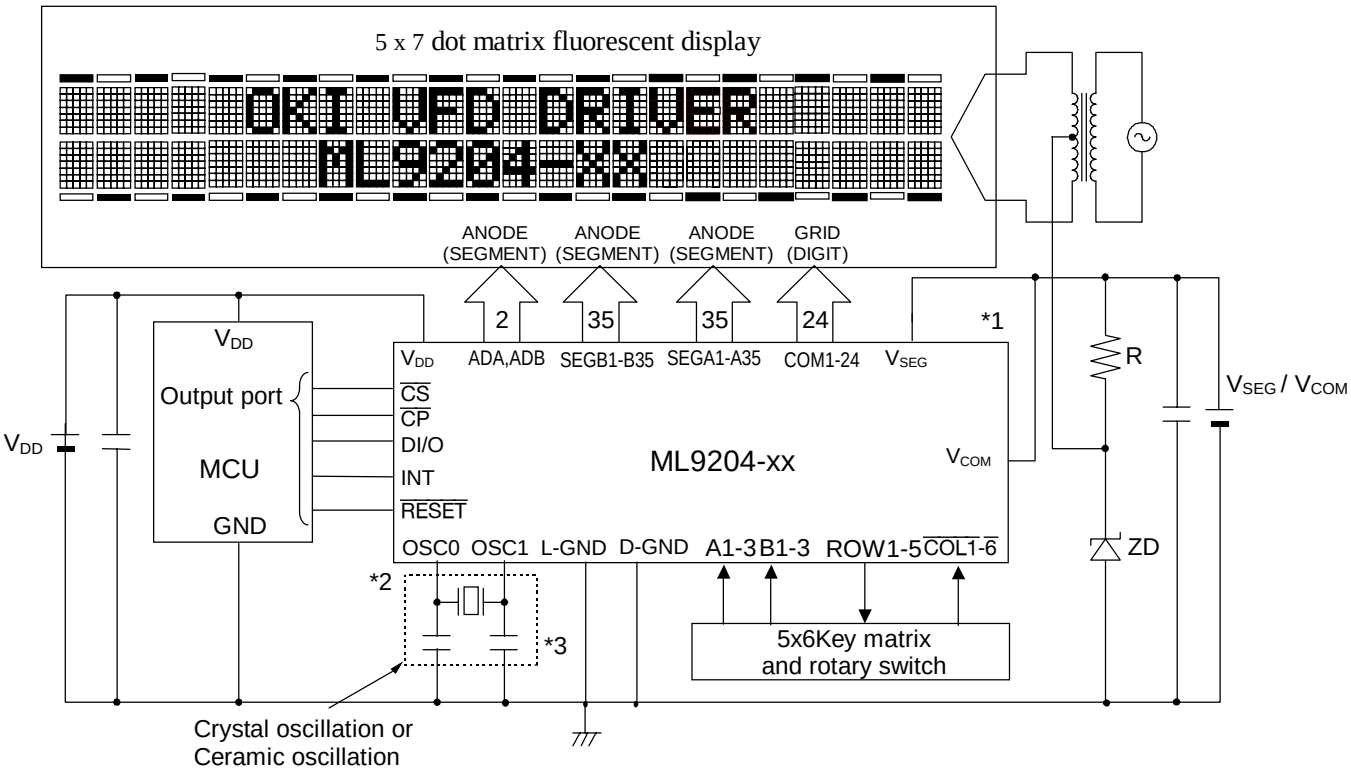
SETTING FLOWCHART
(Power applying included)



POWER-OFF FLOWCHART



APPLICATION CIRCUIT



*1 The V_{SEG} and V_{COM} voltages depend on the fluorescent display tube used. Adjust the value of the constants R and ZD to the V_{SEG} and V_{COM} voltages used.

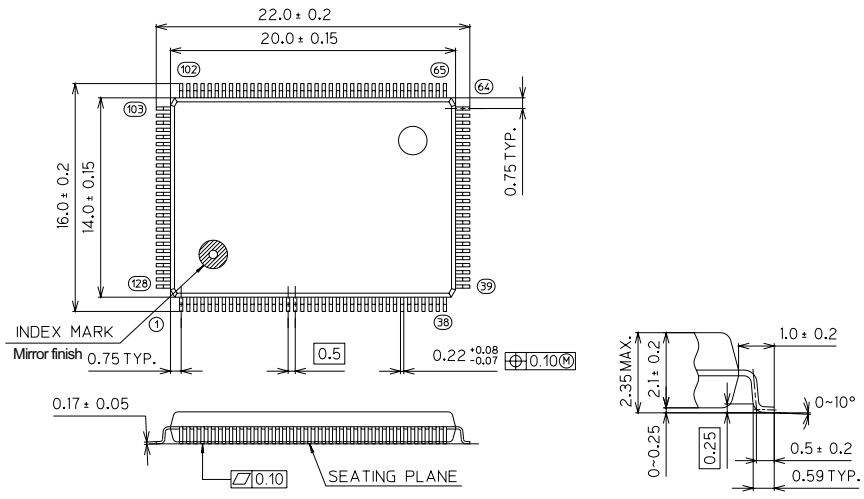
*2 The wiring trace between the OSC0 pin and the resonator should be kept as short as possible, and the GND traces should be provided along both sides of the wiring trace.

*3 Adjust the capacitance of the capacitor depending on the type of the oscillator used. (Refer to the data of oscillator used.)

PACKAGE DIMENSIONS

(Unit: mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.19 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9204-01	Jan. 8, 2003	–	–	Preliminary edition 1
PEDL9204-02	Oct. 12, 2004	4	4	Pin description added

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