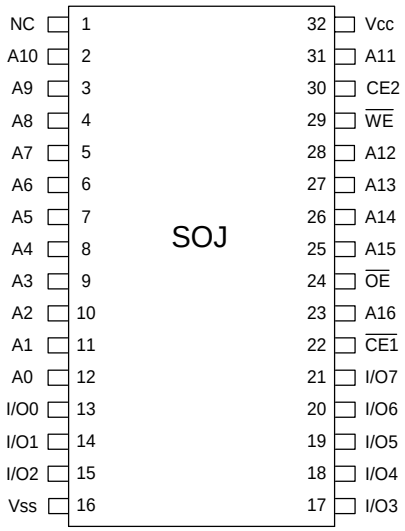
SRAM

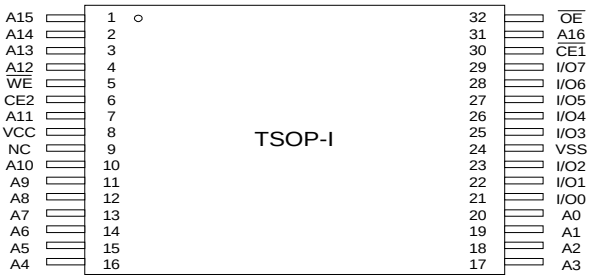
128K X 8 HIGH SPEED CMOS STATIC RAM

FEATURES

- Fast Address Access Times : 10/12/15ns
- Single 5V +10% power supply
- Low Power Consumption : 110/105/100mA
- TTL I/O compatible
- 2.0V data retention mode
- Automatic power-down when deselected
- Available packages :
  32-pin 300 mil SOJ & 32-pin TSOP-I
- Industry Standard Pin Assignment

PIN CONFIGURATION

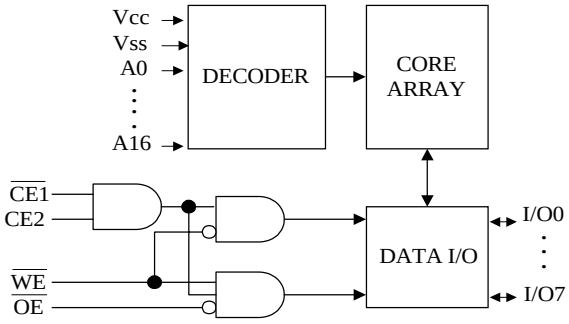




GENERAL DESCRIPTION

The T14M1024A is a one-megabit density, fast static random access memory organized as 131,072 words by 8 bits. It is designed for use in high performance memory applications such as main memory storage and high speed communication buffers. Fabricated using high performance CMOS technology, access times down to 10ns are achieved. Memory expansion by banking is easily accomplished using the chip enable pins $\overline{CE1}$ and CE2. This device is packaged in a standard 32-pin 300 mil SOJ and 32-pin TSOP-I.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CE1}$,CE2	Chip Select Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground

PART NUMBER EXAMPLES

	PACKAGE	SPEED
T14M1024A-10J	SOJ 300mil	10ns
T14M1024A-10P	TSOP-I 8x13.4mm	10ns
T14M1024A-10H	TSOP-I 8x20mm	10ns

DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM	RATING	UNIT
Power Supply Voltage	Vcc	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to Vcc+0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc+0.5	V
Operating Temperatrue	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I/O0- I/O7	Vcc
H	X	X	X	Not Selected	High-Z	$I_{SB,}I_{SB1}$
X	L	X	X	Not Selected	High-Z	$I_{SB,}I_{SB1}$
L	H	H	H	Output Disable	High-Z	Icc
L	H	L	H	Read	Data Out	Icc
L	H	X	L	Write	Data In	Icc

OPERATING CHARACTERISTICS

(Vcc = 5V ± 10%, Ta = 0 to 70°C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	MAX.	UNIT
Power Supply Voltage	Vcc			4.5	5.5	V
Input Low Voltage	V_{IL}			-0.5	0.8	V
Input High Voltage	V_{IH}			2.2	Vcc+0.5	V
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN} =Vss to Vcc		-	5	uA
Output Leakage Current	$\lvert I_{LO} \rvert$	V_{IN}=Vss to Vcc , $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-	5	uA
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} =-2.0 mA		2.4	-	V
Operating Power Supply Current	Icc	$\overline{CE1}$ = V_{IL} CE2 = V_{IH} ;f=max IO = 0mA	10ns	-	110	mA
			12ns	-	105	mA
			15ns	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1}$ = V_{IH}, CE2 = V_{IL}, IO = 0mA		-	25	mA
	I_{SB1}	Vcc = max; $\overline{CE1}$ ≥ Vcc-0.2V or CE2 ≤ Vss+0.2V; f=0mhz; IO = 0mA		-	5	mA

Note: Typical characteristics are at Vcc = 5V, Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	Typ-10%	5	Typ+10%	V
Input Voltage, low	V_{IL}	-0.3	-	0.8	V
Input Voltage, high	V_{IH}	2.2	-	Vcc+0.3	V
Ambient Temperature	T_A	0	-	70	°C

CAPACITANCE

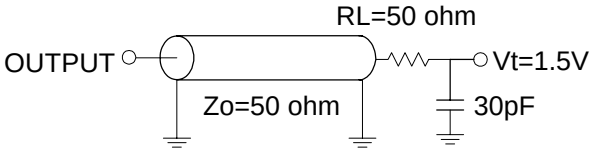
PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/ Output Capacitance	$C_{I/O}$	V_{OUT}= 0V	8	pF

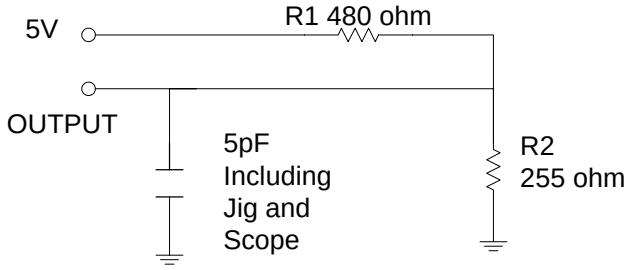
Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3.0 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L =30pF,I_{OH}/I_{OL} = -2mA/4mA

AC TEST LOADS AND WAVEFORM





(For TCLZ, TOLZ, TCHZ, TOHZ, TWHZ, TOW)

AC CHARACTERISTICS

(V_{CC}=5V ± 10%, Vss = 0V, Ta = 0 to 70°C)

(1) READ CYCLE

PARAMETER	SYM.	T14M1024A-10		T14M1024A-12		T14M1024A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACS}	-	10	-	12	-	15	ns
Output Enable to Output Valid	t_{AOE}	-	6	-	7	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

* These parameters are sampled but not 100% tested.

(2)WRITE CYCLE

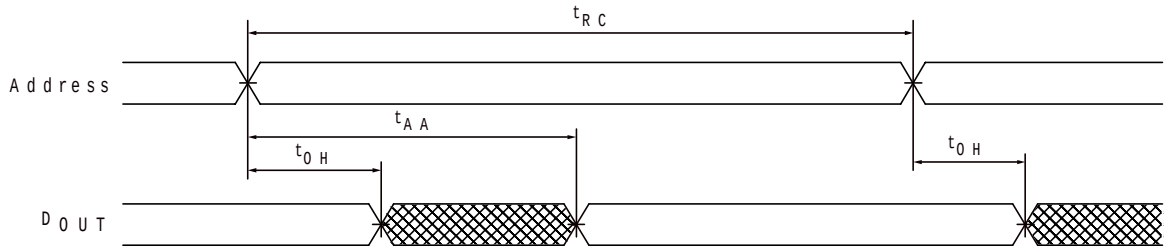
PARAMETER	SYM.	T14M1024A-10		T14M1024A-12		T14M1024A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Enable to End of Write	t_{CW}	8	-	10	-	11	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	11	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	10	-	11	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data Valid to End of Write	t_{DW}	6	-	8	-	8	-	ns
Data Hold from End of Write	t_{DH}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ*}	-	5	-	6	-	6	ns
Output Disable to Output in High Z	t_{OHZ*}	-	5	-	6	-	7	ns
Output Active from End of Write	t_{OW}	0	-	0	-	0	-	ns

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

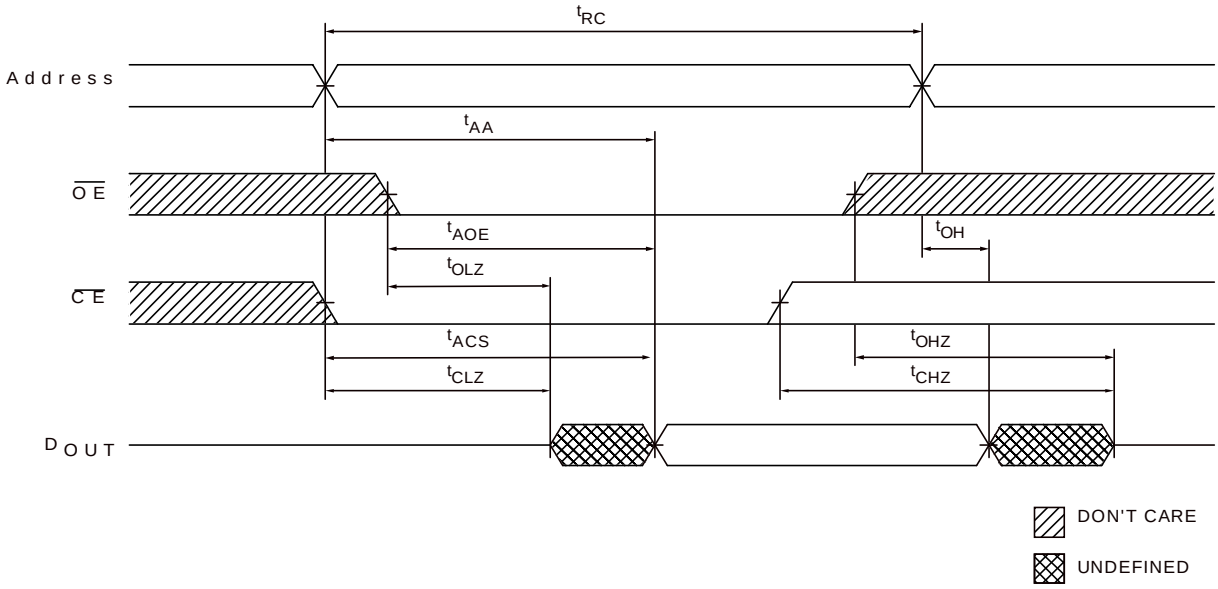
READ CYCLE 1

(Address Controlled)

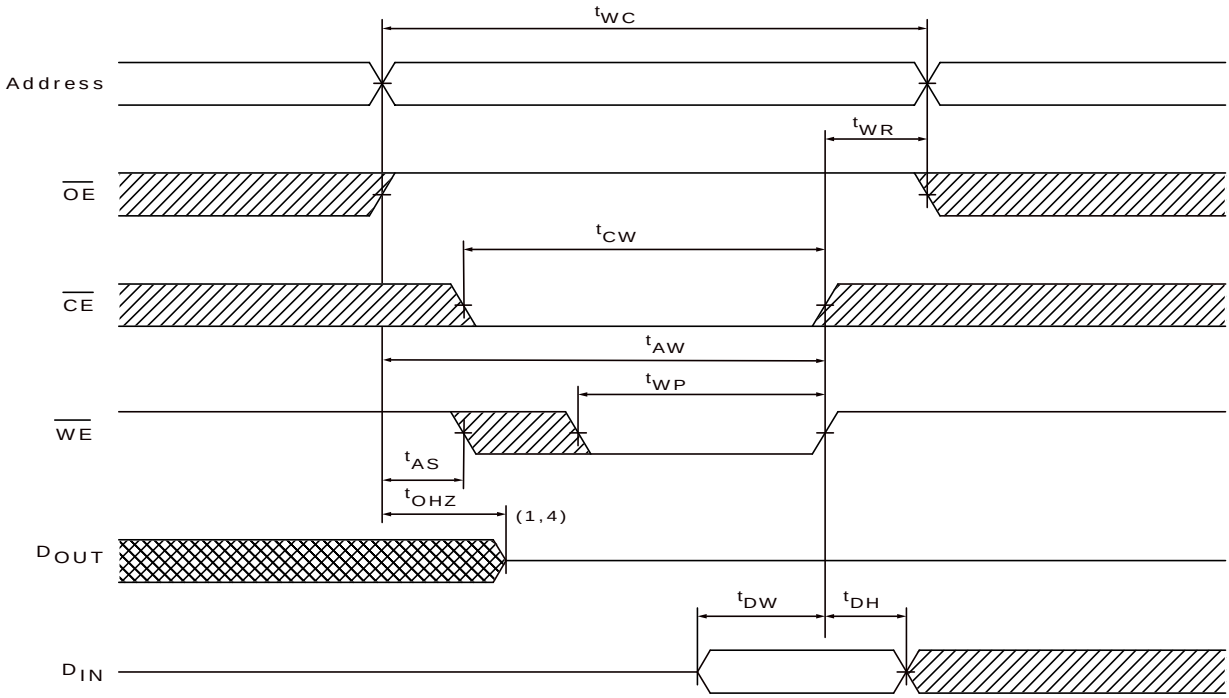


READ CYCLE 2

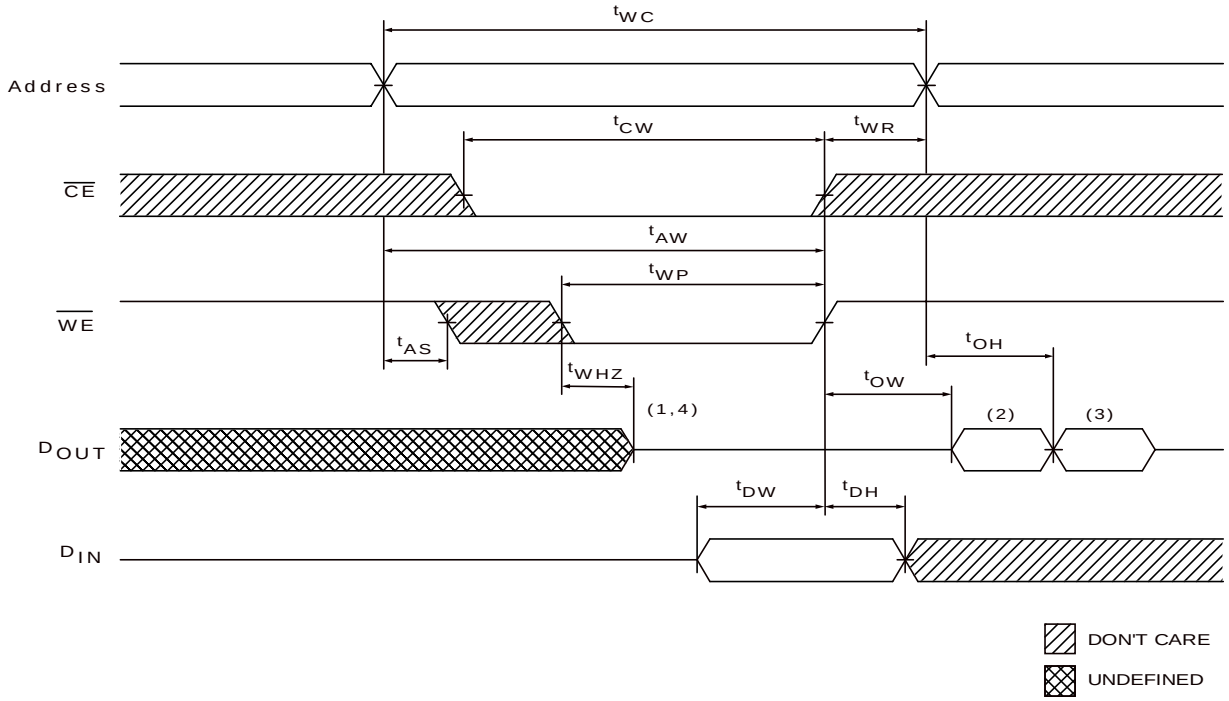
(Chip Enable Controlled)



WRITE CYCLE 1 ($\overline{OE}$ CLOCK)



WRITE CYCLE 2 ($\overline{OE}$ = V_{IL} Fixed)

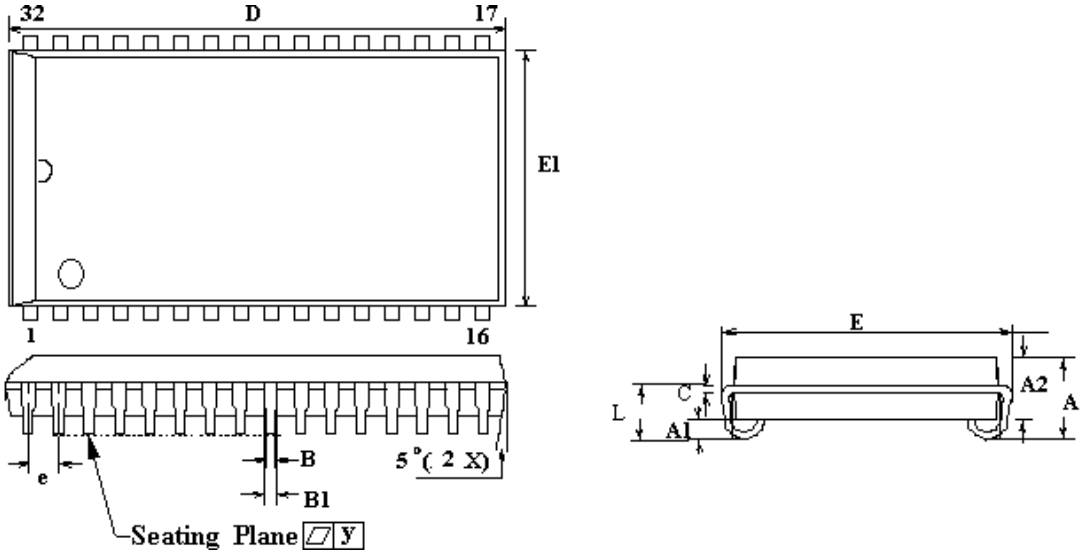


Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

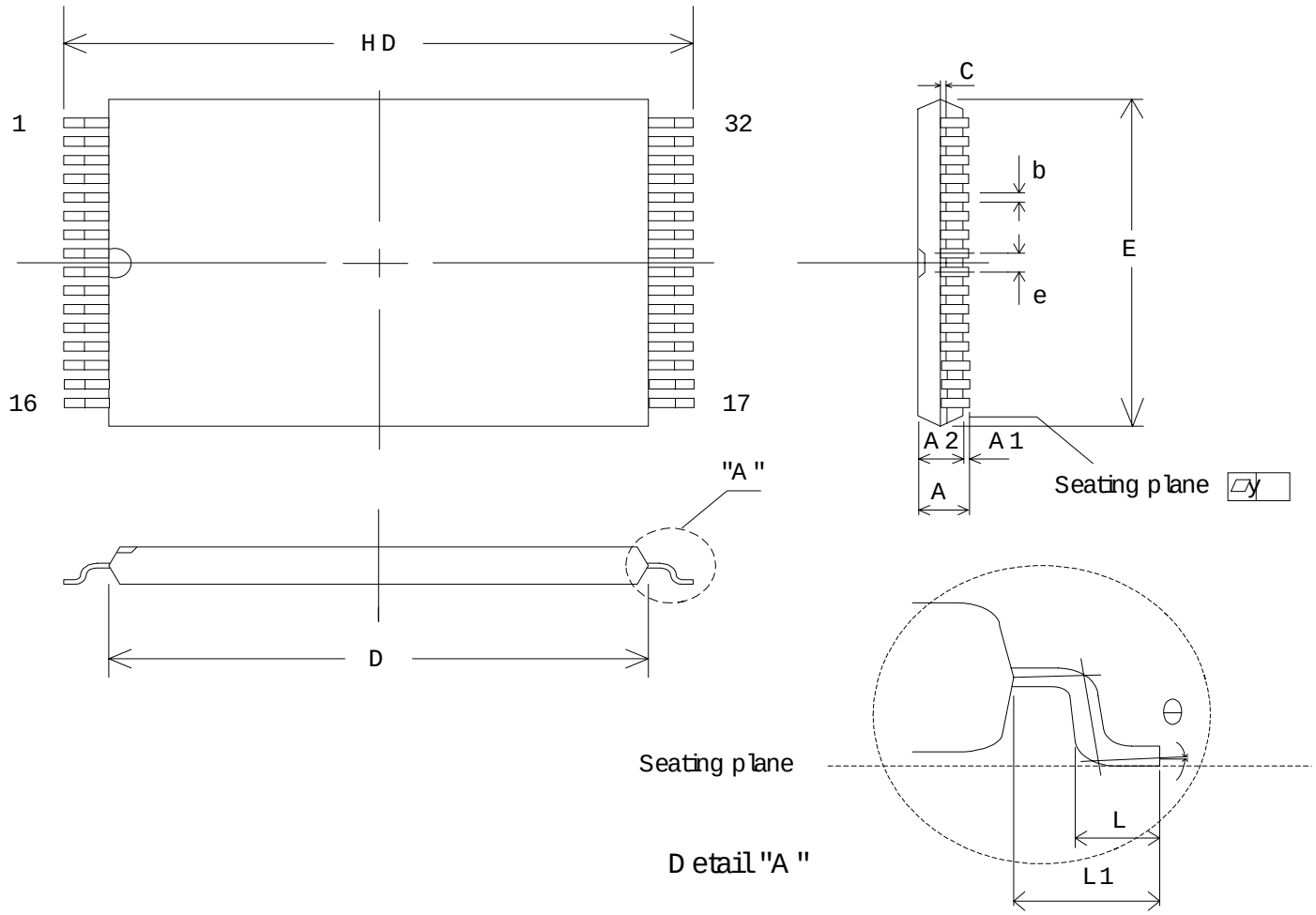
PACKAGE DIMENSIONS

32-LEAD SOJ SRAM (300 mil)



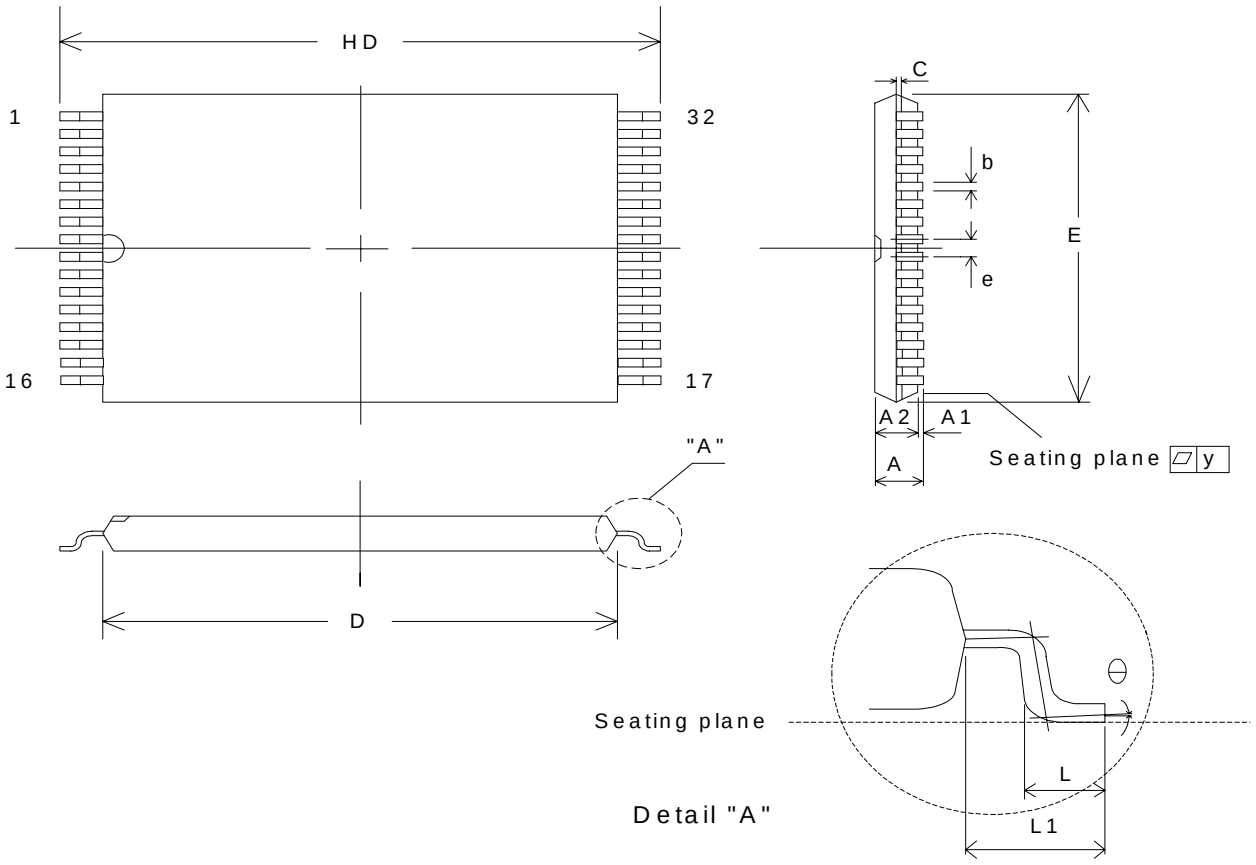
SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.140(MAX)	3.556(MAX)
A1	0.026(MIN)	0.660(MIN)
A2	0.100±0.005	2.540±0.127
B	0.018(TYP)	0.457(TYP)
B1	0.028(TYP)	0.711(TYP)
C	0.008(TYP)	0.203(TYP)
D	0.823±0.005	20.904±0.127
E	0.335±0.010	8.509±0.254
E1	0.300±0.005	7.620±0.127
e	0.050(TYP)	1.270(TYP)
L	0.086±0.010	2.184±0.254
y	0.003(MAX)	0.076(MAX)

PACKAGE DIMENSIONS
32-LEAD TSOP-I (8x20mm)



SYMBOL	DIMENSIONS IN INCHES			DIMENSIONS IN MM		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.035	0.040	0.041	0.90	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
C	0.004	0.006	0.008	0.10	0.15	0.21
HD	0.787 TYP			20.00 TYP		
D	0.724 TYP			18.40 TYP		
E	0.315 TYP			8.00 TYP		
e	0.020 TYP			0.50 TYP		
L	0.020	0.024	0.028	0.50	0.60	0.70
L1	0.032 TYP			0.813 TYP		
θ	0°	3°	5°	0°	3°	5°

PACKAGE DIMENSIONS
32-LEAD TSOP-I (8x13.4mm)



SYMBOL	DIMENSIONS IN INCHES			DIMENSIONS IN MM		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.035	0.040	0.041	0.90	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
C	0.004	0.006	0.008	0.10	0.15	0.21
HD	0.528 TYP			13.40 TYP		
D	0.465 TYP			11.80 TYP		
E	0.315 TYP			8.00 TYP		
e	0.020 TYP			0.50 TYP		
L	0.020	0.024	0.028	0.50	0.60	0.7
L1	0.032TYP			0.813 TYP		
θ	0°	3°	5°	0°	3°	5°