## Features

**Advance Information**

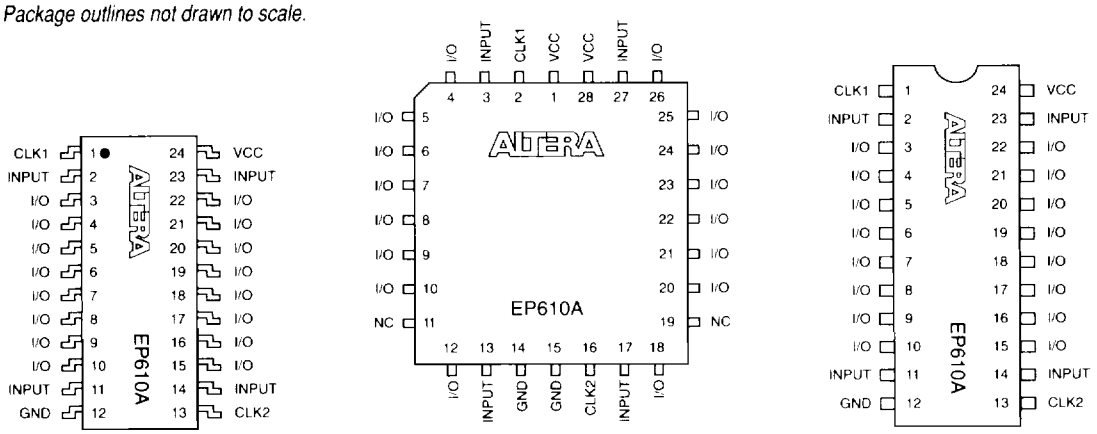
- Highest-performance 16-macrocell EPLD
  - Combinatorial speeds with $t_{PD}$ = 10 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610T, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in reprogrammable plastic chip carrier packages:
  - 24-pin dual in-line package (PDIP)
  - 24-pin small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

## General Description

Altera's EP610A Erasable Programmable Logic Device (EPLD) is a high-speed version of the EP610 EPLD. It offers enhanced performance and is available in reprogrammable plastic 24-pin, 300-mil DIP; 24-pin SOIC; and 28-pin J-lead chip carrier packages. It is also available with maximum $t_{PD}$ values of 10 ns and 12 ns. See Figure 9.

***Figure 9. EP610A Package Pin-Out Diagrams***

*Package outlines not drawn to scale.*



### Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | -2.0 | 7.0 | V |
| $V_{PP}$ | Programming supply voltage | *See Note (1)* | -2.0 | 13.5 | V |
| $V_I$ | DC input voltage | | -2.0 | 7.0 | V |
| $I_{MAX}$ | DC $V_{CC}$ or GND current | | -175 | 175 | mA |
| $I_{OUT}$ | DC output current, per pin | | -25 | 25 | mA |
| $P_D$ | Power dissipation | | | 1000 | mW |
| $T_{STG}$ | Storage temperature | No bias | -65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | -65 | 135 | °C |

### Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | °C |
| $T_A$ | Operating temperature | For industrial use | -40 | 85 | °C |
| $T_C$ | Case temperature | For military use | -55 | 125 | °C |
| $t_R$ | Input rise time | | | 25 | ns |
| $t_F$ | Input fall time | | | 25 | ns |

### DC Operating Conditions

*See Notes (2), (3)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | -0.3 | | 0.8 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}$ = -4 mA DC | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA DC | | | 0.5 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | -10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or GND | -40 | | 40 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current (standby) | $V_I$ = $V_{CC}$ or GND, No load | | 45 | 90 | mA |
| $I_{CC3}$ | $V_{CC}$ supply current (active) | $V_I$ = $V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)* | | 45 | 90 | mA |

### Capacitance

*See Note (5)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{CLK}$ | Clock pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 16 | pF |

## AC Operating Conditions *See Note (3)*

| | | | EP610A-10 | | EP610A-12 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 10 | | 12 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 10 | | 12 | ns |
| $t_{PZX}$ | Input to output enable | | | 10 | | 12 | ns |
| $t_{PXZ}$ | Input to output disable, *See Note (6)* | C1 = 5 pF | | 10 | | 12 | ns |
| $t_{CLR}$ | Asynchronous output clear time | C1 = 35 pF | | 10 | | 12 | ns |

| ***Global Clock Mode*** | | | EP610A-10 | | EP610A-12 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $f_{MAX}$ | Maximum frequency | *See Note (7)* | 100 | | 83.3 | | MHz |
| $t_{SU}$ | Input setup time | | 8 | | 8 | | ns |
| $t_{H}$ | Input hold time | | 0 | | 0 | | ns |
| $t_{CH}$ | Clock high time | | 5 | | 6 | | ns |
| $t_{CL}$ | Clock low time | | 5 | | 6 | | ns |
| $t_{CO1}$ | Clock to output delay | | | 6 | | 6 | ns |
| $t_{CNT}$ | Minimum clock period | | | 10 | | 12 | ns |
| $f_{CNT}$ | Internal maximum frequency | *See Note (4)* | 100 | | 83.3 | | MHz |

| ***Array Clock Mode*** | | | EP610A-10 | | EP610A-12 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $f_{MAX}$ | Maximum frequency | *See Note (7)* | 100 | | 83.3 | | MHz |
| $t_{ASU}$ | Input setup time | | 5 | | 6 | | ns |
| $t_{AH}$ | Input hold time | | 5 | | 6 | | ns |
| $t_{ACH}$ | Clock high time | | 5 | | 6 | | ns |
| $t_{ACL}$ | Clock low time | | 5 | | 6 | | ns |
| $t_{ACO1}$ | Clock to output delay | | | 12 | | 13 | ns |
| $t_{ACNT}$ | Minimum clock period | | | 10 | | 12 | ns |
| $f_{ACNT}$ | Internal maximum frequency | *See Note (4)* | 100 | | 83.3 | | MHz |

*Notes to tables:*

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5 V.
(3) Operating conditions: $V_{CC}$ = 5 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
$V_{CC}$ = 5 V ± 10%, $T_A$ = –40° C to 85° C for industrial use.
$V_{CC}$ = 5 V ± 10%, $T_C$ = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 16-bit counter.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF.
(6) Sample-tested only for an output change of 500 mV.
(7) The $f_{MAX}$ values represent the highest frequency for pipelined data.

## Product Availability

| Operating Temperature | | Availability |
|---|---|---|
| Commercial | (0 C to 70 C) | Consult factory |
| Industrial | (–40° C to 85 C) | Consult factory |
| Military | (–55 C to 125° C) | Consult factory |