Supertex inc.

HCT/SC373
HCT/SC374
HCT/SC533
HCT/SC534
HCT/SC563
HCT/SC564
HCT/SC573
HCT/SC574

Octal D-Type Transparent Latches
Octal Edge-Triggered Flip Flops

Product Summary

Device	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
Transparent Latches	Non-Inverted	74HCT373	74SC373	54HCT373
	Inverted	74HCT533	74SC533	54HCT533
	Inverted	74HCT563	74SC563	54HCT563
	Non-Inverted	74HCT573	74SC573	54HCT573
D-Type Flip Flop	Non-Inverted	74HCT374	74SC374	54HCT374
	Inverted	74HCT534	74SC534	54HCT534
	Inverted	74HCT564	74SC564	54HCT564
	Non-Inverted	74HCT574	74SC574	54HCT574
Operating temperature range (°C)		−40 to +85	−40 to +85	−55 to +125
Recommended opearting voltage (V)		4.75 to 5.25	4.75 to 5.25	4.50 to 5.50
Maximum gate propagation delay time (ns)		38	47	47

Features

- ☐ Pin and function compatible to 54/74LS equivalent circuits.
- ☐ Typical operating supply current: 10μA
- ☐ MIL STD 883B Screening/Leadless chip carrier available.
- ☐ Fast propagation delay times
- ☐ Fan out of 30 LSTTL loads.
- ☐ Fully TTL and CMOS compatible
- ☐ −40°C to +85°C operating temperature range
- ☐ Capable of operating over 3-volt to 6-volt range
- ☐ High speed silicon-gate CMOS technology

General Description

This family of 8-bit latches/flip flops feature 3-state operation and are designed for use in high speed, bus oriented systems.

The octal latches are transparent D-type latches, meaning that while the enable (E) is high, the Q outputs will follow the data D-inputs. When the enable is taken low, the outputs will be latched at the level of the data that was setup.

The octal flip flips are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the last state that was setup at the D-inputs.

Schmidtt Trigger buffered inputs at the enable/clock lines simplify system design through improved noise rejection capability of the hysteresis. A buffered output control input can be used to place the outputs in either an active state or in a high impedance state. While in the high impedance state, the outputs neither load nor drive the bus lines.

Absolute Maximum Ratings

Rating	Value
Supply voltage, VCC	−0.5V to +7.0V
Input voltage, VI	−0.3V to VCC +0.3V
Short circuit output current, ISC (not more than 1 output for more than 1 second)	±100mA
Operating temperature range, TA 74HCT, 74SC (commercial) 54HCT (military)	−40° C to + 85° C −55°C to +125°C
Storage temperature, TS	−65°C to +150°C
Power dissipation, PD	500mW

Recommended Operating Conditions

Symbol	Parameter	54HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
VCC	Supply voltage	4.50	5.00	5.50	4.75	5.00	5.25	V	
VI	Input voltage	0		VCC	0		VCC		
TA	Operating temperature range	−55		125	0		70	°C	
tW	Clock/enable pulse clock width high low	 15 15			 15 15			ns	
tSU	Data setup time XX3 XX4	 0 ↓ 20↑			 0 ↓ 20↑			ns	(see note 1)
tH	Data hold time XX3 XX4	 10↓ 0 ↑			 10↓ 0 ↑			ns	(see note 1)
VCCF	Functional operating VCC Range	3.00		6.00	3.00		6.00	V	

Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	54HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
VIH	High-level input voltage	2.0			2.0			V	
VIL	Low-level input voltage			0.7			0.8		
VOH	High-level output voltage	2.4			2.4			V	VCC = min, IOH = −10mA VIL = 0.8V, VIH = 2V
VOL	Low-level output voltage			0.40			0.40		VCC = min, IOL = 12mA VIL = 0.8V, VIH = 2V
IOZH	OFF-State output current, high-level voltage applied			20			20	μA	VCC = max, VO = 2.7V VIL = 0.8V, VIH = 2V
IOZL	OFF-State output current, low-level voltage applied			−20			−20		VCC = max, VO = 0.4V VIL = 0.8V, VIH = 2V
II	Input current			5			1	μA	VCC = max, VI = VCC
ICC	Supply current		0.01	0.5		0.01	0.1	mA	VCC = max, outputs open VI = VCC or GND

Note 1: Clock/Enable transition – ↑ Low to high, ↓ High to low.

Switching Characteristics (V_{CC} = 5.0V, T_A = 25°C)

Symbol	Parameter	54HCT/74HCT			74SC			Unit	Conditions
		min	typ	max	min	typ	max		
tPLH	Data to output propagation delay, low-to-high-level output								
	XX3			38			47	ns	C_L = 50 pF, R_L = 1 KΩ
tPHL	Data to output propagation delay, high-to-low-level output								
	XX3			38			47		
tPLH	Clock/enable to output propagation delay, low-to-high-level output								
	XX3			30			49		
	XX4			28			47	ns	C_L = 50 pF, R_L = 1 KΩ
tPHL	Clock/enable to output propagation delay, high-to-low level output								
	XX3			30			49		
	XX4			28			47		
tPZH	Output control to output propagation delay, enable time to high-level output								
	XX3			28			47		
	XX4			28			47	ns	C_L = 50 pF, R_L = 1 KΩ
tPZL	Output control to output propagation delay, enable time to low-level output								
	XX3			36			47		
	XX4			28			47		
tPHZ	Output control to output propagation delay, disable time from high-level output								
	XX3			20			33		
	XX4			20			33	ns	C_L = 50 pF, R_L =1 KΩ
tPLZ	Output control to output propagation delay, disable time from low-level output								
	XX3			25			41		
	XX4			25			41		
fmax	Maximum operating frequency	35			20			MHz	All outputs loaded
C_I	Input Capacitance		8			8		pF	

Ordering Information

Octal D-Type Transparent Latches

Package	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
20-pin plastic DIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT373P 74HCT533P 74HCT563P 74HCT573P	74SC373P 74SC533P 74SC563P 74SC573P	N/A
20-pin CERDIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT373D 74HCT533D 74HCT563D 74HCT573D	74SC373D 74SC533D 74SC563D 74SC573D	54HCT373D 54HCT533D 54HCT563D 54HCT573D
20-pin ceramic side-brazed DIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT373C 74HCT533C 74HCT563C 74HCT573C	74SC373C 74SC533C 74SC563C 74SC573C	54HCT373C 54HCT533C 54HCT563C 54HCT573C

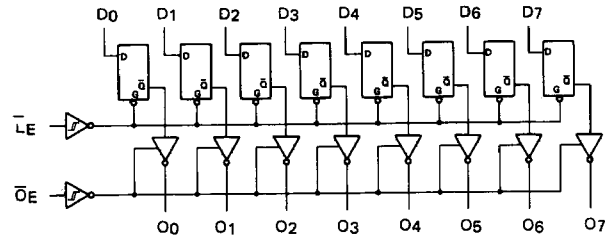
Octal Edge-Triggered Flip Flops

Package	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
20-pin plastic DIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT374P 74HCT534P 74HCT564P 74HCT574P	74SC374P 74SC534P 74SC564P 74SC574P	N/A
20-pin CERDIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT374D 74HCT534D 74HCT564D 74HCT574D	74SC374D 74SC534D 74SC564D 74SC574D	54HCT374D 54HCT534D 54HCT564D 54HCT574D
20-pin ceramic side-brazed DIP	Non-Inverting Inverting Inverting Non-Inverting	74HCT374C 74HCT534C 74HCT564C 74HCT574C	74SC374C 74SC534C 74SC564C 74SC574C	54HCT374C 54HCT534C 54HCT564C 54HCT574C

Note: See Switching Waveforms and Test Circuit at end of this section.

Functional Block Diagrams and Pin Configurations

373, 573



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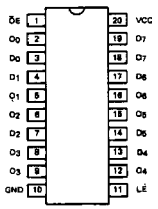

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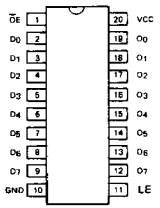

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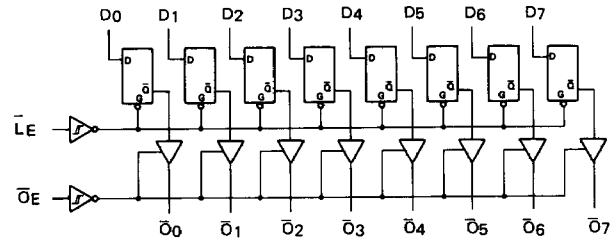

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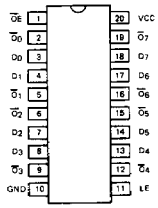

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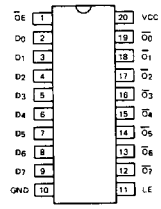

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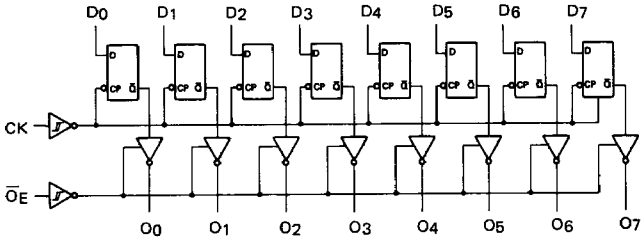

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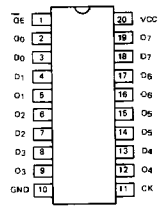

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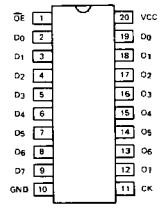

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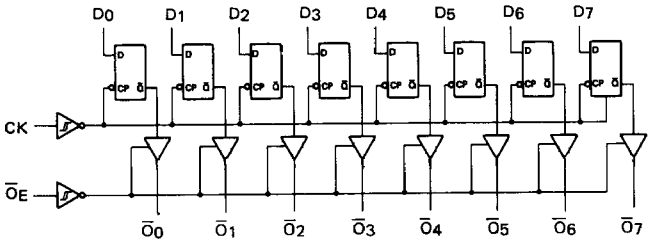

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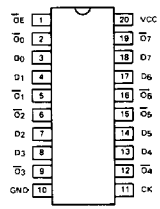

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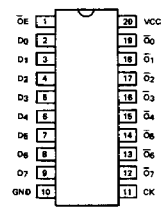

373,533,563,573 Function Table

OPERATING MODE	Inputs			Outputs	
	$\overline{OE}$	$\overline{LE}$	DN	373,573 ON	533,563 ON
Enable and Read Register	L	H	L	L	H
	L	H	H	H	L
*Latch and Read Register	L	L	D_{IN}*1	D	$\overline{D}$
Outputs Disable	H	X	X	Hi - Z	Hi - Z

D_{IN}*1= Voltage level on input one set up time prior to High to Low transition on LE.

374,534,564,574 Function Table

OPERATING MODE	Inputs			Outputs	
	$\overline{OE}$	CK	DN	374,574 ON	534,564 ON
Latch and Read Register	L	↑	D_{IN}*2	D	$\overline{D}$
*Latch Register and Output disable	H	↑	D_{IN}*2	Hi - Z	Hi - Z

D_{IN}*2= Voltage level on input one set up time prior to Low to High transition on CK.

*Even though the outputs may be disabled the latch function of the device is still operational.