

Preliminary W24V04



512K × 8 CMOS STATIC RAM

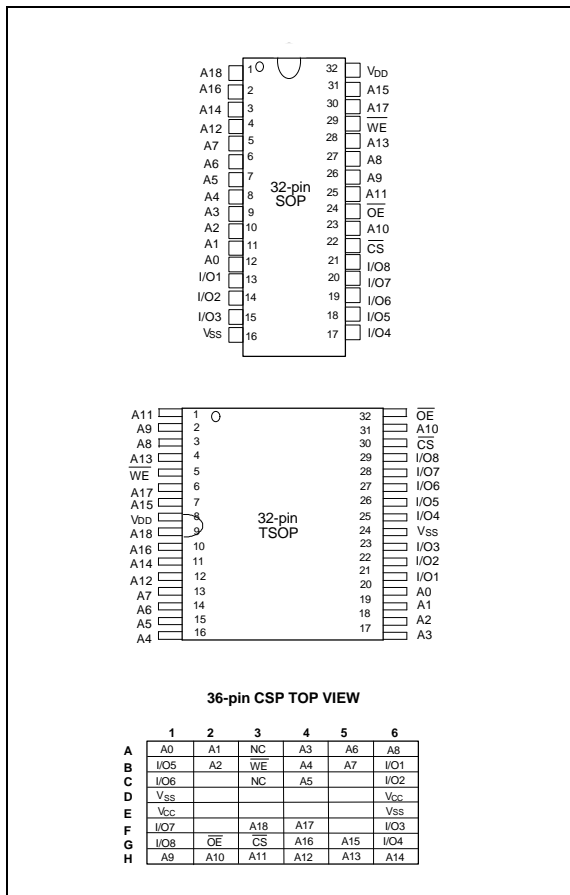
GENERAL DESCRIPTION

The W24V04 is a normal-speed, very low-power CMOS static RAM organized as 524288 × 8 bits that operates on a wide voltage range from 2.3V to 2.7V power supply. The W24V04, W24V04-LE and W24V04-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

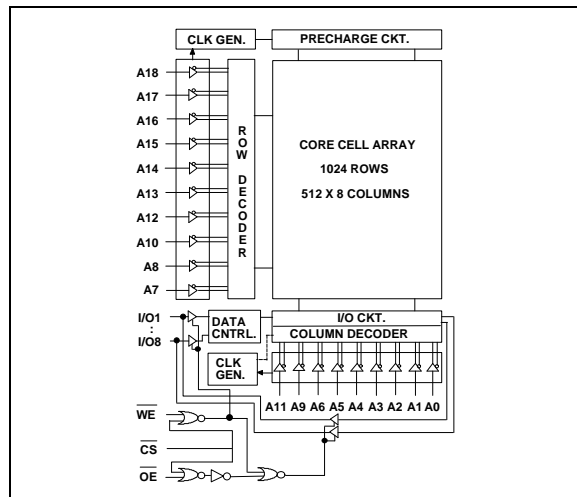
FEATURES

- Low power consumption
- Access time: 85 nS
- 2.3V to 2.7V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Packaged in 32-pin 450 mil SOP, standard type one TSOP (8 mm × 20 mm), small type one TSOP (8 mm × 13.4 mm) and 36-pin CSP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A18	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

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TRUTH TABLE

CS	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to VSS Potential		-0.5 to +4.6	V
Input/Output to VSS Potential		-0.5 to VDD +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VSS = 0V; TA (°C) = -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	W24V04		UNIT
			MIN.	MAX.	
Operating Power Voltage	VDD	-	2.3	2.7	V
Input Low Voltage	VIL	-	-0.2	+0.4	V
Input High Voltage	VIH	-	+2.0	VDD +0.2	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	+1	μA
Output Leakage Current	ILO	V _{I/O} = VSS to VDD CS = VIH (min.) or OE = VIH (min.) or WE = VIL (max.)	-1	+1	μA
Output Low Voltage	VOL	IOL = +0.5 mA	-	0.4	V
Output High Voltage	VOH	IOH = -0.5 mA	2.0	-	V

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Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	W24V04		UNIT
			MIN.	MAX.	
Operating Power Supply Current	I _{DD}	$\overline{CS} = V_{IL} \text{ (max.)}$ I/O = 0 mA Cycle = min. Duty = 100%	-	30	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH} \text{ (min.)}$ Duty = 100%	-	0.3	mA
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	5	μA

CAPACITANCE

(T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	8	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	10	pF

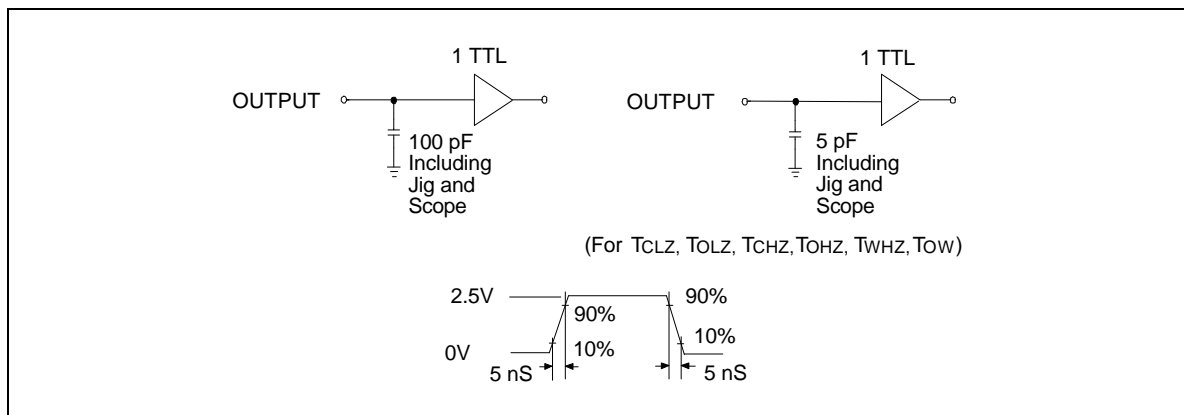
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 2.5V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.2V
Output Load	See the drawing below

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = -20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	W24V04		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	85	-	nS
Address Access Time	TAA	-	85	nS
Chip Select Access Time	TACS	-	85	nS
Output Enable to Output Valid	TAOE	-	50	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	35	nS
Output Hold from Address Change	TOH	10	-	nS

*These parameters are sampled but not 100% tested

Write Cycle

PARAMETER	SYM.	W24V04		UNIT
		MIN.	MAX.	
Write Cycle Time	TWC	85	-	nS
Chip Selection to End of Write	TCW	75	-	nS
Address Valid to End of Write	TAW	75	-	nS
Address Setup Time	TAS	0	-	nS
Write Pulse Width	TWP	65	-	nS
Write Recovery Time	\overline{CS} , \overline{WE} TWR	0	-	nS
Data Valid to End of Write	TDW	50	-	nS
Data Hold from End of Write	TDH	0	-	nS
Write to Output in High Z	TWHZ*	-	35	nS
Output Active from End of Write	TOW	8	-	nS

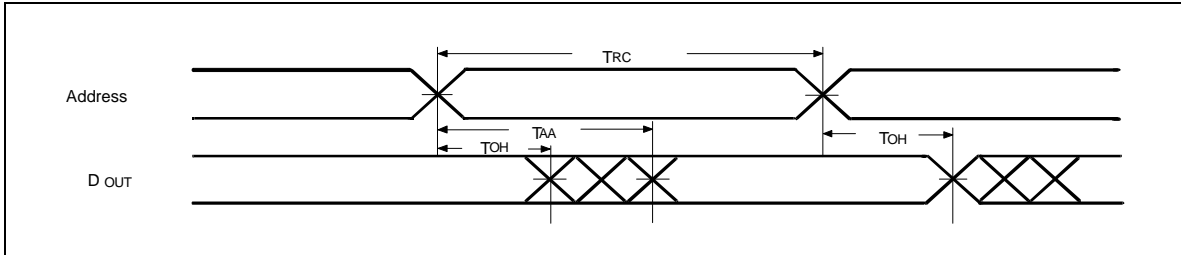
*These parameters are sampled but not 100% tested



TIMING WAVEFORMS

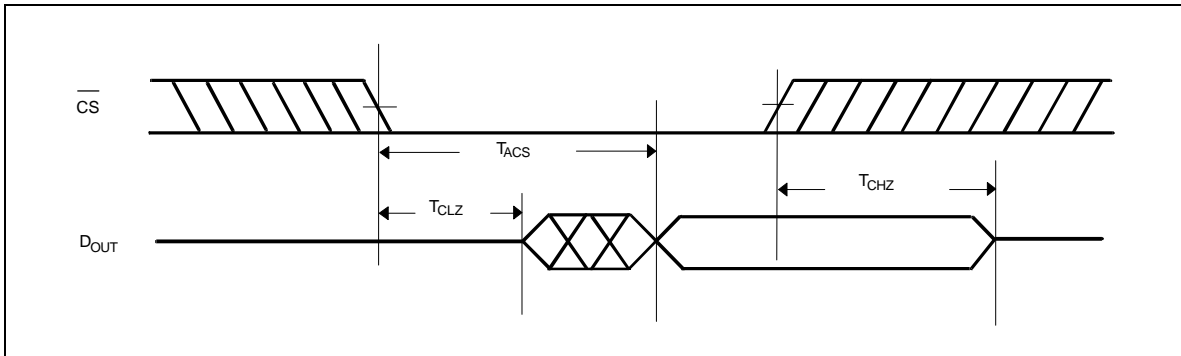
Read Cycle 1

(Address Controlled)



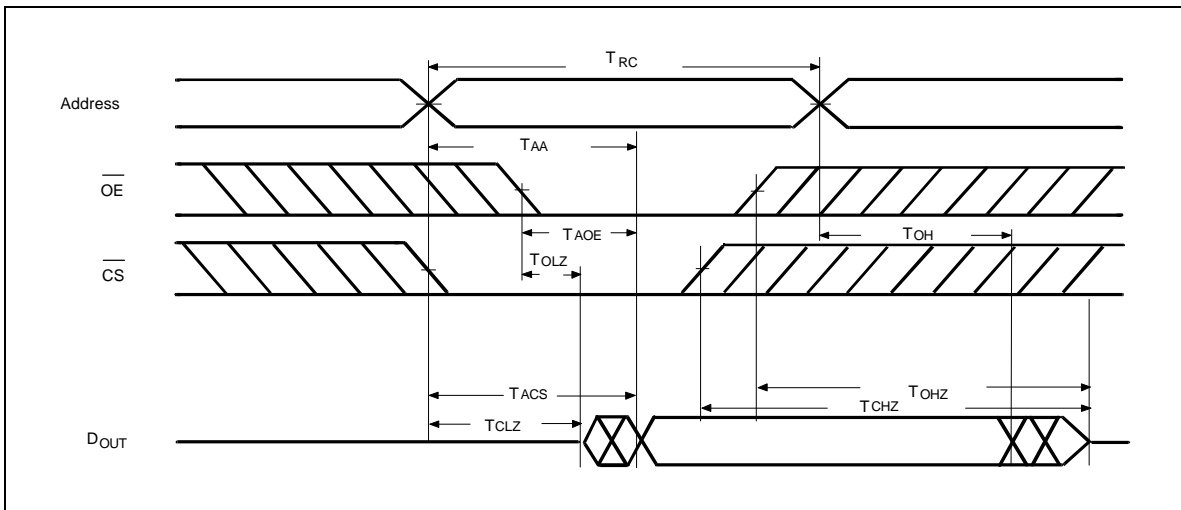
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)

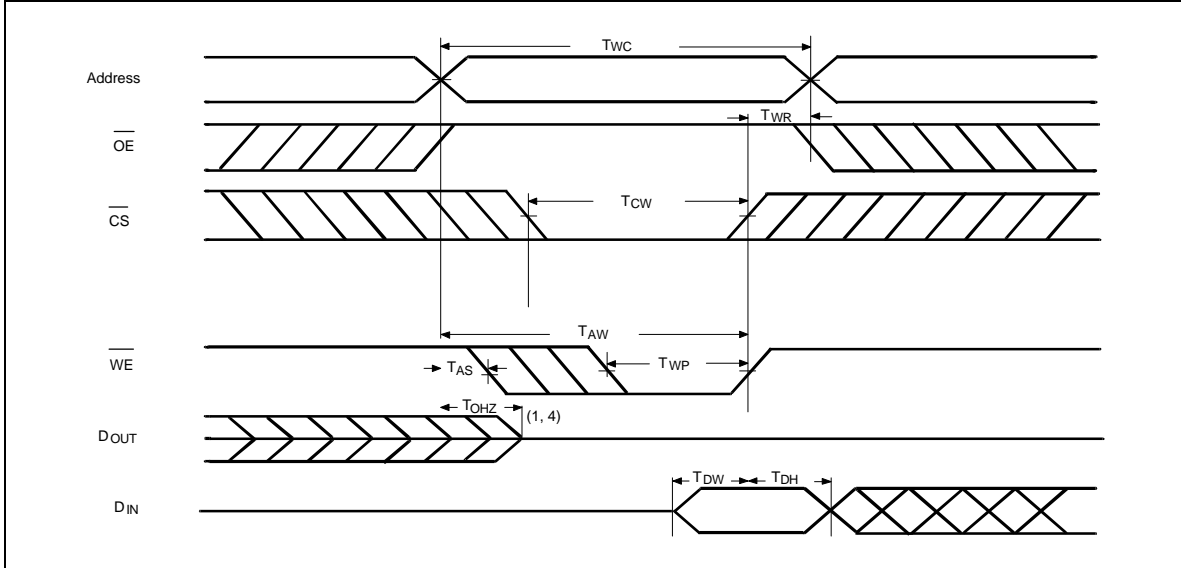


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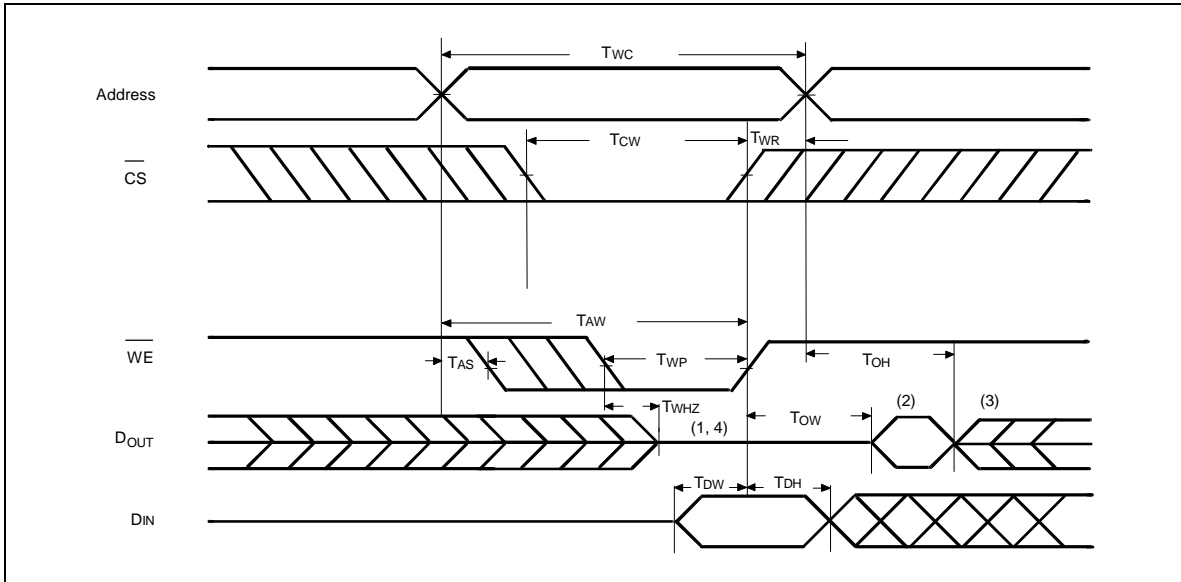
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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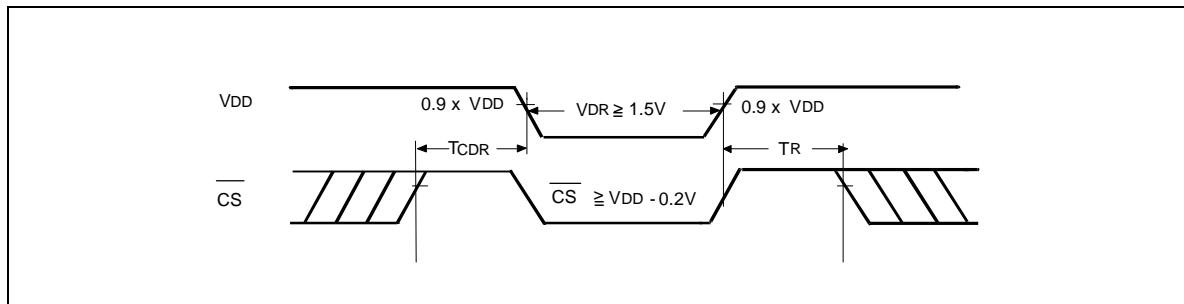
DATA RETENTION CHARACTERISTICS

(T_A (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	1.5	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3.0V$	-	-	5	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



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ORDERING INFORMATION

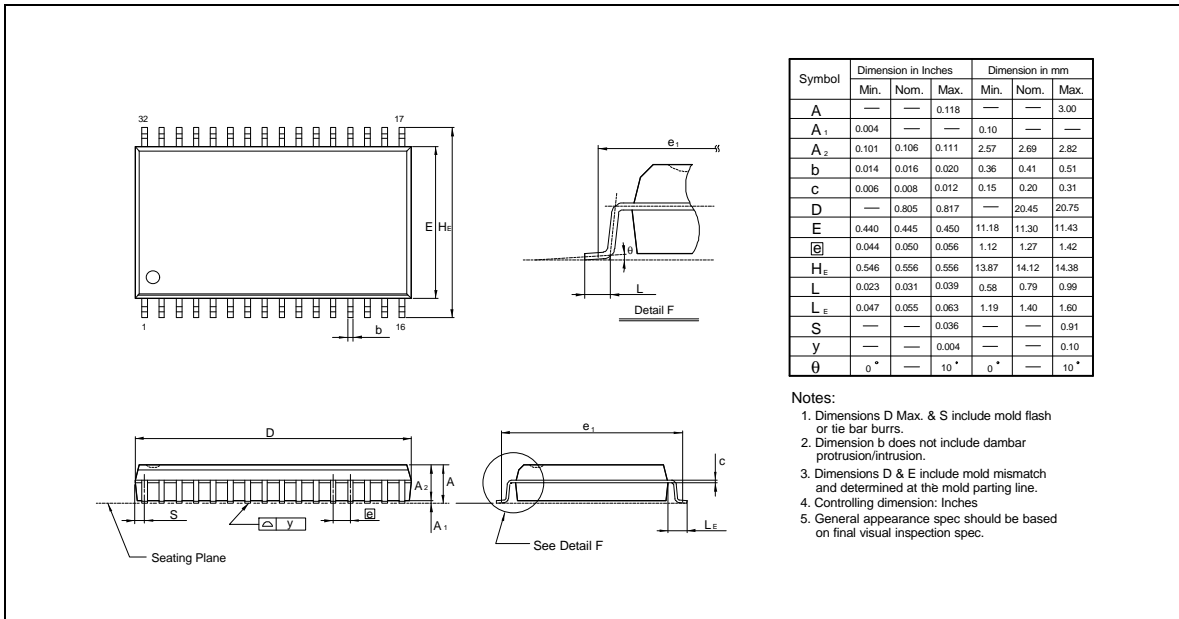
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V) / STANDBY CURRENT (μ A)	OPERATING TEMPERATURE ($^{\circ}$ C)	PACKAGE
W24V04B-85LE	85	2.5V / 5 μ A	-20 to 85	CSP
W24V04Q-85LE	85	2.5V / 5 μ A	-20 to 85	Small type one TSOP
W24V04S-85LE	85	2.5V / 5 μ A	-20 to 85	450 mil SOP
W24V04T-85LE	85	2.5V / 5 μ A	-20 to 85	Standard type one TSOP
W24V04B-85LI	85	2.5V / 5 μ A	-40 to 85	CSP
W24V04Q-85LI	85	2.5V / 5 μ A	-40 to 85	Small type one TSOP
W24V04S-85LI	85	2.5V / 5 μ A	-40 to 85	450 mil SOP
W24V04T-85LI	85	2.5V / 5 μ A	-40 to 85	Standard type one TSOP
W24V04B-85LL	85	2.5V / 20 μ A	0 to 70	CSP
W24V04Q-85LL	85	2.5V / 20 μ A	0 to 70	Small type one TSOP
W24V04S-85LL	85	2.5V / 20 μ A	0 to 70	450 mil SOP
W24V04T-85LL	85	2.5V / 20 μ A	0 to 70	Standard type one TSOP

Notes:

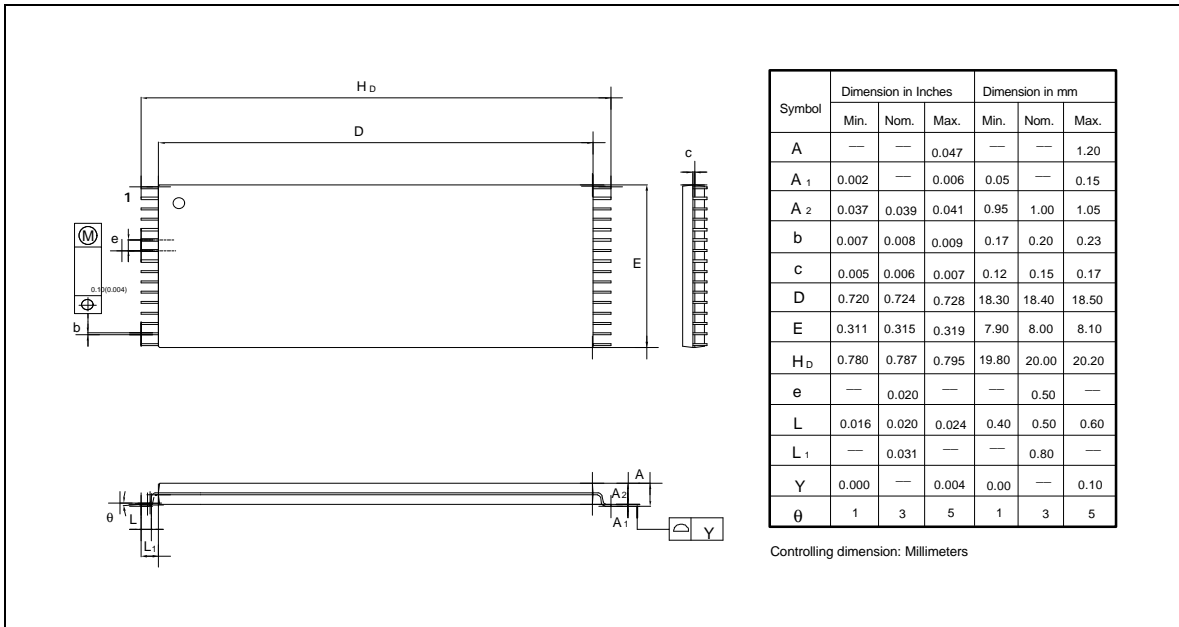
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin SOP Wide Body



32-pin Standard Type One TSOP

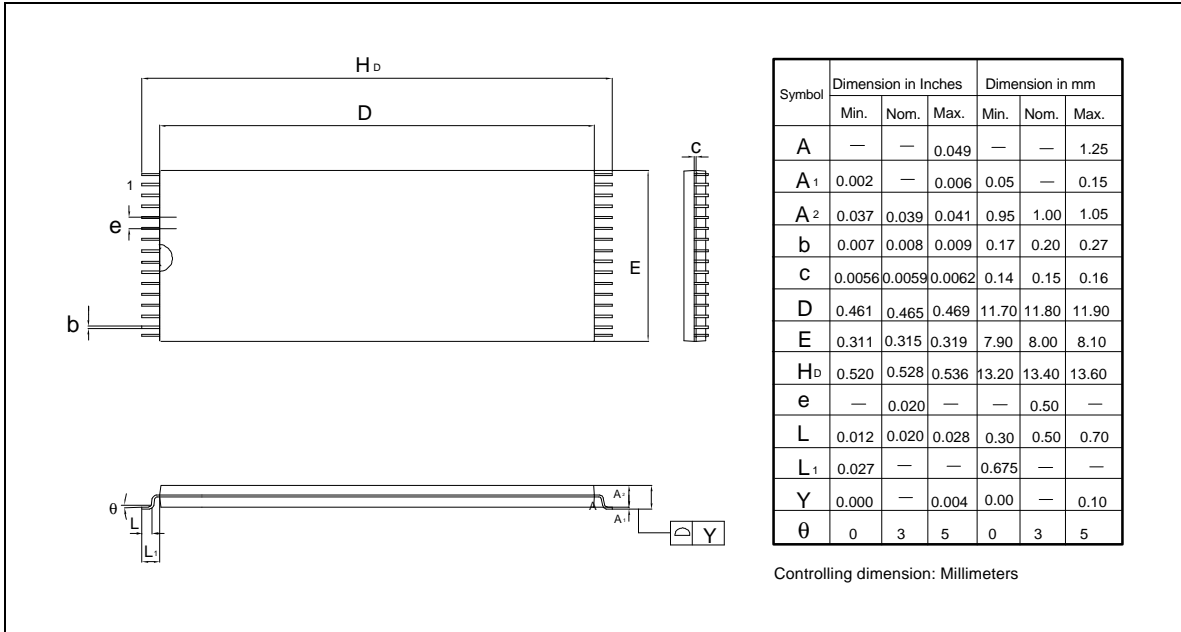


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Package Dimensions, continued

32-pin Small Type One TSOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 2000	-	Initial Issued



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Note: All data and specifications are subject to change without notice.