

**DRAM**

**4M x 4 DYNAMIC RAM**  
**EDO PAGE MODE**

**FEATURES**

- Industry-standard x 4 pinouts and timing functions
- power supply : T2316405A 2.6V(±0.2V)  
T2316407A 3.3V(±0.3V)
- All device pins are TTL- compatible.
- 2048-cycle refresh in 32 ms.
- Refresh modes:  $\overline{\text{RAS}}$  only,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  (CBR) and HIDDEN.
- Extended data-out (EDO) PAGE MODE access cycle.

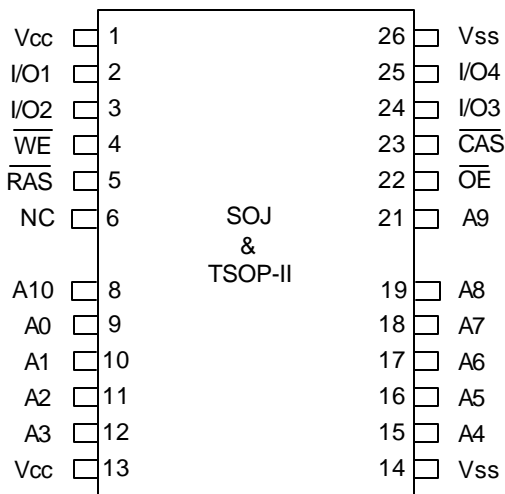
**OPTION**

TIMING	MARKING
50ns (For T2316407A only)	-50
60ns (For T2316407A only)	-60
70ns (For T2316407A only)	-70
100ns (For T2316405A only)	-10

**PACKAGE**

26/24-pin SOJ	J
26/24-pin TSOP-II	S

**PIN ARRANGEMENT (Top View)**



**GRNERAL DESCRIPTION**

The T2316405A and T2316407A is a randomly accessed solid state memory containing 16,777,216 bits organized in a x 4 configuration. It offers Fast Page mode with Extended Data Output (EDO).

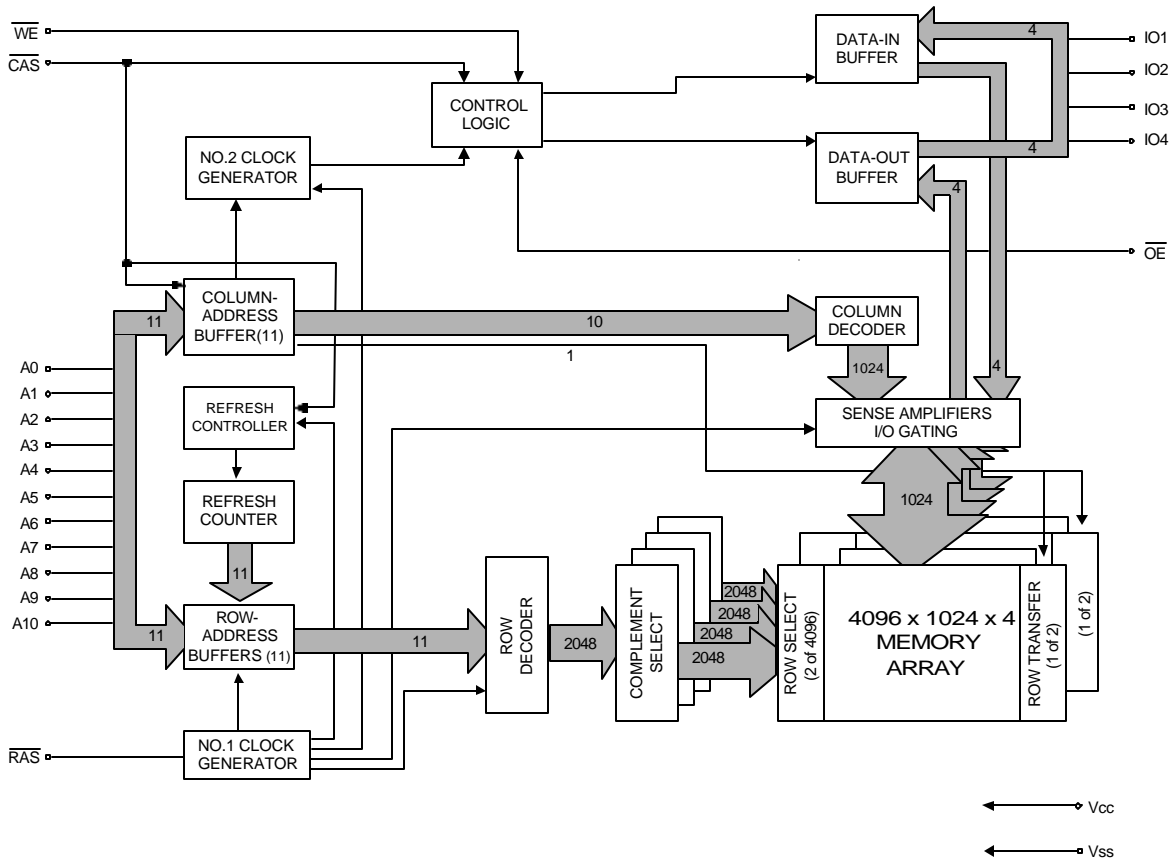
During READ or WRITE cycles, each of the 4 memory bits (1 bit per I/O) is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time.  $\overline{\text{RAS}}$  latches the first 11 bits and  $\overline{\text{CAS}}$  latches the latter 11 bits.

A READ or WRITE cycle is selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data-in is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. When  $\overline{\text{WE}}$  goes Low prior to  $\overline{\text{CAS}}$  going LOW (EARLY WRITE cycle), the output pins remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle.

A Late Write or Read-Modify-Write occurs. When  $\overline{\text{WE}}$  falls after  $\overline{\text{CAS}}$  was taken LOW (Late Write cycle).  $\overline{\text{OE}}$  must be taken HIGH to disable the data-outputs prior to applying input data.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$ .

**BLOCK DIAGRAM**



**PIN DESCRIPTION**

PIN NO.	SYM.	TYPE	DESCRIPTION
8~12,15~19,21	A0-A10	Input	Address Input
5	$\overline{RAS}$	Input	Row Address Strobe
23	$\overline{CAS}$	Input	Column Address Strobe
4	$\overline{WE}$	Input	Write Enable
22	$\overline{OE}$	Input	Output Enable
2,3,24,25	I/O1 -I/O4	Input/ Output	Data Input/ Output
1,13	Vcc	Supply	Power
14,26	Vss	Ground	Ground
6	NC		No Connect

### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative To V <sub>ss</sub>	V <sub>T</sub>	-0.5 to 4.6	V
Supply Voltage Relative To V <sub>ss</sub>	V <sub>cc</sub>	-0.5 to 4.6	V
Short circuit Output Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>T</sub>	1	W
Operating Temperature	T <sub>OPR</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 125	°C

### RECOMMENDED DC OPERATING CONDITIONS

(T<sub>a</sub> = 0 to +70°C) For T2316405A-10 only

Parameter	Symbol	Min.	Typ	Max.	Unit	Notes
Supply Voltage	V <sub>ss</sub>	0	0	0	V	
	V <sub>cc</sub>	2.4	2.6	2.8	V	1
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>cc</sub> +0.3V	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V	1

(T<sub>a</sub> = 0 to +70°C) For T2316407A-50/60/70 only

Parameter	Symbol	Min.	Typ	Max.	Unit	Notes
Supply Voltage	V <sub>ss</sub>	0	0	0	V	
	V <sub>cc</sub>	3.0	3.3	3.6	V	1
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>cc</sub> +0.3V	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V	1

Notes : 1. All voltages referenced to V<sub>ss</sub>

**DC CHARACTERISTICS**

(Ta = 0 to 70°C) T2316405A-10 Vcc = 2.6V ± 0.2V, Vss = 0V

T2316407A-50/60/70 Vcc = 3.3V ± 0.3V, Vss = 0V

Parameter	Symbol	-50		-60		-70		-10		Unit	Test Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Leakage Current	I <sub>LI</sub>	-5	5	-5	5	-5	5	-5	5	uA	0V ≤ Vin ≤ Vcc + 0.3V Other pins = 0V
Output Leakage Current	I <sub>LO</sub>	-5	5	-5	5	-5	5	-5	5	uA	0V ≤ Vout ≤ Vcc Dout = disable
Output High Voltage	V <sub>OH</sub>	2.0	-	2.0	-	2.0	-	2.0	-	V	High Iout = -2.0mA
Output Low Voltage	V <sub>OL</sub>	-	0.8	-	0.8	-	0.8	-	0.8	V	Low Iout = 2.0mA
Operating Current	I <sub>cc1</sub>	-	95	-	90	-	80	-	50	mA	RAS, CAS cycling t <sub>RC</sub> = min
Standby Current	I <sub>cc2</sub>	-	2	-	2	-	2	-	2	mA	TTL interface, RAS, CAS = VIH, DOUT = High-Z
Standby Current	I <sub>cc3</sub>	-	0.5	-	0.5	-	0.5	-	0.5	mA	CMOS interface, RAS, CAS > Vcc - 0.2V
EDO Page Mode Current	I <sub>cc4</sub>	-	95	-	90	-	80	-	50	mA	RAS = VIL, CAS cycling, t <sub>PC</sub> = min
RAS-only refresh Current	I <sub>cc5</sub>	-	95	-	90	-	80	-	50	mA	CAS = VIH, RAS cycling, t <sub>RC</sub> = min
CAS Before RAS Refresh Current	I <sub>cc6</sub>	-	95	-	90	-	80	-	50	mA	RAS, CAS cycling, t <sub>RC</sub> = min

 Note: I<sub>cc</sub> depends on output load condition when the device is selected.

 I<sub>cc</sub> max is specified at the output open condition, I<sub>cc</sub> is specified as an average current.

**CAPACITANCE**

(Ta = 25°C, f = 1M HZ, T2316405A-10 Vcc = 2.6V, T2316407A-50/60/70 Vcc = 3.3V)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (address)	C <sub>I1</sub>	-	5	pF
Input Capacitance (RAS, CAS, WE, OE)	C <sub>I2</sub>	-	7	pF
Output Capacitance (data-in/out)	C <sub>I/O</sub>	-	7	pF

**AC CHARACTERISTICS** (note 1,2,3) (Ta = 0 to 70°C)

TEST CONDITIONS:

T2316405A-10 Vcc = 2.6V ±0.2V , T2316407A-50/60/70 Vcc = 3.3V ±0.3V

VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V

Input rise and fall times: 2ns , Output Load: 2TTL gate + CL (100pF)

AC CHARACTERISTICS PARAMETER	SYM	-50		-60		-70		-10		UNIT	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read or Write Cycle Time	t <sub>RC</sub>	84		104		124		180		ns	
Read Write Cycle Time	t <sub>RWC</sub>	108		135		160		240		ns	
EDO-Page-Mode Read or Write Cycle Time	t <sub>PC</sub>	20		25		30		40		ns	
EDO-Page-Mode Read-Write Cycle Time	t <sub>PCM</sub>	56		68		78		120		ns	
Access Time From $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		60		70		100	ns	4
Access Time From $\overline{\text{CAS}}$	t <sub>CAC</sub>		13		15		20		25	ns	5
Access Time From $\overline{\text{OE}}$	t <sub>OAC</sub>		13		15		20		25	ns	13
Access Time From Column Address	t <sub>AA</sub>		25		30		35		50	ns	8
Access Time From $\overline{\text{CAS}}$ Precharge	t <sub>ACP</sub>		30		35		40		55	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	50	10K	60	10K	70	10K	100	10K	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	t <sub>RASC</sub>	50	100K	60	100K	70	100K	100	100K	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	8		10		13		25		ns	
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	30		40		50		70		ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	8	10K	10	10K	13	10K	25	10K	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	38		40		45		100		ns	
$\overline{\text{CAS}}$ Precharge Time (EDO Page Mode)	t <sub>CP</sub>	10		10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	12	37	14	45	14	50	25	75	ns	7
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5		5		5		5		ns	
Row Address Setup Time	t <sub>ASR</sub>	0		0		0		0		ns	
Row Address Hold Time	t <sub>RAH</sub>	8		10		10		15		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	10	25	12	30	12	35	20	50	ns	8
Column Address Setup Time	t <sub>ASC</sub>	0		0		0		0		ns	
Column Address Hold Time	t <sub>CAH</sub>	8		10		13		20		ns	
Column Address Hold Time (Reference to $\overline{\text{RAS}}$ )	t <sub>AR</sub>	21		24		27		45		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	25		30		35		50		ns	
Read Command Setup Time	t <sub>RCS</sub>	0		0		0		0		ns	14
Read Command Hold Time Reference to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		0		0		ns	9,14
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0		0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	t <sub>CLZ</sub>	0		0		0		0		ns	
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	t <sub>OFF1</sub>	0	12	0	15	0	20	0	25	ns	10,16

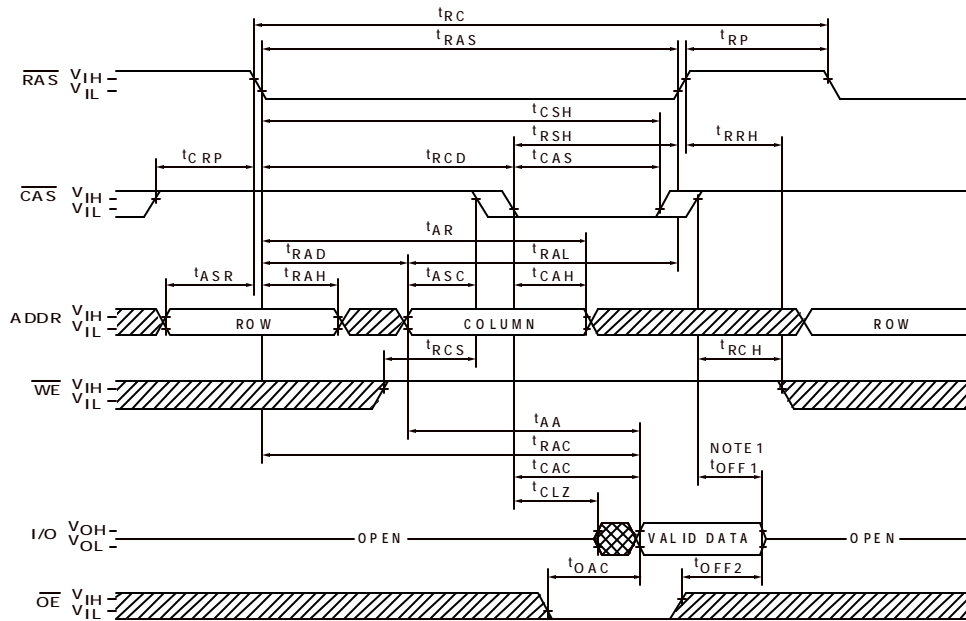
**AC CHARACTERISTICS (continued)**

AC CHARACTERISTICS PARAMETER	SYM	-50		-60		-70		-10		UNIT	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output Buffer Turn-off to $\overline{OE}$	$t_{OFF2}$	0	12	0	15	0	20	0	25	ns	16
Write Command Setup Time	$t_{WCS}$	0		0		0		0		ns	11,14
Write Command Hold Time	$t_{WCH}$	8		10		13		15		ns	
Write Command Hold Time (Reference to $\overline{RAS}$ )	$t_{WCR}$	21		24		27		40		ns	14
Write Command Pulse Width	$t_{WP}$	8		10		10		15		ns	14
Write Command to $\overline{RAS}$ Lead Time	$t_{RWL}$	10		10		13		25		ns	14
Write Command to $\overline{CAS}$ Lead Time	$t_{CWL}$	8		10		13		25		ns	14
Data-in Setup Time	$t_{DS}$	0		0		0		0		ns	12
Data-in Hold Time	$t_{DH}$	8		10		13		20		ns	12
Data-in Hold Time (Reference to $\overline{RAS}$ )	$t_{DHR}$	21		24		27		45		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	$t_{RWD}$	64		79		94		130		ns	11
Column Address to $\overline{WE}$ Delay Time	$t_{AWD}$	39		49		59		80		ns	11
$\overline{CAS}$ to $\overline{WE}$ Delay Time	$t_{CWD}$	26		34		44		55		ns	11
Transition Time (rise or fall)	$t_T$	2	50	2	50	2	50	2	50	ns	2,3
Refresh Period (2048 cycles)	$t_{REF}$	32		32		32		32		ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	$t_{RPC}$	5		5		5		5		ns	
$\overline{CAS}$ Setup Time (CBR REFRESH)	$t_{CSR}$	5		10		10		10		ns	6
$\overline{CAS}$ Hold Time (CBR REFRESH)	$t_{CHR}$	8		10		10		10		ns	6
$\overline{OE}$ Hold Time From $\overline{WE}$ During Read-Modify-Write Cycle	$t_{OEH}$	8		10		13		25		ns	15
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	$t_{OES}$	5		5		5		5		ns	
$\overline{OE}$ High Hold Time From $\overline{CAS}$ High	$t_{OEHC}$	5		5		5		5		ns	
$\overline{OE}$ High Pulse Width	$t_{OEP}$	10		10		10		10		ns	
$\overline{OE}$ Setup Prior to $\overline{RAS}$ During Hidden Refresh Cycle	$t_{ORD}$	5		7		10		13		ns	
Data Output Hold After $\overline{CAS}$ Returning Low	$t_{COH}$	5		5		5		5		ns	
Output Disable Delay From $\overline{WE}$	$t_{WHZ}$		10		15		20		25	ns	

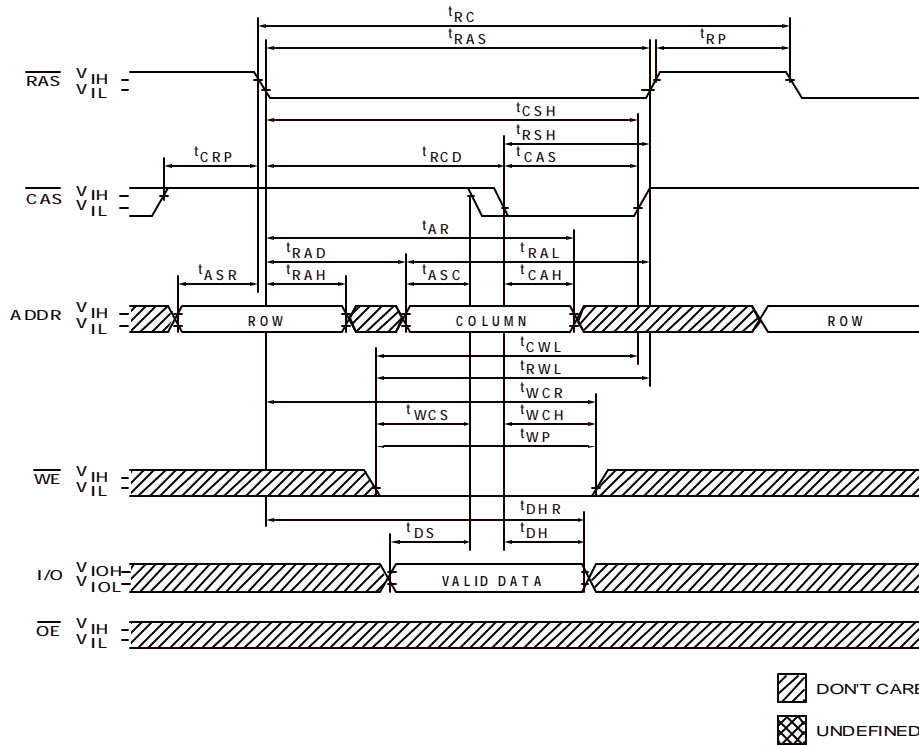
**Notes:**

1. An initial pause of 200us is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycles ( $\overline{\text{RAS}}$  only or CBR) before proper device operation is assured. The eight  $\overline{\text{RAS}}$  cycle wake-ups should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
2.  $V_{\text{IH}}(2.0\text{V})$  and  $V_{\text{IL}}(0.8\text{V})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{\text{IH}}(2.0\text{V})$  and  $V_{\text{IL}}(0.8\text{V})$ .
3. In addition to meet the transition rate specification, all input signals must transit between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  in a monotonic manner.
4. Assume that  $t_{\text{RCD}} < t_{\text{RCD}}(\text{max})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
5. Assume that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
6. Enables on-chip refresh and address counters.
7. Operation within the  $t_{\text{RCD}}(\text{max})$  limit ensures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, access time is controlled by  $t_{\text{CAC}}$ .
8. Operation within the  $t_{\text{RAD}}$  limit ensures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, access time is controlled by  $t_{\text{AA}}$ .
9. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a READ cycle.
10.  $t_{\text{OFF1}}(\text{max})$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .
11.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ , the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  or  $\overline{\text{OE}}$  go back to  $V_{\text{IH}}$ ) is indeterminate.  $\overline{\text{OE}}$  held high and  $\overline{\text{WE}}$  taken low after  $\overline{\text{CAS}}$  goes low result in a LATE WRITE ( $\overline{\text{OE}}$  - controlled) cycle.
12. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if  $\overline{\text{OE}}$  is low then taken HIGH before  $\overline{\text{CAS}}$  goes high, I/O goes open, if  $\overline{\text{OE}}$  is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. WRITE command is defined as  $\overline{\text{WE}}$  going low.
15. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{\text{OFF2}}$  and  $t_{\text{OEH}}$  met ( $\overline{\text{OE}}$  high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
16. The I/Os open during READ cycles once  $t_{\text{OFF1}}$  or  $t_{\text{OFF2}}$  occur.

READ CYCLE



EARLY WRITE CYCLE

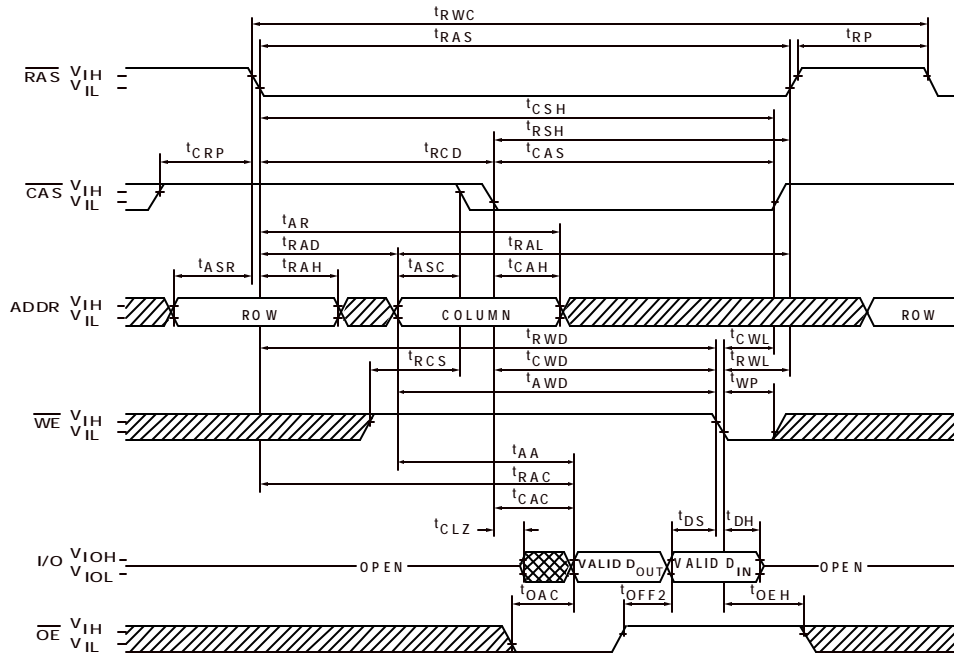


 DONT CARE  
 UNDEFINED

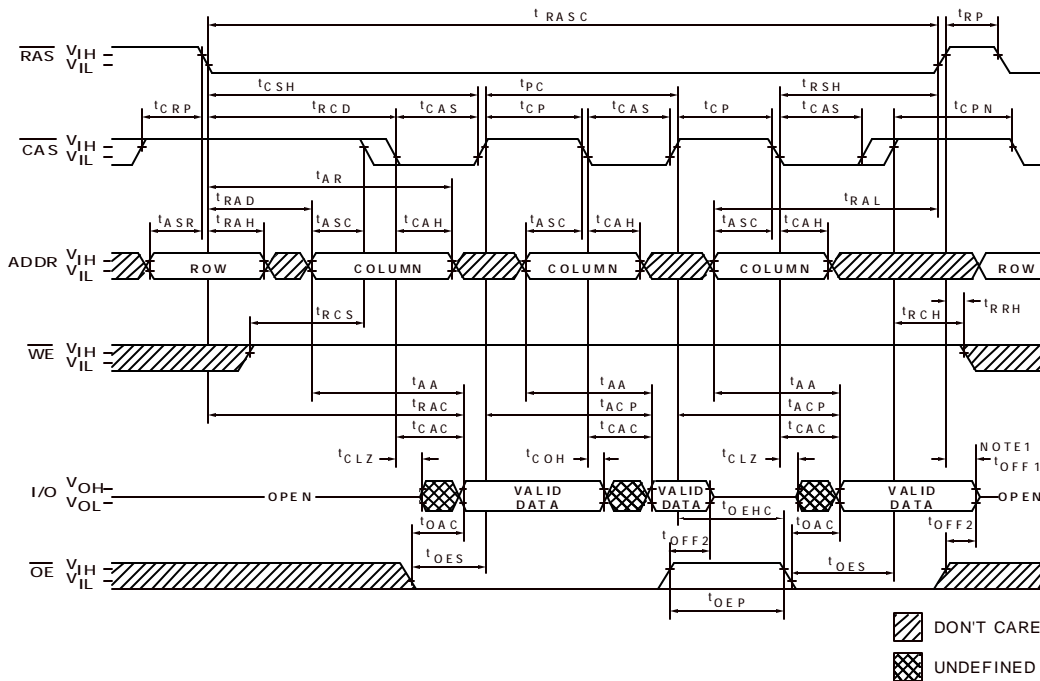
**Note:**  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.



**READ WRITE CYCLE**  
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



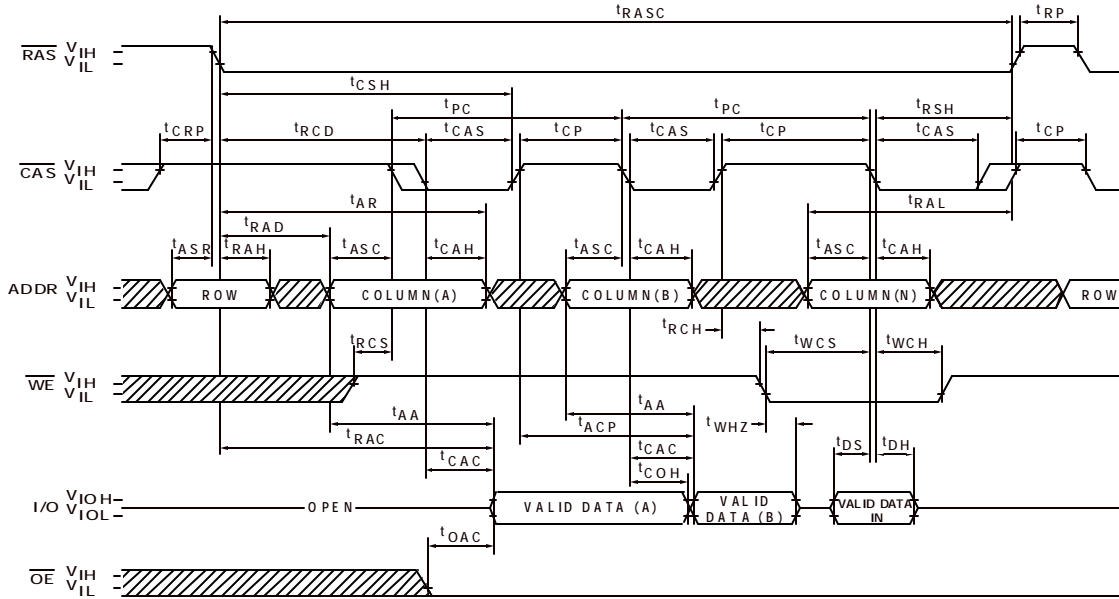
**EDO-PAGE-MODE READ CYCLE**



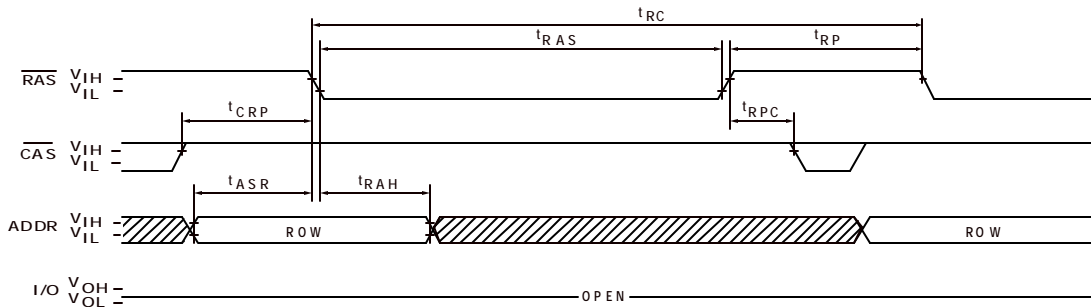
- Note:** 1.  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.  
 2.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specification.



**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE**  
(Pseudo READ-MODIFY-WRITE)

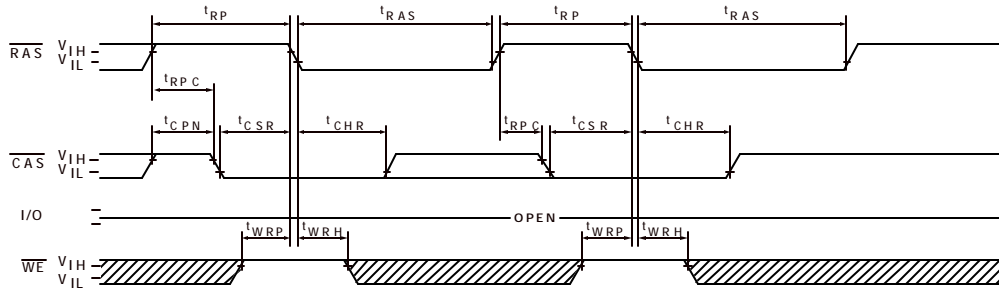


**RAS ONLY REFRESH CYCLE**  
(ADDR=A0-A10;  $\overline{OE}$ ,  $\overline{WE}$  =DON'T CARE)

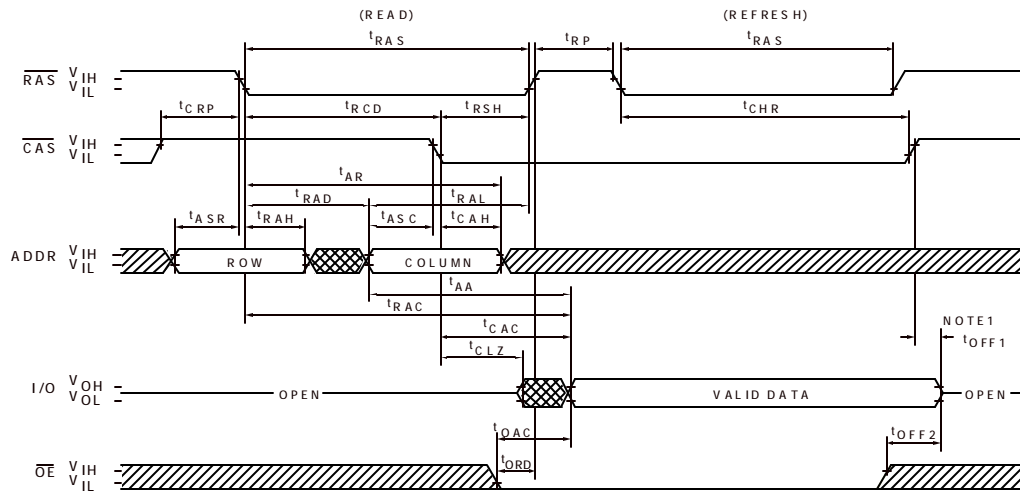


 DON'T CARE  
 UNDEFINED

**CBR REFRESH CYCLE**  
(A0-A10;  $\overline{OE}$  =DON'T CARE)

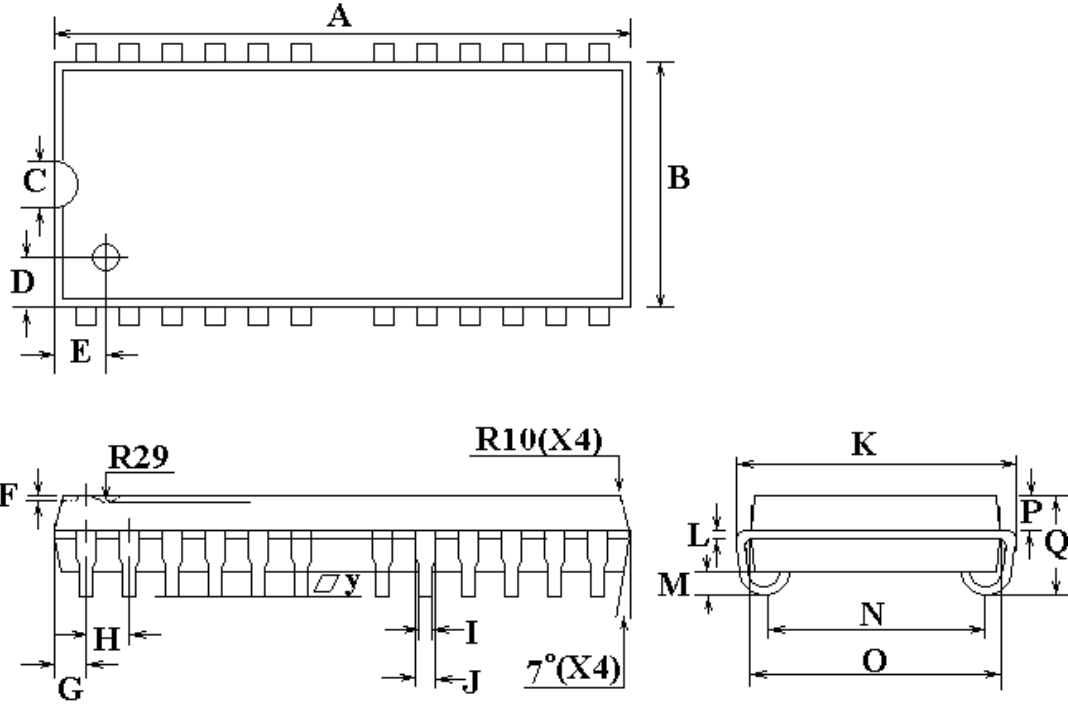


**HIDDEN REFRESH CYCLE**  
( $\overline{WE}$  =HIGH;  $\overline{OE}$  =LOW)



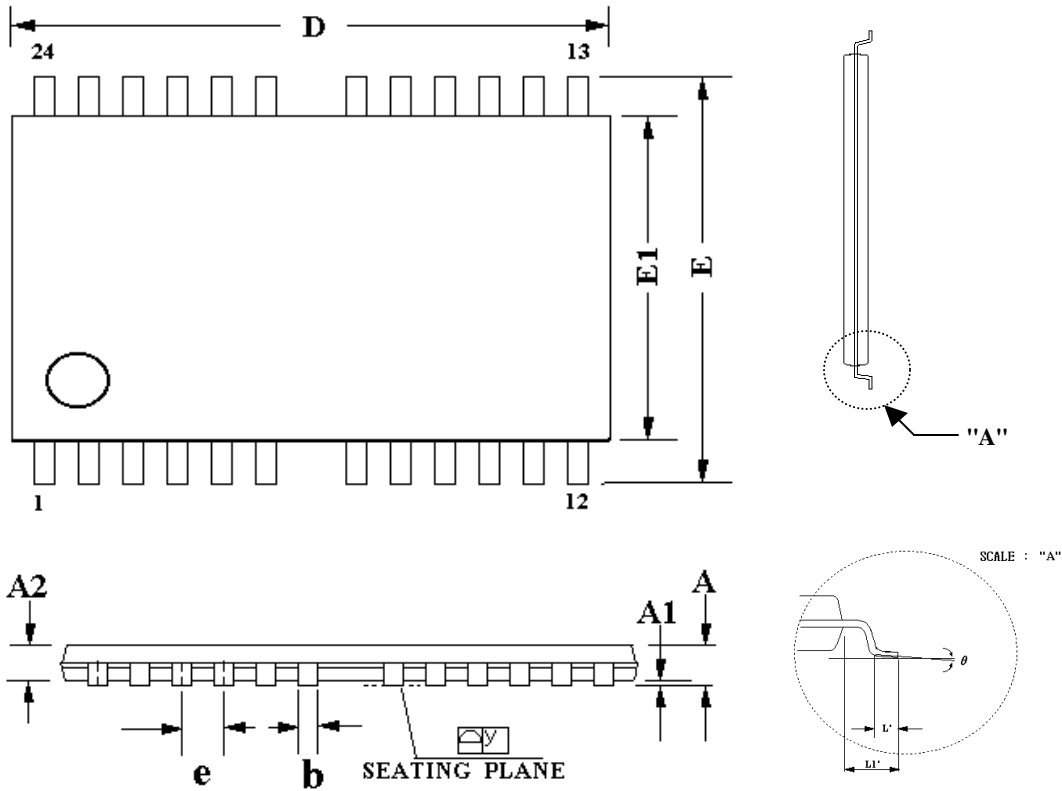
**Note:** 1.  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

**PACKAGE DIMENSIONS**  
**24-LEAD SOJ DRAM (300 mil)**



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.673±0.002	17.09±0.05
B	0.300±0.002	7.62±0.13
C	0.060±0.002	1.52±0.05
D	0.050±0.001	1.27±0.03
E	0.063±0.001	1.63±0.03
F	0.015±0.002	0.38±0.05
G	0.036±0.002	0.91±0.05
H	0.050±0.002	1.27±0.05
I	0.018±0.002	0.46±0.05
J	0.028±0.002	0.71±0.05
K	0.336±0.003	8.53±0.08
L	0.010±0.001	0.25±0.03
M	0.029±0.002	0.74±0.05
N	0.268±0.003	6.81±0.08
O	0.300±0.002	7.62±0.05
P	0.042±0.001	1.07±0.03
Q	0.129±0.004	3.28±0.10
y	0.004(MAX)	0.102(MAX)

**PACKAGE DIMENSIONS**  
**24-LEAD TSOP II DRAM (300 mil)**



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(MAX)	1.20(MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.016±0.004	0.41±0.11
D	0.675±0.005	17.14±0.13
E	0.368±0.003	9.22±0.20
E1	0.300±0.005	7.62±0.13
e	0.050	1.27
L'	0.020±0.004	0.50±0.10
L1'	0.031	0.80
y	0.002±0.002	0.05±0.05
$\theta$	1°~ 5°	1°~ 5°