

HD14516B

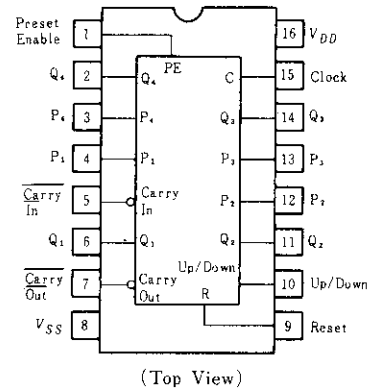
Binary Up/Down Counter

The HD14516B finds primary use where low power dissipation and/or high noise immunity is desired. This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

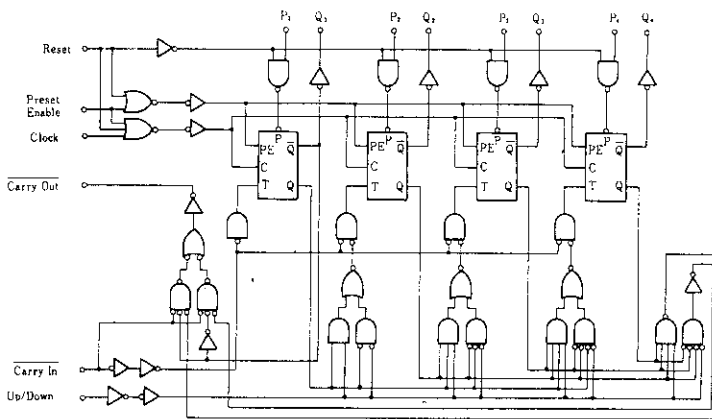
FEATURES

- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Internally Synchronous for High Speed
- Logic Edge-clocked Design ... Count Occurs on Positive Going Edge of Clock
- 6MHz Counting Rate (@10V)
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

PIN ARRANGEMENT



LOGIC DIAGRAM



TRUTH TABLE

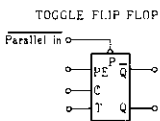
Carry In	Up/Down	Preset Enable	Reset	Action
1	x	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
x	x	1	0	Preset
x	x	x	1	Reset

x=Don't Care

Flip-flop Functional Truth Table

Preset Enable	Clock	Toggle Enable	Q _{n+1}
1	x	x	Parallel in
0	—	0	Q _n
0	—	1	Q̄ _n
0	—	x	Q _n

x=Don't Care



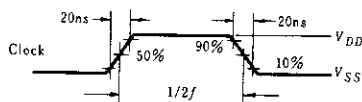
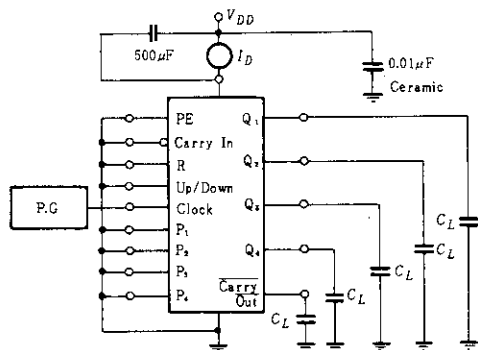
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	V _{OL}	V _{in} = V _{DD} or 0	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V _{OH}	V _{in} = 0 or V _{DD}	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage	V _{IL}	V _{out} = 4.5 or 0.5V	5.0	—	1.5	—	2.25	1.5	—	1.5	V
		V _{out} = 9.0 or 1.0V	10	—	3.0	—	4.50	3.0	—	3.0	
		V _{out} = 13.5 or 1.5V	15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	V _{out} = 0.5 or 4.5V	5.0	3.5	—	3.5	2.75	—	3.5	—	V
		V _{out} = 1.0 or 9.0V	10	7.0	—	7.0	5.50	—	7.0	—	
		V _{out} = 1.5 or 13.5V	15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I _{OH}	V _{OH} = 2.5V	5.0	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		V _{OH} = 4.6V	5.0	-0.2	—	-0.16	-0.36	—	-0.12	—	
		V _{OH} = 9.5V	10	-0.5	—	-0.4	-0.9	—	-0.3	—	
		V _{OH} = 13.5V	15	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I _{OL}	V _{OL} = 0.4V	5.0	0.52	—	0.44	0.88	—	0.36	—	mA
		V _{OL} = 0.5V	10	1.3	—	1.1	2.25	—	0.9	—	
V _{OL} = 1.5V		15	3.6	—	3.0	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.3	—	±0.0001	±0.3	—	±1.0	μA	
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current	I _{DD}	Zero Signal, per Package	5.0	—	20	—	0.005	20	—	150	μA
		10	—	40	—	0.010	40	—	300		
		15	—	80	—	0.015	80	—	600		
Total Supply Current*	I _T	Dynamic + I _{DD} , C _L = 50pF	5.0	—	—	—	0.58	—	—	—	μA
		f = 1 kHz,	10	—	—	—	1.2	—	—	—	
		per Gate	15	—	—	—	1.7	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

© V_{DD} = 5.0V I_T = (0.58μA/kHz)f + I_{DD} © V_{DD} = 10V I_T = (1.2μA/kHz)f + I_{DD} © V_{DD} = 15V I_T = (1.7μA/kHz)f + I_{DD}

POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

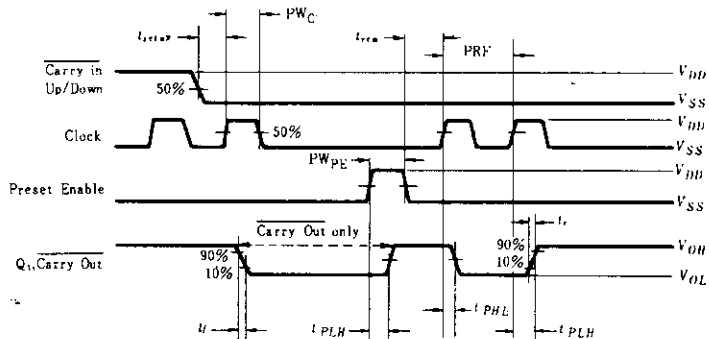


■SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

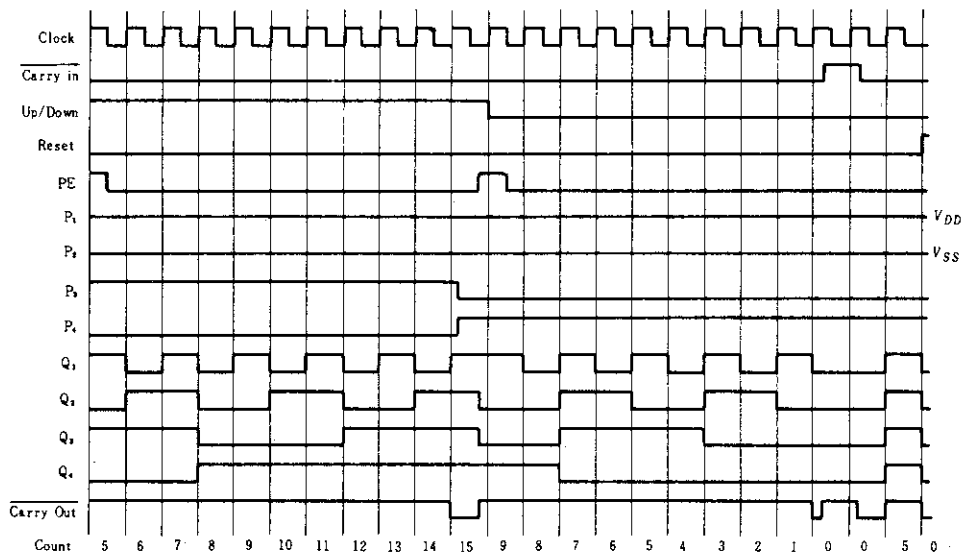
Characteristic		Symbol	V_{DD} (V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	360	ns
			10	—	90	180	
			15	—	65	130	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Clock-to-Q	t_{PLH} t_{PHL}	5.0	—	315	630	ns
			10	—	130	260	
			15	—	100	200	
	Clock-to-Carry Out		5.0	—	315	630	
			10	—	130	260	
			15	—	100	200	
	Carry In-to-Carry Out		5.0	—	180	360	
			10	—	80	160	
			15	—	60	120	
	Preset or Reset-to-Q		5.0	—	315	630	
			10	—	130	360	
			15	—	100	300	
Preset or Reset-to-Carry Out	5.0	—	550	1100			
	10	—	225	450			
	15	—	150	300			
Clock Pulse Width		PW_C	5.0	400	200	—	ns
			10	200	100	—	
			15	150	75	—	
Clock Frequency		PRF	5.0	—	3.0	1.5	MHz
			10	—	6.0	3.0	
			15	—	8.0	4.0	
Preset or Reset Removal Time*		t_{rem}	5.0	650	325	—	ns
			10	230	115	—	
			15	180	90	—	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Carry In Setup Time		t_{setup}	5.0	260	130	—	ns
			10	120	60	—	
			15	100	50	—	
Up/Down Setup Time	5.0		500	250	—		
	10		200	100	—		
	15		150	75	—		
Preset Enable Pulse Width		PW_{PE}	5.0	200	100	—	ns
			10	100	50	—	
			15	80	40	—	

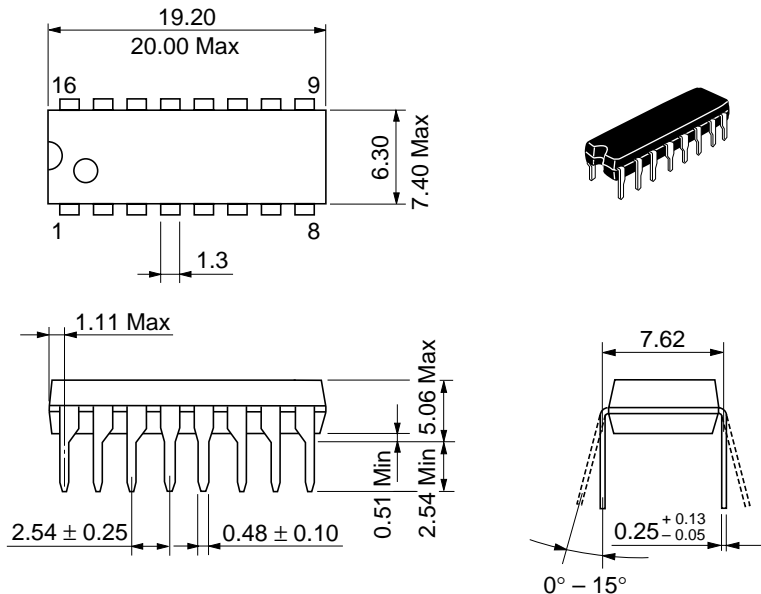
*The Preset or Reset Signal must be low prior to a positive-going transition of the clock.

■ DYNAMIC SIGNAL WAVEFORMS

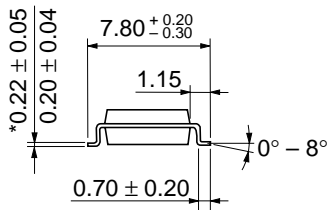
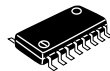
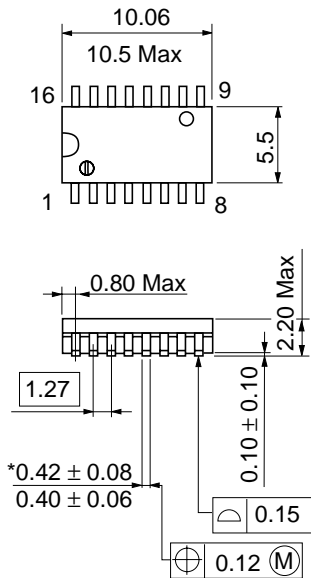


■ TIMING DIAGRAM



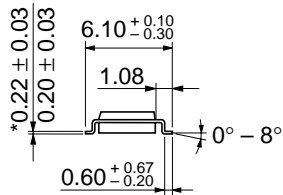
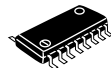
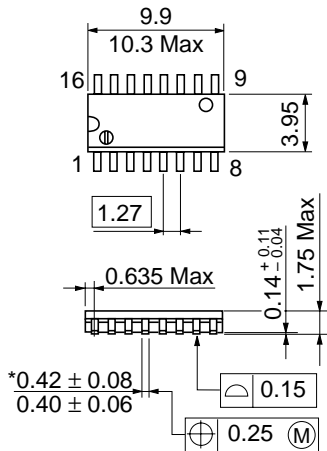


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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