TOKO

TK84819

POWER FACTOR CONTROLLER PWM COMBO

FEATURES

- Reduced Overall Current Consumption
- Reduced Start-Up Current
- Slow Start Following Current Limit Shutdown
- Boost Mode Power Factor Control
- Current or Voltage Mode PWM
- Peak or Average Current Sensing PFC Control
- Typical Power Factor > .996
- Current Limit and Over Voltage Protection
- Programmable Ramp Compensation
- Electrostatic Discharge Protection
- Pin Compatible with the ML4819

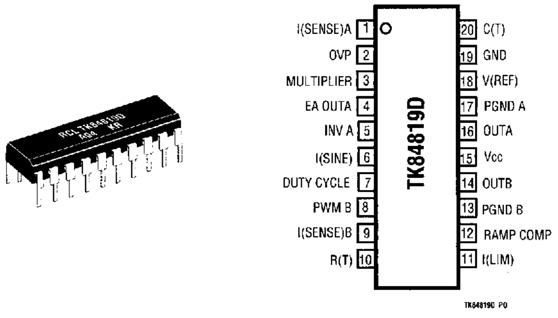
APPLICATIONS

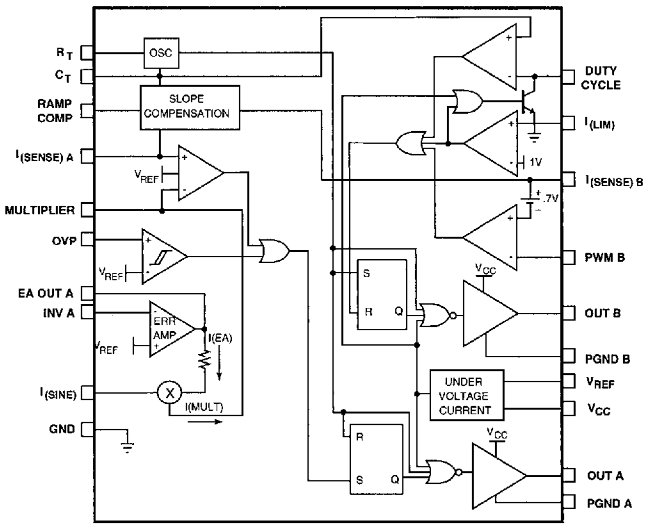
- Switching Power Supplies with PFC
- Computers
- Work Stations
- Telecommunications Equipment
- Office Equipment
- Medical Electronics
- IEC-555 Power Supplies

DESCRIPTION

The TK84819 is a complete boost mode Power Factor Control (PFC) circuit which also includes a PWM controller. The PFC circuit and PWM controller share the same oscillator and are synchronized. The outputs of the controller provide high current (>1 A peak) and high slew rate for excellent control of MOSFET gates. The PFC section utilizes peak current sensing control circuitry, with a current sense transformer or a SENSE FET device as a sense element. This non-dissipative method of current sensing improves overall efficiency. The PWM section includes cycle by cycle current limiting, precise duty cycle limiting for single ended converters, and slope compensation. Special care has been taken to provide high system noise immunity. The device has under voltage lockout circuitry with 6 V hysteresis, wide common mode range current sense comparators and precision duty cycle limiting circuit for the PWM section.

TK84819





ORDERING INFORMATION

TK84819 □ □ □□

- Tape/Reel Code
- Temp. Range
- Package Code

PACKAGE CODE	TEMP. RANGE	TAPE/REEL CODE
D : DIP-20	C : -20 to +70 °C	BX : Bulk/Bag
J : CERDIP-20	I : -40 to +85 °C	MG: Magazine

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... 35 V
Output Current, Source or Sink (Pin 14,16) DC....... 1.0 A
Output Energy (Capacitive Load Per Cycle)............. 5 µj
Multiplier I(SINE) Input Pin 6 .... 1.2 mA
Analog Inputs ....-0.3 V to 5.5 V
Storage Temperature Range.................... -65 to +150 °C

Operating Temperature Range
(Commercial)... -20 to +70 °C
(Industrial) .... -40 to +85 °C
Lead Soldering Temp. (10 sec.) .... 260 °C
Junction Temperature ....150 °C
Thermal Resistance, Plastic Dip..........................65 °C/W

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 15 V (Note 2), R_T = 14 kΩ, C_T = 1000 pF, T_A= Operating Temperature Range.

SYMBOL	PARAMETER	TEST CONDITION	TK84819C			TK84819I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator									
$f_{INTL(OSC)}$	Initial Accuracy	T_J = 25 °C	90	97	104	90	97	104	kHz
$\Delta f_{V(OSC)}$	Voltage Stability	12 V< V_{CC} < 25 V		3.0			3.0		%
$\Delta f_{T(OSC)}$	Temperature Stability			6			6		%
$\Delta f_{(OSC)}$	Total Variation	Temp	84		110	84		110	kHz
$V_{RV\ (OSC)}$	Ramp Valley			.9			.9		V
$V_{RP(OSC)}$	Ramp Peak			4.3			4.3		V
$V_{RT(OSC)}$	R(T) Pin Voltage		4.7	5.0	5.3	4.7	5.0	5.3	V
$I_{D(OSC)}$	Discharge Current	T_J = 25 °C, $V_{PIN\ 20}$ = 2 V	7.5	8.4	9.3	7.5	8.4	9.3	mA
	(Pin 10 open)	$V_{PIN\ 20}$ = 2 V	7.0	8.4	10.0	7.0	8.4	10.0	mA
Duty Cycle Comp.									
$V_{OS(DCC)}$	Input Offset Voltage		-15		+15	-15		+15	mV
$I_{B(DCC)}$	Input Bias Current			-0.7	-10		-0.7	-10	µA
$\partial_{(DCC)}$	Duty Cycle	$V_{PIN\ 7} = V_{REF}/2$	39	45	51.5	39	45	51.5	%
Reference Section									
$V_{(REF)}$	Output Voltage	I_O = 1 mA, T_J = 25 °C	4.9	5.00	5.10	4.90	5.00	5.10	V
$LI_{REG(REF)}$	Line Regulation	12 V < V_{CC} < 25 V		2	45		2	65	mV
$LD_{REG(REF)}$	Load Regulation	1 mA < I_O < 20 mA		8	35		8	40	mV
$\Delta V_{T(REF)}$	Temperature Stability			0.4			0.4		%
$\Delta V_{TOT(REF)}$	Total Variation	Line, Load, Temp	4.85		5.15	4.75		5.25	V
$V_{N(REF)}$	Output Noise Voltage	10 Hz to 10 kHz		50			50		µV
$V_{LT(REF)}$	Long Term Stability	T_J = 125 °C, 1000 hrs. (Note 1)		5	25		5		mV
$I_{SC(REF)}$	Short Circuit Current	V_{REF} = 0 V	-30	-85	-180	-25	-85	-185	mA
Error Amp Section									
$V_{OS(EA)}$	Input Offset Voltage		-15		+15	-15		+15	mV
$I_{B(EA)}$	Input Bias Current	$V_{PIN\ 4} = V_{REF}$ = 25 mV		-0.1	-1.0		-0.1	-1.0	µA
$A_{V(OL,EA)}$	Open Loop Gain	1 V < $V_{PIN\ 4}$ < 5 V	60	90		55	90		dB
$PSRR_{(EA)}$	PSRR	12 V < V_{CC} < 25 V	50	75		50	75		dB

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the startup threshold first to activate the IC, then returned to 15 V.

ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: V_{CC} = 15 V (Note 2), R_T = 14 kΩ, C_T = 1000 pF, T_A= Operating Temperature Range.

SYMBOL	PARAMETER	TEST CONDITION	TK84819C			TK84819I			
			MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Error Amp Section (Cont.)									
$I_{SINK(EA)}$	Output Sink Current	$V_{PIN\ 4}$ = 1.1 V, $V_{PIN\ 5}$= 5.2 V	2	12		1.5	12		mA
$I_{SOURCE(EA)}$	Output Source Current	$V_{PIN\ 4}$ = 5.0 V, $V_{PIN\ 5}$ = 4.8 V	-0.5	-1.0		-0.35	-1.0		mA
$V_{OH(EA)}$	Output High Voltage	I_{PIN4} = -0.5 mA, $V_{PIN\ 5}$ = 4.8 V	6.5	7.0		6.3	7.0		V
$V_{OL(EA)}$	Output Low Voltage	$I_{PIN\ 4}$ = 1 mA, V_{PIN5} = 5.2 V		0.7	1.2		0.7	1.2	V
$BW_{(EA)}$	Unity Gain Bandwidth			1.0			1.0		MHz
Multiplier									
$V_{ISINE(M)}$	I(SINE) Input Voltage	I(SINE) = 500 µA	0.4	.7	0.9	0.35	0.7	1.1	V
$I_{OUT(M)}$	Output Current (Pin 3)	I(SINE) = 500 µA, Pin 5 = V_{REF} -20 mV	460	495	505	450	495	520	µA
		I(SINE) = 500 µA, Pin 5 = V_{REF} +20 mV		0	10		0	40	µA
		I(SINE) = 1 mA, Pin 5 = V_{REF} -20 mV	900	990	1025	900	990	1035	µA
BW(M)	Bandwidth			200			200		kHz
$PSRR_{(EA)}$	PSRR	12 V < V_{CC} < 25 V		70			70		dB
Slope Compensator									
$V_{R(SC)}$	RAMP COMP VPin 12			V_{PIN20}-1			V_{PIN20}-1		V
$I_{R(SC)}$	Iout Pin 1 or Pin 9	IPIN 12 = 100 µA (Note 3)	45	48	51	40	48	55	µA
OVP Comparator									
$V_{OS(OVP)}$	Input Offset Voltage	Output Off	-20		+30	-20		+30	mV
$V_{H(OVP)}$	Hysteresis		100	120	140	85	120	150	mV
$I_{B(OVP)}$	Input Bias Current		-0.3		-3.0	-0.3		-3.0	µA
$\Delta t_{(OVP)}$	Propagation Delay			150			150		ns
I(SENSE) Comparator									
$V_{CMR(SENSE)}$	Input CMR	$V_{PIN\ 5}$ = V_{REF} - 20 mV	-0.2		5.5	-0.2		5.5	V
$V_{OS(SENSE)}$	Input Offset Voltage	I(SENSE) A	-15		+15	-15		+30	mV
		I(SENSE) B	0.4	0.7	0.9	0.38	0.7	0.92	V
$I_{B(SENSE)}$	Input Bias Current			-0.7	-10		-0.7	-10	µA
$I_{OS(SENSE)}$	Input Offset Current		-1		+1				µA
$\Delta t_{(SENSE)}$	Propagation Delay			150			150		ns
$I_{LIM(SENSE)}$	I(limit A) Trip Point	$V_{PIN\ 3}$ = 5.5 V	4.75	5	5.25	4.75	5	5.25	V
I(LIM) Comparator									
$V_{TRIP(LIM)}$	I(limit) Trip Point		.94	1	1.06	.9	1	1.1	V
$I_{B(LIM)}$	Input Bias Current			-0.7	-10		-0.7	-10	µA
$\Delta t_{(LIM)}$	Propagation Delay			150			150		ns

ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: R_T = 14 kΩ, C_T = 1000 pF, T_A= Operating Temperature Range. V_{CC} = 15 V (Note 2)

SYMBOL	PARAMETER	TEST CONDITION	TK84819C			TK84819I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Section A, B									
$V_{OL(O)}$	Output Voltage Low	I_{OUT} = -20 mA		0.1	0.4		0.1	0.5	V
		I_{OUT} = -200 mA		1.6	2.3		1.6	2.3	V
$V_{OH(O)}$	Output Voltage High	I_{OUT} = 20 mA	12.5	13.5		12.5	13.5		V
		I_{OUT} = 200 mA	12	13.4		11.5	13.4		V
$V_{ULVO(O)}$	V_{OUT} Low in UVLO	I_{OUT} = -5 mA, V_{CC} = 8 V		0.65	0.8		0.65	1.0	V
$t_{R(O)}$; $t_{F(O)}$	Output Rise/Fall Time	C_L = 1000 pF		50			50		ns
Under Voltage Lockout									
$V_{ST(UVLO)}$	Start-Up Threshold		14.5	16	17.5	14.5	16	17.5	V
$V_{SD(UVLO)}$	Shut-Down Threshold		8.75	10	11.25	8.5	10	11.5	V
V_{REFG}	V_{REF} Good Threshold			4.4			4.4		V
Total Device									
I_{TOT}	Supply Current	Start-Up, V_{CC} = 14 V		0.27	0.5		0.27	0.6	mA
		Operating T_J = 25 °C		25	35		25	35	mA
		Op Temp		25	38		25	48	mA

Note 1: This parameter not 100% tested in production but guaranteed by design.
Note 2: V_{CC} is raised above the startup threshold first to activate the IC, then returned to 15 V.
Note 3: PWM comparator bias currents are subtracted from this reading.

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	I(SENSE)A	Input from the Current Sense Transformer to the PWM comparator (+). Current Limit occurs when this point reaches 5 V.
2	OVP	Input to the over voltage comparator.
3	MULTIPLIER	Output of the current multiplier. A resistor to ground on this pin converts the current to a voltage.
4	EA OUT A	Output error amplifier
5	INV A	Inverting input to error amplifier.
6	I(SINE)	Current multiplier input
7	DUTY CYCLE SOFT START	PWM controller duty cycle is limited by setting this pin to a fixed voltage. A capacitor to ground sets the soft start time constant.
8	PWM B	Error voltage feedback input.
9	I(SENSE) B	Input for current sense resistor for current mode operation or for oscillator ramp for voltage mode operation.
10	R(T)	Oscillator timing resistor pin. A 5 V source across this resistor sets the charging current for C(T)
11	I(LIM)	Cycle by cycle PWM current limit. Exeeding the 1 V threshold on this pin terminates the PWM cycle.

PIN DESCRIPTION (CONT.)

PIN #	NAME	FUNCTION
12	RAMP COMP	Buffered output from the Oscillator ramp (C(T)). A resistor to ground sets a current 1/2 of which is sourced on pins 9 and 1.
13	GND B	Return for the high current totem pole output of the PWM controller.
14	OUT B	PWM Controller totem pole output.
15	V_{CC}	Positive supply for the IC.
16	OUT A	PFC controller totem pole output.
17	GND A	Return for the high current totem pole output of the PFC controller.
18	V_{REF}	Buffered output for the 5V voltage reference.
19	GND	Analog Signal Ground.
20	C(T)	Timing capacitor for the oscillator.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The TK84819 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, the clock pulse is high.

The Oscillator period can be described by the following relationship: $T_{OSC} = T_{RAMP} + T_{DEADTIME}$

where: $$T_{RAMP} = \frac{C_V \times V_\Delta}{I_{SET}}$$

and: $$T_{DEADTIME} = \frac{C_V \times V_\Delta}{8.4\text{ mA} - I_{SET}}$$

The maximum duty cycle of the PWM section can be limited by setting a threshold on pin 7. When the (C_T) ramp is above the threshold at pin 7, the PWM output is held off and the PWM flip-flop is set:

$$D_{LIMIT} = \frac{D_{OSC} \times (Y_{PIN7} - 0.9)}{3.4}$$

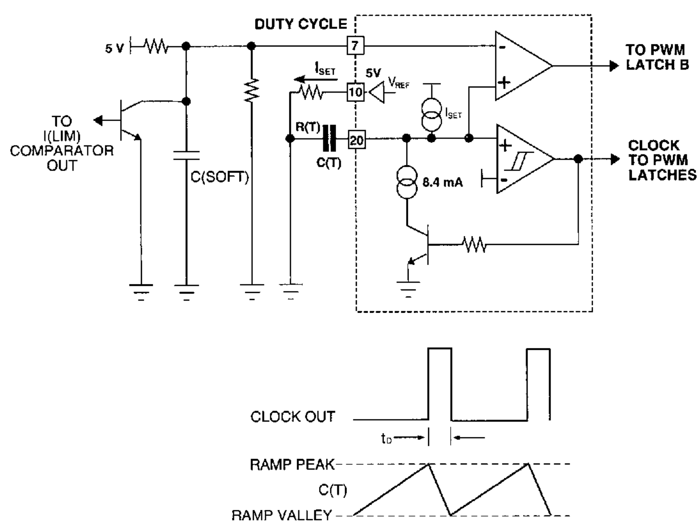


Figure 1. Oscillator Block Diagram

FUNCTIONAL DESCRIPTION (CONT.)

Where:

D_{LIMIT} = Desired duty cycle

D_{OSC} = Oscillator duty cycle

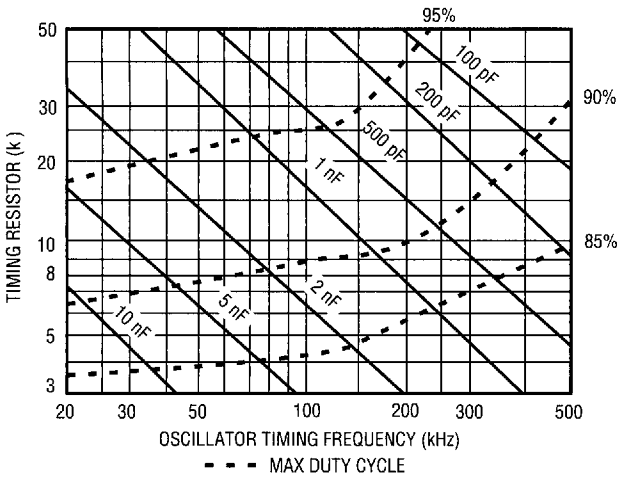


Figure 2. Oscillator Timing Resistance vs. Frequency

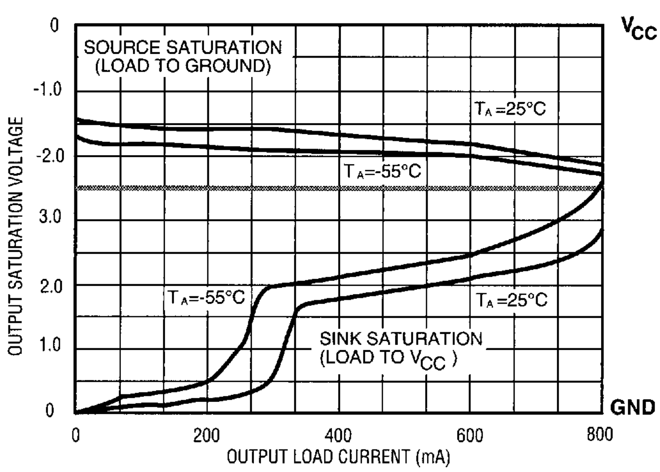


Figure 3. Output Saturation Voltage vs. Output Current

A capacitor from pin 7 to ground can be used for soft start when the current limit threshold (pin 11) is exceeded.

ERROR AMPLIFIER

The TK84819 error amplifier is a high open loop gain, wide bandwidth amplifier.

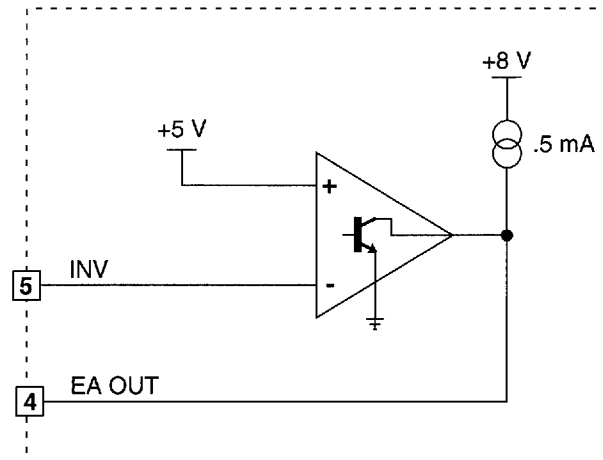


Figure 4. Error Amplifier

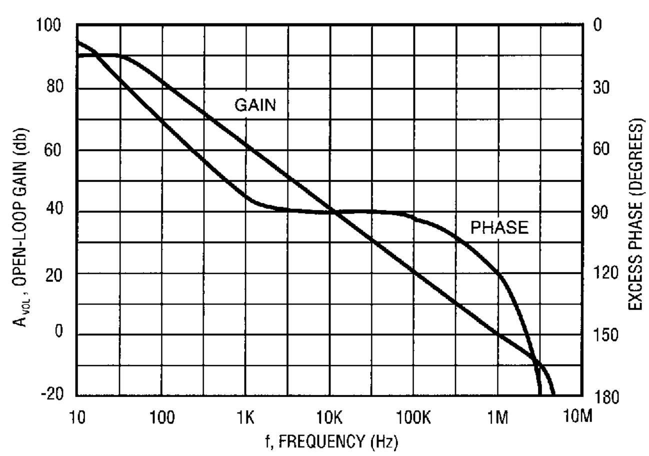


Figure 5. Error Amp Open-Loop Gain and Phase vs. Frequency

MULTIPLIER

The TK84819 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

FUNCTIONAL DESCRIPTION (CONT.)

The output of the multiplier is a current proportional to :

$$I_{OUT} \propto I(SINE) \times I(EA)$$

Where: I(SINE) is the current in the dropping resistor, and I(EA) is a factor which varies from 0 to 1 proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output (pin 3).

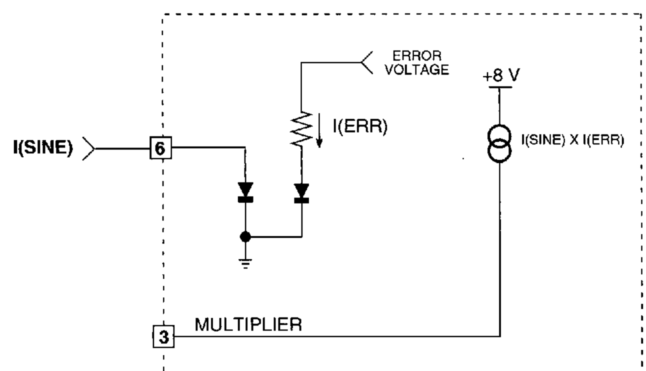


Figure 6. Multiplier Block Diagram

SLOPE COMPENSATION

Slope compensation is accomplished by adding 1/2 of the current flowing out of pin 12 to pin 1 (for the PFC section). The amount of slope compensation is equal to:

$$(I_{PIN12}/2) \times R_L$$

Where: R_L is the impedance to ground on pin 1 or pin 9. Since most of the PWM applications will be limited to 50% duty cycle, slope compensation should not be needed for the PWM section. This can be defeated by using a low impedance load to the current sense on pin 9.

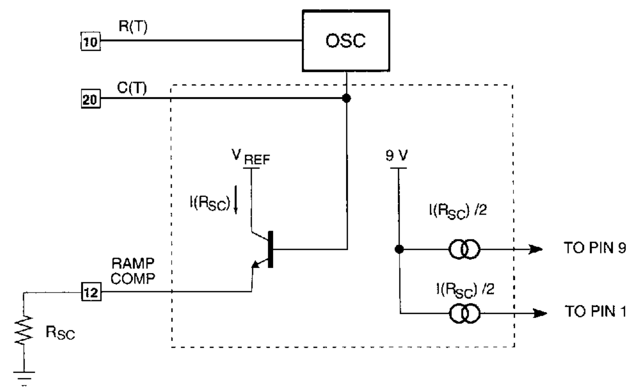


Figure 7. Slope Compensation

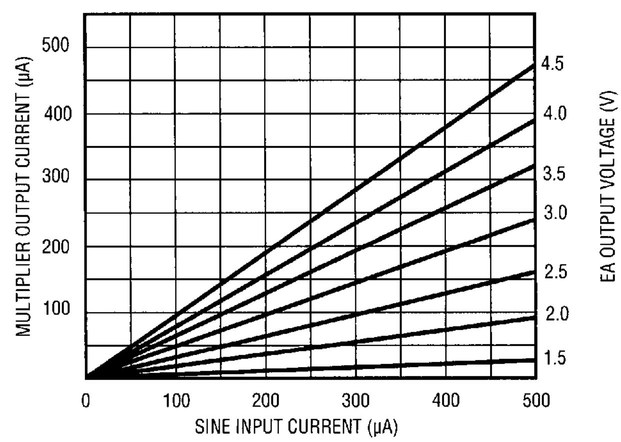


Figure 8. Multiplier Linearity

UNDER VOLTAGE LOCKOUT

On power up the TK84819 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16 V. When V_{CC} drops below 10 V, the UVLO condition is imposed. During the UVLO condition, the 5 V V_{REF} pin is "off", making it usable as a "flag".

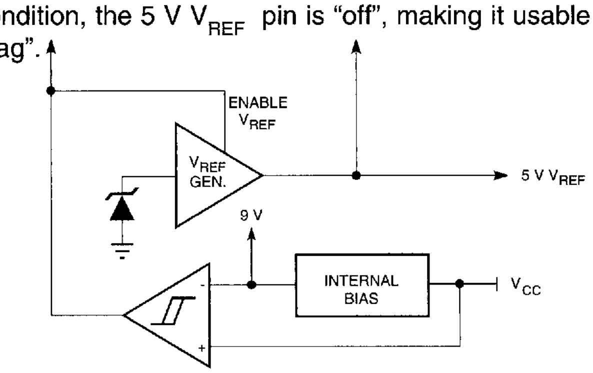


Figure 9. Under Voltage Lockout

TYPICAL APPLICATIONS

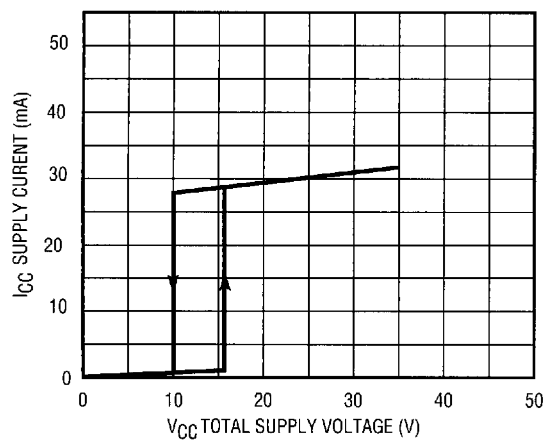


Figure 10. Total Supply Current vs. Supply Voltage

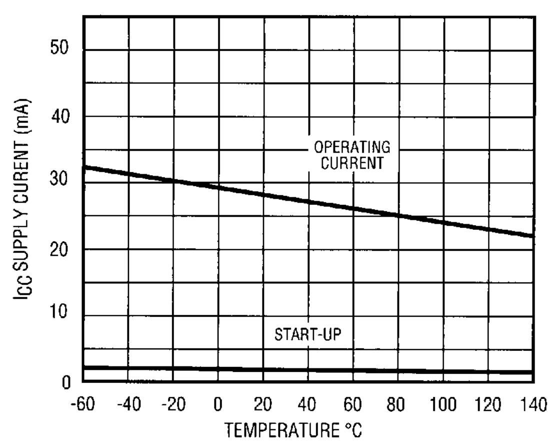


Figure 11. Total Supply Current vs. Temperature

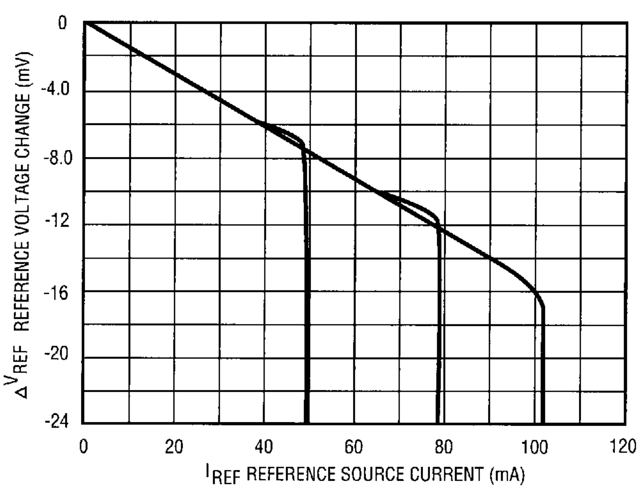


Figure 12. Reference Load Regulation

POWER FACTOR SECTION

The power factor section is a boost mode pre-regulator that provides approxamately 380 volts DC for the PWM section. It utilizes peak current sensing to give a typical corrected power factor of .996 over all load conditions. The following calculations refer to the applications circuit. (The component designators in the equations below refer to components in the application circuit.)

$$R_T = R15,\ C_T = C6$$

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, for a given operating current, the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size. One more condition where the inductor can dry out is analyzed below, where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}}$$

Where D_{ON} is the duty cycle $(T_{ON}/(T_{ON} + T_{OFF})$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON})$$

$$V_{INDRY} = (1 - D_{ON\,(max)}) \times V_{OUT}$$

V_{INDRY}: Voltage where the inductor dries out

V_{OUT} : Output DC Voltage

TYPICAL APPLICATIONS (CONT.)

The previous relationship shows that the resetting volt-seconds are more than setting volts-seconds. In energy transfer terms, this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out. The recommended maximum duty cycle is 95% at 100 kHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: $V_{OUT} = 380$ V and

$D_{ON\,(max)} = 0.95$

then substituting in (3) yields $V_{INDRY} = 20$ V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN(min)\ PEAK} = \frac{1.414 \times P_{IN(min)}}{V_{IN(max)}}$$

$V_{IN(max)} = 260$ V

$P_{IN(min)} = 50$ W

then: $I_{IN(min)} = 0.272$A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in Step 1 was chosen.

then:

$I_{LDRY} = 100$ mA

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON(max)}}{L_{INDRY} \times f_{OSC}}$$

$$= \frac{20\text{ V} \times 0.95}{100\text{ mA} \times 100\text{ kHz}} = 2\text{ mH}$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200 W is the T157-18 made by Micrometals. Two of these toroids are stacked with 140 turns of AWG #20 to provide 2 millihenries at 2 amps DC.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36.}{R_T\ C_T}$$

TYPICAL APPLICATIONS (CONT.)

For example:

Step 1: At 100 kHz with 95% duty cycle T_{OFF} = 500 ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} X I_{DIS}}{V_{OSC}} = 1000 \text{ pf}$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} X C_T} = \frac{1.36}{100 \text{ kHz} X 1000 \text{ pF}} = 13.6 \text{ k}$$

Choose R_T = 14 k

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the TK84819 is provided internally. A current equal to $V_{C(T)}$/2(R18) is added to I(SENSE) A (pin 1). This is converted to a voltage by R10, adding slope to the sensed current through T1. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time as reflected on pin 1. Note that slope compensation is a requirement only if the inductor current is continuous and the duty cycle is more than 50%. The highest inductor downslope is found at the point of inductor discontinuity:

$$\frac{d_L}{d_t} = \frac{V_b - V_{INDRY}}{L} = \frac{380 \text{ V} - 20 \text{ V}}{2 \text{ mH}}$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_b - V_{INDRY}}{L1} X \text{ R11/Nc}$$

Where NC is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. We have used a standard Beckman Industrial HM31-20100 current sense transformer. The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75 mA average. Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the IC.

The value of ramp compensation (SC_{PWM}) as seen at pin1 is:

$$SC_{PWM} = \frac{2.5 X R9}{R15 x C6 X R18}$$

The required value for R18 can be found by:

$$SC_{PWM} = A_{SC} X S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R18

The value of R9 (pin 2) depends on the selection of R2 (pin 6)

$$R2 = \frac{V_{IN(max) PEAK}}{I_{sine(PEAK)}} = \frac{260 X 1.414}{0.72 \text{ mA}} = 510 \text{ k}$$

$$R9 > \frac{V_{CLAMP} X R2}{V_{IN(min)}} = \frac{4.8 X 510 \text{ k}}{80 X 1.414} \quad 22 \text{ k}$$

Choose R9 = 27K

The peak inductor current can be found approximately by:

$$II_{PEAK} = \frac{1.414 X P_{OUT}}{V_{IN(min)RMS}} = \frac{1.414 X 200}{90} = 3.14 \text{ A}$$

The selection of Nc which depends on the maximum switch current, assume 4A for this example is 80 turns,

$$R11 = \frac{V_{CLAMP} X Nc}{I_{PEAK}} = \frac{4.8 X 80}{4} \approx 100 \text{ Ohms}$$

Where R11 is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. The

TYPICAL APPLICATIONS (CONT.)

clamp is internally set to 5 V. In actual application it is a good idea to assume a value less than 5 V to avoid unwanted current limiting action due to component tolerances. In the application V_{CLAMP} was chosen as 4.8 V.

Having calculated R11 the value S_{PWM} and of R18 can now be calculated:

$$S_{PWM} = \frac{380\text{ V} - 20}{2\text{ mH}} \times \frac{100}{80} = 0.225\text{ V/}\mu\text{s}$$

$$R18 = \frac{2.5 \times R9}{A_{SC} \times S_{PWM} \times R_T \times C_T}$$

$$R18 = \frac{2.5 \times 27\text{k}}{0.7 \times (.225 \times 10^6) \times 14\text{k} \times 1\text{nf}} \approx 30\text{ k}$$

Choose R18 = 33 k

The following values were used for calculation:

R9 = 27 k
Asc = 0.7
Rt = 14 k
Ct = 1 nF

VOLTAGE REGULATION COMPONENTS

The value of the regulation loop components are calculated based on the operating output voltage. Note that safety regulations require the use of sense resistors that have adequate voltage rating. As a rule, if 1/4 watt resistors are available, two should be used in series. The input bias current of the error amplifier is approximately 0.5 µA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4 watt resistors have to be used, the total power rating is 1/2 W. The operating power is set to be 0.4 W, then with 380 V output voltage, the value can be calculated as follows:

$R5 = (380V)^2/0.4\text{ W} = 360\text{ k}$

Therefore choose two 178 k 1/4 W 1% resistors connected in series.Then R6 can be calculated as follows:

$$R6 = \frac{V_{REF} \times R5}{V_B - V_{REF}} = \frac{5\text{ V} \times 357\text{ k}}{380\text{ V} - 5\text{ V}} = 4.76\text{ k}$$

Choose 4.75 k 1%

One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120 Hz ripple which is present at the output. If this ripple is not adequately attenuated, it will cause distortion of the input current waveform. Typical bandwidths range anywhere from a few Hz to 15 Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C8 = \frac{1}{3.142 \times R5 \times BW} =$$

$$C8 = \frac{1}{3.162 \times 357\text{ k} \times 2\text{ Hz}} = 0.45\text{ }\mu\text{F}$$

OVERVOLTAGE PROTECTION (OVP)

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395 V.

By choosing the high voltage side resistor of the OVP circuit the same way as above, (R7 = 356 k) then R8 can be calculated as:

$$R8 = \frac{V_{REF} \times R7}{V_{OVP} - V_{REF}} = \frac{5\text{ V} \times 357\text{ k}}{395\text{ V} - 5\text{ V}} = 4.576\text{ k}$$

Choose 4.53 k 1%

Note that R5, R6, R7, and R8 should be 1% or better tolerance.

TYPICAL APPLICATIONS (CONT.)

OFF- LINE START-UP AND BIAS SUPPLY GENERATION

The start-up circuit can either be a "bleed resistor" type (39 k,2 W) or the circuit shown at right. The bleed resistor method offers the advantage of simplicity and lowest cost, but may cause excessive turn-on time at low line voltage.

When the voltage on V_{CC} (pin 15) exceeds 16 V, the IC starts up. The energy stored on C10 supplies the IC with running power until the supplemental winding on the output transformer can provide power to sustain operation.

PWM SECTION

The PWM section uses current mode control. Current is sensed through R24 and filtered for high frequency noise and leading edge transients by R23 and C14. The main regulation loop is through PWM B. The TL431 in the secondary serves as both a voltage reference and error amplifier, with isolation provided by an opto-coupler which give a current command signal on pin 8. Loop compensation is provided by R29 and C20. The output voltage is set by:

$$V_{OUT} = 2.5 \times \left(1 + \frac{R29}{R28}\right)$$

The control loop is compensated using standard techniques.

Current is limited to a threshold of 2A(1 V on R24). The duty cycle is limited in this circuit to below 50% to prevent output transformer core saturation. The maximum duty cycle limit of 45% is set using a threshold of $V_{REF}/2$ on pin 7.

The circuit can be modified for voltage mode operation by using the slope current that appears on pin 9.

The ramp amplitude appearing on pin 9 can be shown as:

$$V_R = \frac{I(R18)}{2} \times R(V)$$

where R18 is the slope compensation resistor. Since this circuit operates with a constant input voltage, (as provided by the PFC section), voltage feed-foward is unnecessary.

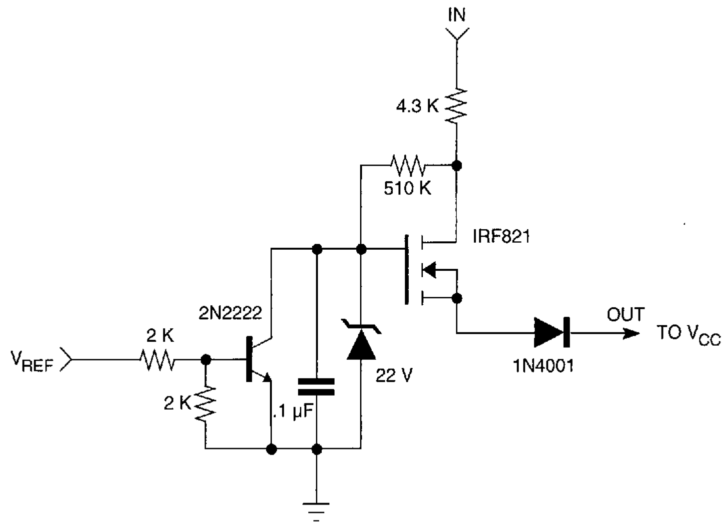


Figure 13. Start-Up Circuit

MODIFYING THE 180 WATT APPLICATION BOARD FOR AVERAGE-CURRENT-MODE POWER FACTOR CORRECTION

Modifications from Peak Current Control

The distinction between the presently proposed average current control technique and that of devoted average current control ICs is the presence (or lack thereof, in the present proposal) of a current amplifier. However, a current amplifier is not necessary to implement average current control nor the corresponding improvement of line current distortion and power factor brought about by average current control. Using the following technique developed by Toko, the TK84819 can successfully perform average current control. While both the power factor correction converter and the DC-DC converter are current-controlled, it is only the prior converter which is converted to average current control. The schematic change from the peak-current-controlled power supply reflects a change in the typically-used current sensing method and in the optimal pre-distortion requirement. For more detailed differentiation between the two control modes in this power supply application, Toko offers application note AN-9301.

Here is a summary of the changes which have been implemented in the supply:

1) The current sensing has been changed from a transformer to a resistor;
2) The pre-distortion circuitry has been changed substantially;
3) The current sense signal to the IC is now filtered and is applied to the multiplier output pin, pin 3;
4) Pin 1 of the IC labeled "I(SENSE)A" is grounded through a resistor and no longer serves as a current sensing node, but only as a slope compensation reference for the current signal seen at the multiplier output pin.

The previous pre-distortion circuitry was optimized for removing the non-linearities inherent when controlling the peak current rather than the average current. With average current control there is now only a slight non-linearity due to the ripple on the filtered current sense signal. The pre-distortion circuitry can be softened substantially. An error-voltage-dependent pre-distortion circuit recently developed by Toko provides the softer and more precise distortion. For a detailed analysis of various distortion reducing methods the reader is referred to a paper presented by Toko at APEC '94: Reducing Distortion in Peak-Current-Controlled Boost Power Factor Correctors, Conference Proceedings (p. 576).

How the Modifications Work

With respect to the control ground, the voltage developed at the negative of the input bridge is a cycle-by-cycle negative-polarity current signal of the power factor correction boost converter input current. C26 serves to keep the low frequency current signal, which represents the average current, unattenuated. At approximately the frequency set by C26 and R47 (~10 kHz) the current signal is attenuated. About a decade higher up in frequency the attenuation is held constant at about -20 dB. This means that the switching frequency (100 kHz) current signal and its higher frequency components are attenuated by 20 dB. Therefore, the distortion effect of the high frequency ripple is also attenuated.

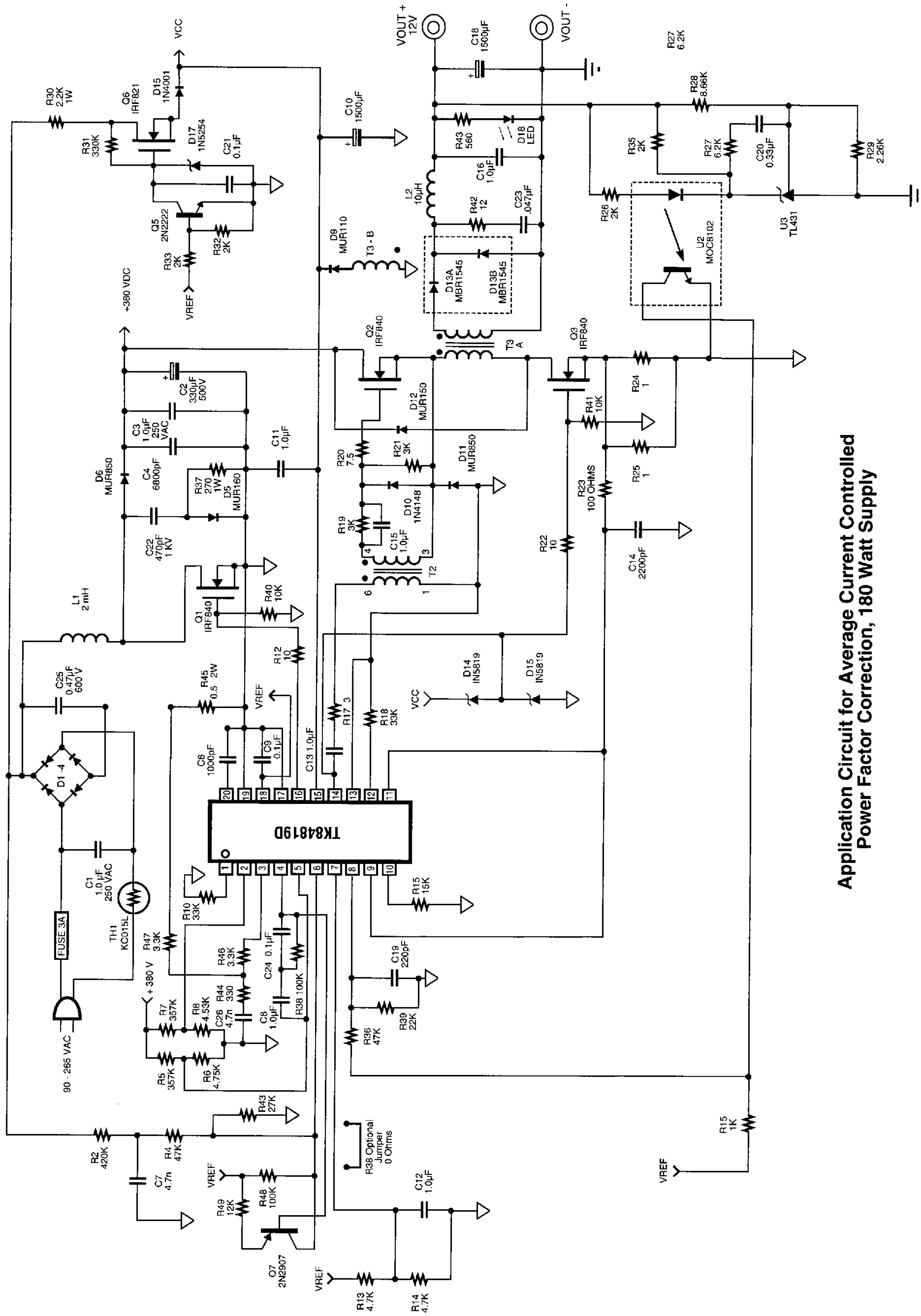
It is important to note that the preceding description is equally valid for that which has come to be known as "average current control" and for which the user is used to requiring a current-signal amplifier. All that really distinguishes average current control from peak current control is a frequency-dependent processing of the current signal - whether or not an amplifier is involved in the process. Likewise, it must be acknowledged that without an amplifier the noise sensitivity of the current-signal input is increased because of the attenuated signal level. Thus, it is important to observe good printed-wiring-board layout techniques. Also, since the line current distortion reduction relates directly to the gain difference between low and high frequencies, and since without an amplifier the low frequency gain is limited to 0 dB, the user must determine for a given power supply what is the acceptable tradeoff between distortion caused by low attenuation and noise caused by high attenuation. Emperical results tell us that an acceptable tradeoff can indeed be found.

Returning to the explanation of how the current signal is processed, the multiplier output is a current which is developed across the R9, and this voltage remains fairly constant over a cycle due to the low frequency characteristic of all of the multiplier input signals. In this configuration, the multiplier output voltage rides atop the negative-polarity filtered current sense signal. The PFC PWM comparator switches off the drive when the filtered current sense signal goes far enough negative to pull the multiplier input down to ground each cycle.

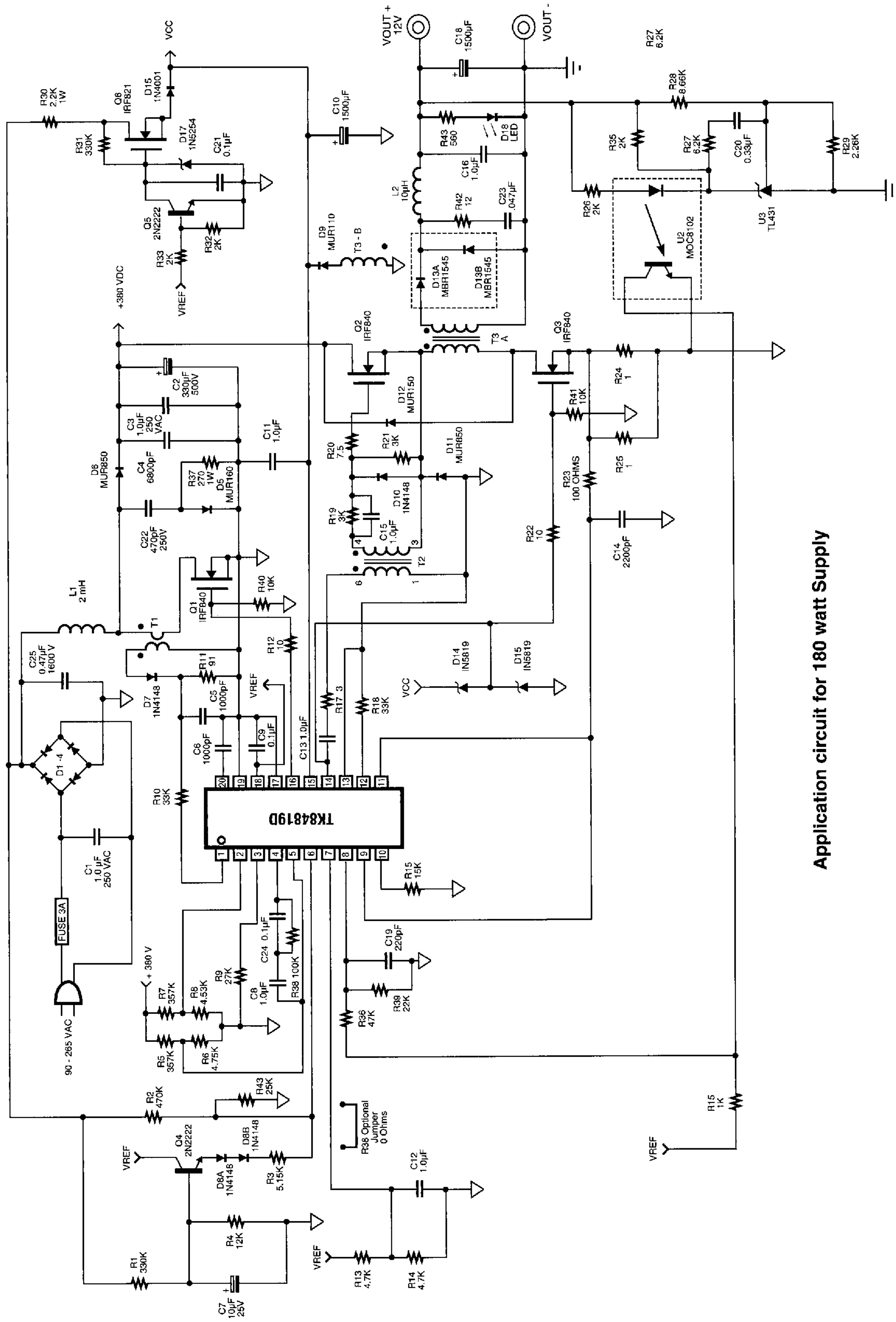
Conclusions

For the person who wishes to experiment with the average current control technique presented herein, it is important to clarify that the pre-distortion circuit used to improve the characteristics of the peak current control technique was not optimized for this supply. It has been verified that with a 10-to-1 attenuation of the current signal, the noise performance can be made quite good without placing undue burden on the layout. Nonetheless, it must also be stated that the current-signal filter is not optimized either - although optimization will depend on the user in this situation where noise susceptibility is largely a function of the environment.

A simplified version of average current control gives the power factor converter design engineer the option to use a peak current control IC while still attaining the prime benefits of average current control. This presents the opportunity for greater cost-effectivity and versatility. A line current waveform well within the IEC555 harmonic limits can be attained. This control technique is granted for unrestricted use and development exclusively to power supply manufacturing firms.



Application Circuit for Average Current Controlled Power Factor Correction, 180 Watt Supply



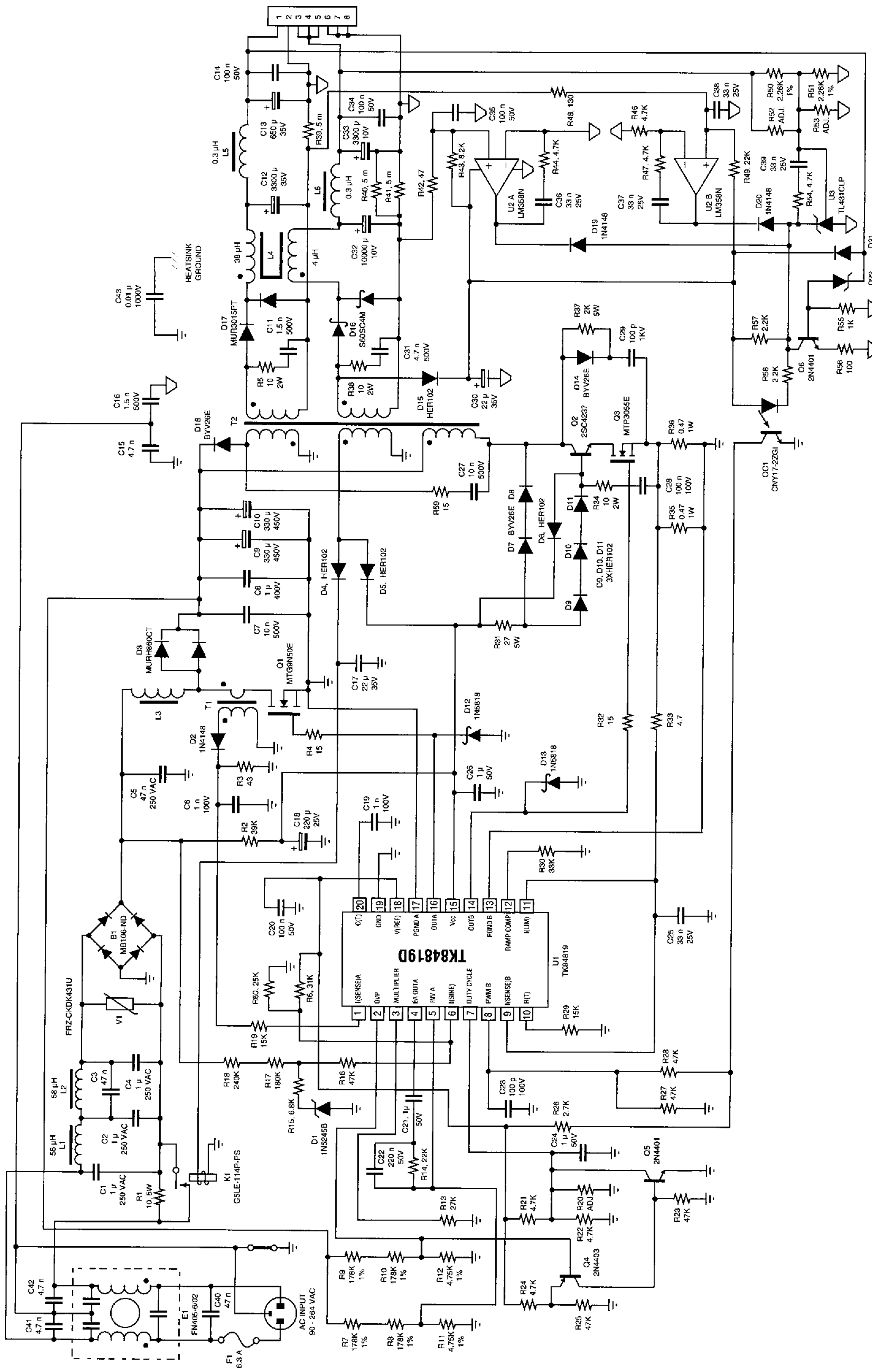
Application circuit for 180 watt Supply

180 WATT APPLICATIONS CIRCUIT PARTS LIST

ITEM	DESCRIPTION	MANUFACTURER	PART NO.
U1	TK84819	Toko	
U2	MOC8100	Motorola	
U3	TL431	Texas Instr.	
Q1 - Q3	IRF840	Interntl. Rectifier	
Q4, Q5	2N2222		
Q6	IRF821	Interntl. Rectifier	
Q7	2N2907		
D1 - 4	KBU8J Bridge Rectifier	G.I.	
D5	MUR160	Motorola	
D6	MUR850	Motorola	
D7, D8A, D8B, D10	1N4148		
D9	MUR110	Motorola	
D11, D12	MUR150	Motorola	
D13A,B	MBR1545	Motorola, G.I.	
D14, D16	1N5819		
D15	1N4001		
D17	IN5254		
D18	LED		
C1, C3	1 µF, 250 VAC		
C2	330 µF, 450 V		
C4	6.8 NF, 1 kV, Ceramic		
C5, C6	1000 pF		
C7	10 µF, 25 V	Panasonic	
C8, C15	1 µF, 35 V, Non-polarized		
C9, C21	0.1 µF, 50 V, Ceramic		
C10	1500 µF,25 V, Electrolytic	Illinois Capacitor	158CKR025M
C11 - C13, C16, C17	1 µF, Ceramic		
C14	2,000 pF, 50 V		
C18	1500 µF,16 V, Electrolytic	Illinois Capacitor	158CKR016M
C19	220 pF, 50 V		
C20	0.33 µF, 50 V		
C22	470 pF, 1 kV		
C23	.047 µF, 1 kV		
C24	0.1 µF, 50 V		
C25	0.47 µF, 250 VAC	Panasonic	
C26	0.01 µF, 50 V		
L1	2 mH, Ipeak=4 A Core: Powdered Iron toroid CTM-23891	CTM Magnetics 1419 W. 12th Place #102 Tempe, AZ 85281 (602) 967-9447	CTM-23891
L2	10 µH	CTM	CTM-23991

180 WATT APPLICATION CIRCUIT PARTS LIST (CONT.)

ITEM	DESCRIPTION	MANUFACTURER	PART NO.
T1	Current transformer	Beckman Industrial	HM31-20100
T2	Toroid Core	Beckman Industrial	HM00-91878
	Np=Ns=15 turns bifilar #28		
	Teflon Insulated Wire		
T3	Output Transformer	CTM	CTM-24091
R1	330 k, 1/8 W		
R2	470 k, 1/8 W		
R3	5.15 k, 1%, 1/8 W		
R4, R49	12 k, 1/8 W		
R5, R7	357 k, 1%, 1/4 W		
R6	4.75 k, 1%, 1/4 W		
R8	4.53 k, 1%, 1/4 W		
R9	27 k, 1/8 W		
R10, R18	33 k, 1/8 W		
R11	91 Ω, 1/8 W		
R12, R22	10 , 1/4 W		
R13, R14	4.7 k, 1/8 W		
R15	1 k, 1/8 W		
R16	15 k, 1/8 W		
R17	3 Ω, 1/8 W		
R19, R21	3k, 1/4 W		
R20	7.5 Ω, 1/4 W		
R23	100 Ω, 1/8 W		
R24, R25	1 Ω, 1/4 W		
R26	2 k, 1/8 W		
R27	6.2 k, 1/8 W		
R28	8.66 k, 1%, 1/4 W		
R29	2.26 k, 1%, 1/4 W		
R30	2.2 k, 1 W		
R31	330 k, 1/8 W		
R32, R33	2 k, 1/8 W		
R34	560 Ω, 1/8 W		
R35	2 k, 1 W		
R36	47 k, 1/8 W		
R37	47 k, 1/8 W		
R38, R48	100 k, 1/8 W		
R39	22 k, 1/8 W		
R40, R41	10 k, 1/8 W		
R42	12 Ω, 2 W		
R43	25 k, 1/8 W		
R44	330, 1/8 W		
R45	0.5 Ω, 2 W		
R46, R47	3.3 k, 1/8 W		



APPLICATION CIRCUIT FOR 350 WATT SUPPLY

350 WATT APPLICATION CIRCUIT PARTS LIST

ITEM	DESCRIPTION	MANUFACTURER	PART NO.
R1	10/5 W	Yageo	10W-5
R2	9 k / 3 W	Panasonic	P39KW-3
R3	43		
R4	15		
R5	10/ 2 W	Panasonic	P10W-2
R6	31 k		
R7	178 k, 1%		
R8	178 k, 1%		
R9	178 k, 1%		
R10	178 k, 1%		
R11	4.75 k, 1%		
R12	4.53 k, 1%		
R13	27 k		
R14	22 k		
R15	6.8 k		
R16	47 k		
R17	180 k		
R18	240 k		
R19	15 k		
R20	ADJ (22 k)		
R21	4.7 k		
R22	4.7 k		
R23	47 k		
R24	4.7 k		
R25	47 k		
R26	2.7 k		
R27	47 k		
R28	47 k		
R29	15 k, 1 %		
R30	33 k		
R31	27/ 5 W	Yageo	27 W-5
R32	15		
R33	4.7		
R34	10/ 2 W	Panasonic	P10W-2
R35	0.47, 1 W	Panasonic	P0.47W-1
R36	0.47, 1 W	Panasonic	P0.47W-1
R37	2 k ,/5 W	Yageo	2.0KW-5
R38	10/ 2 W	Panasonic	P10W-2
R39	5 m/ 3% 3 W	RCL	
R40	5 m, 3% 3 W	RCL	
R41	5 m/ 3% 3 W	RCL	
R42	47		
R43	8.2 k		
R44	4.7 k		
R45	4.7 k		
R46	4.7 k		
R47	4.7 K		

350 WATT APPLICATION CIRCUIT PARTS LIST (CONT.)

ITEM	DESCRIPTION	MANUFACTURER	PART NO.
R48	160		
R49	22 k		
R50	2.26 k/ 1%		
R51	2.26 k / 1%		
R52	ADJ		
R53	30.9 k / 1%		
R54	4.7 k		
R55	1 k		
R56	100		
R57	2.7 k		
R58	2.7 k		
R59	15		
R60	25 k		
C1	1 μ, 250 Vac, X	Panasonic	ECQ-U2A105MV
C2	1 μ, 250 Vac, X	Panasonic	ECQ-U2A105MV
C3	47 n, 100 V	Panasonic	ECQ-V1473JZ
C4	1 μ, 250 Vac, X	Panasonic	ECQ-U2A105MV
C5	47 n, 250 Vac, X	Panasonic	ECQ-U2A473MN
C6	1 n, 100 V	Panasonic	ECK-F2A102KBE
C7	10 n, 500 V	Panasonic	ECK-D2H103KBE
C8	1 μ, 400 V	Panasonic	ECQ-E4105KF
C9	330 μ, 450 V	Panasonic	ECQ-S2WU331Z
C10	330 μ, 450 V	Panasonic	ECQ-S2WU331Z
C11	1.5 n, 500 V	Panasonic	ECK-D2H152KBE
C12	3300 μ, 35 V	Panasonic	ECA-1VFQ332
C13	680 μ, 35 V	Panasonic	ECA-1VFQ681
C14	100 n, 50 V	Panasonic	ECF-F1H104ZF5
C15	4.7 n, 250 Vac, Y	Panasonic	ECQ-U2A472MF
C16	1.5 n, 500 V	Panasonic	ECK-D2H152KBE
C17	22 μ, 35 V	Panasonic	ECE-A1HGE220
C18	200 μ, 25 V	Panasonic	ECA-1EFQ221
C19	1 n, 100 V	Panasonic	ECC-F2A102JE
C20	100 n, 50 V	Panasonic	ECF-F1H104ZF5
C21	1 μ, 50 V	Panasonic	ECQ-V1H105JZ
C22	220 n, 50 V	Panasonic	ECQ-V1H224JZ
C23	100 p, 100 V	Panasonic	ECK-F2A101KBE
C24	1 μ, 50 V	Panasonic	ECQ-V1H105JZ
C25	33 n, 25 V	Panasonic	
C26	1 μ, 50 V	Panasonic	ECQ-V1H105JZ
C27	10 n, 500 V	Panasonic	ECK-D2H103KBE
C28	100 n, 100 V	Panasonic	ECQ-V1104JZ
C29	100 p, 1000V	Panasonic	ECK-D3A101KBN
C30	22 μ, 35 V	Panasonic	ECE-A1HGE220
C31	4.7 n, 500 V	Panasonic	ECK-D2H472KBE
C32	10,000 μ, 10 V	Panasonic	ECA-1AFQ103
C33	3,900 μ, 10 V	Panasonic	ECA-1AFQ392L

350 WATT APPLICATION CIRCUIT PARTS LIST (CONT.)

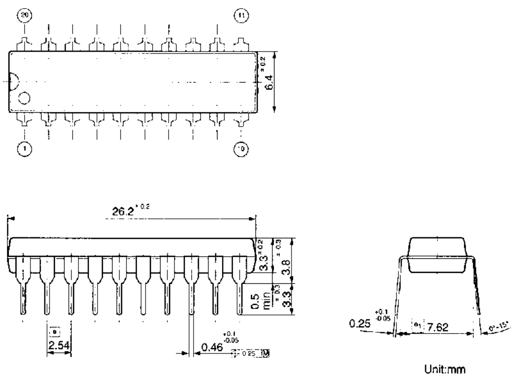
ITEM	DESCRIPTION	MANUFACTURER	PART NO.
C34	100 n, 50 V	Panasonic	ECF-F1H104ZF5
C35	100 n, 50 V	Panasonic	ECF-F1H104ZF5
C36	33 n, 25 V	Panasonic	ECF-F1E333MR
C37	33 n, 25 V	Panasonic	ECF-F1E333MR
C38	33 n, 25 V	Panasonic	ECF-F1E333MR
C39	33 n, 25 V	Panasonic	ECF-F1E333MR
C40	47 n, 250 Vac, X	Panasonic	ECQ-U2A473MN
C41	4.7 n, 250 Vac, Y	Panasonic	ECQ-U2A472MF
C42	4.7 n, 250 Vac, Y	Panasonic	ECQ-U2A472MF
C43	Ceramic Disc .01 µF, 1 kV		
U1	TK84819	TOKO	
U2	LM358N		
U3	TL431CLP	Motorola, TI	
OC1	CNY17-2ZGI	Quality Tech.	
Q1	MTG9N50E	Motorola	
Q2	2SC4237	Shindengen	
Q3	MTP3055E	Motorola	
Q4	2N4403		
Q5	2N4401		
Q6	2N4401		
D1	1N5245B	Motorola	
D2	1N4818		
D3	MURH850Ct	Motorola	
D4	HER102	Diodes, Inc.	
D5	HER102	Diodes, Inc.	
D6	HER102	Diodes, Inc.	
D7	BYV26C	Philips	
D8	BYV26C	Philips	
D9	HER102	Diodes, Inc.	
D10	HER102	Diodes, Inc.	
D11	HER102	Diodes, Inc.	
D12	1N5818		
D13	1N5818	Diodes, Inc.	
D14	BYV26E	Philips	
D15	HER102	Diodes, Inc.	
D16	S60SC4M	Shindengen	
D17	MUR3015PT	Motorola	
D18	BYV26E	Philips	
D19	IN4148		
D20	IN4148		
D21	IN4148		
D22	IN5248B	Motorola	
B1	MB106-ND	Diodes, Inc.	

350 WATT APPLICATION CIRCUIT PARTS LIST (CONT.)

ITEM	DESCRIPTION	MANUFACTURER	PART NO.
K1	G5LE-114P-PS	OMRON	
L1	CTM 27591	CTM Magnetics	
L2	CTM 27591	1419 W. 12th Place	
L3	CTM 27291	Tempe, AZ 85281	
L4	CTM 27391	(602) 967-9447	
L5	*optional	2T AWG 18 Micrometals T51-52C Powered Iron Core	
L6	*optional	2T AWG 18 Micrometals T51-52C Powered Iron Core	
T1	HM31-2100	Beckman Industrial	
T2	CTM 27491	CTM Magnetics	
HS1	HS104-2	AAVID	
HS2	#11269	Thermalloy Extrusion 10.25"	
F1	6.3A SLO-BLO	5X20 MM	
FUSE CLIP	FO58-ND	Digi-Key (2 EA)	
E1	FN405-6/02	Schaffner EMI Filter	
V1	ERZ-C100K431U	Panasonic ZNR	
J2-J5	ED1601	Onshore Tech	

PACKAGE OUTLINES

DIP20



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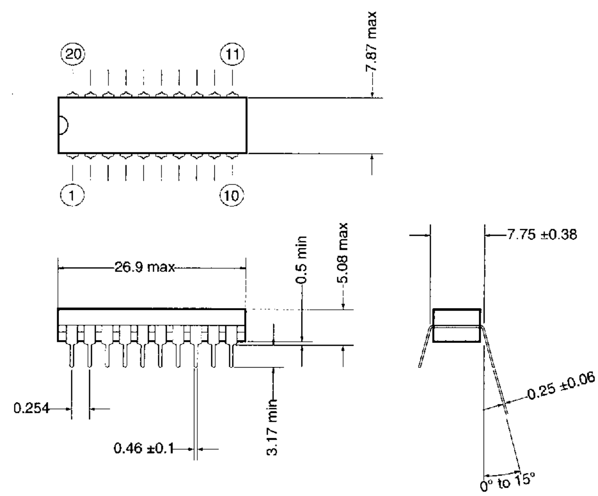

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