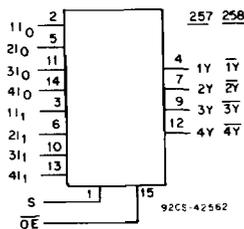


CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

Quad 2-Input Multiplexer with 3-State Outputs

CD54/74AC/ACT257 - Non-Inverting Outputs

CD54/74AC/ACT258 - Inverting Outputs



FUNCTIONAL DIAGRAM

Type Features:

- Buffered inputs
- Typical propagation delay:
4.4 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$, $C_L = 50\text{ pF}$

The RCA-CD54/74AC257 and CD54/74AC258 and the CD54/74ACT257 and CD54/74ACT258 are quad 2-input multiplexers with 3-state outputs. These devices use the RCA ADVANCED CMOS technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable ($\overline{\text{OE}}$) is active LOW. When $\overline{\text{OE}}$ is HIGH, all of the outputs (Y or $\overline{\text{Y}}$) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the CD54/74AC/ACT257 and CD54/74AC/ACT258. The state of the Select input determines the particular register from which the data comes. The CD54/74AC/ACT257 and CD54/74AC/ACT258 can also be used as function generators.

The CD74AC/ACT257 and CD74AC/ACT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70° C); Industrial (-40 to $+85^\circ\text{ C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{ C}$).

The CD54AC/ACT257 and CD54AC/ACT258, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{ C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST[®]/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST[®] ICs
 - Drives 50-ohm transmission lines

[®]FAST is a Registered Trademark of Fairchild Semiconductor Corp.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		257 Outputs	258 Outputs
		I ₀	I ₁	Y	$\overline{\text{Y}}$
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level voltage
 L = Low level voltage
 Z = High impedance (off) state.
 X = Don't care

CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_o (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

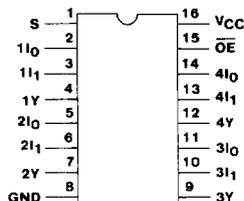
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_i, V_o	0	V_{CC}	V
Operating Temperature, T_A	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dV/dt at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.

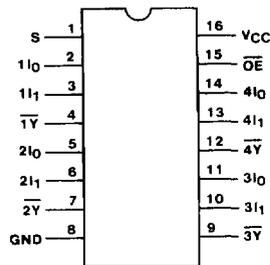
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TERMINAL ASSIGNMENT DIAGRAMS



92CS-38420R1

CD54/74AC/ACT257



92CS-39815

CD54/74AC/ACT258

CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V _{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V _{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
	#, * {	-4	3	2.58	—	2.48	—	2.4	—	
	-24	4.5	3.94	—	3.8	—	3.7	—		
	-75	5.5	—	—	3.85	—	—	—		
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
	#, * {	12	3	—	0.36	—	0.44	—	0.5	
	24	4.5	—	0.36	—	0.44	—	0.5		
	75	5.5	—	—	—	1.65	—	—		
Input Leakage Current I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
	V _I (V)	I _O (mA)		+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I _{oz}	V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Data	0.83
S	1.27
\overline{OE}	1.27

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: I_n to Y	257	t_{PLH} t_{PHL}	1.5	—	106	—	117	ns
			3.3*	3.3	11.8	3.3	13	
S to Y	257	t_{PLH} t_{PHL}	5†	2.4	8.5	2.3	9.3	ns
			1.5	—	153	—	168	
\overline{OE} to Y	257	t_{PLH} t_{PHL}	3.3	4.8	17.1	4.7	18.8	ns
			5	3.5	12.2	3.4	13.4	
\overline{OE} to Y	257	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	1.5	—	167	—	184	ns
			3.3	5.3	18.7	5.2	20.6	
I_n to \overline{Y}	258	t_{PLH} t_{PHL}	5	3.8	13.4	3.7	14.7	ns
			1.5	—	91	—	100	
S to \overline{Y}	258	t_{PLH} t_{PHL}	3.3	2.9	10.2	2.8	11.2	ns
			5	2.1	7.3	2	8	
\overline{OE} to \overline{Y}	258	t_{PLH} t_{PHL}	1.5	—	153	—	168	ns
			3.3	4.8	17.1	4.7	18.8	
\overline{OE} to \overline{Y}	258	t_{PLH} t_{PHL}	5	3.5	12.2	3.4	13.4	ns
			1.5	—	167	—	184	
\overline{OE} to \overline{Y}	258	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	3.3	5.3	18.7	5.2	20.6	ns
			5	3.8	13.4	3.7	14.7	
Power Dissipation Capacitance	$C_{PD}\S$	—	130 Typ.		130 Typ.		pF	
Input Capacitance	C_i	—	—	10	—	10	pF	
3-State Output Capacitance	C_o	—	—	15	—	15	pF	

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
			-40 to +85		-55 to +125			
			MIN.	MAX.	MIN.	MAX.		
Propagation Delays: I_n to Y	257	t_{PLH} t_{PHL}	5†	2.8	9.7	2.7	10.7	ns
			1.5	—	153	—	168	
S to Y	257	t_{PLH} t_{PHL}	5	4	14	3.9	15.4	ns
			1.5	—	153	—	168	
\overline{OE} to Y	257	t_{PLH} t_{PHL}	3.3	4.8	17.1	4.7	18.8	ns
			5	3.5	12.2	3.4	13.4	
\overline{OE} to Y	257	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	1.5	—	167	—	184	ns
			3.3	5.3	18.7	5.2	20.6	
I_n to \overline{Y}	258	t_{PLH} t_{PHL}	5	3.8	13.4	3.7	14.7	ns
			1.5	—	91	—	100	
S to \overline{Y}	258	t_{PLH} t_{PHL}	3.3	2.9	10.2	2.8	11.2	ns
			5	2.1	7.3	2	8	
\overline{OE} to \overline{Y}	258	t_{PLH} t_{PHL}	1.5	—	153	—	168	ns
			3.3	4.8	17.1	4.7	18.8	
\overline{OE} to \overline{Y}	258	t_{PLH} t_{PHL}	5	3.5	12.2	3.4	13.4	ns
			1.5	—	167	—	184	
\overline{OE} to \overline{Y}	258	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	3.3	5.3	18.7	5.2	20.6	ns
			5	3.8	13.4	3.7	14.7	
Power Dissipation Capacitance	$C_{PD}\S$	—	130 Typ.		130 Typ.		pF	
Input Capacitance	C_i	—	—	10	—	10	pF	
3-State Output Capacitance	C_o	—	—	15	—	15	pF	

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

$\S C_{PD}$ is used to determine the dynamic power consumption per multiplexer.

For AC Series: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$

For ACT Series: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$

where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

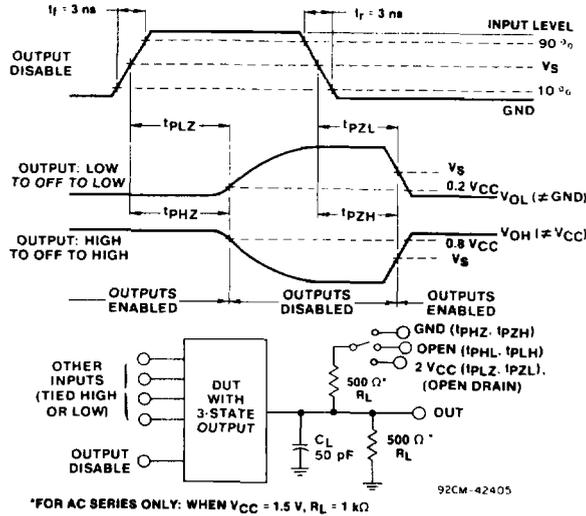


Fig. 1 - Three-state propagation delay waveforms and test circuit.

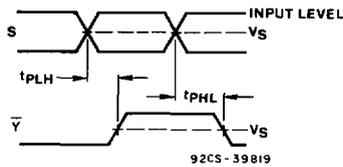


Fig. 2 - Select to output propagation delays (AC:ACT258).

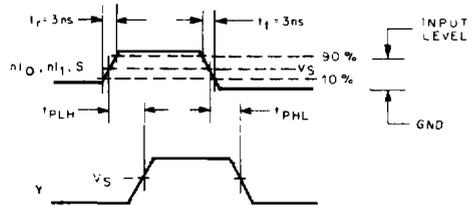


Fig. 3 - Inputs or select to output propagation delays (AC:ACT257).

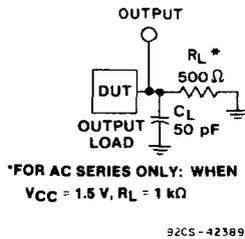


Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$