

# OC-35 Series

3.2X5X1.2mm / 3.3V / SMD / HCMOS/TTL Oscillator

Lead-Free  
RoHS Compliant

**CALIBER**  
Electronics Inc.

## PART NUMBERING GUIDE

Environmental/Mechanical Specifications on page F5

<b>OC-35A- 100 48 A T - 30.000MHz</b>	
<b>Package</b> OC-35 = 3.3Vdc OC-35A = 1.8Vdc OC-35B = 2.5Vdc	<b>Pin One Connection</b> T = Tri State Enable High
<b>Inclusive Stability</b> 100= +/-100ppm, 50= +/-50ppm, 30= +/-30ppm, 25= +/-25ppm, 20= +/-20ppm (25,20 = 0°C-70°C Only)	<b>Output Symmetry</b> Blank = 40/60%, A = 45/55%
	<b>Operating Temperature Range</b> Blank = -10°C to 70°C, 27 = -20°C to 70°C, 48 = -40°C to 85°C

## ELECTRICAL SPECIFICATIONS

Revision: 2003-B

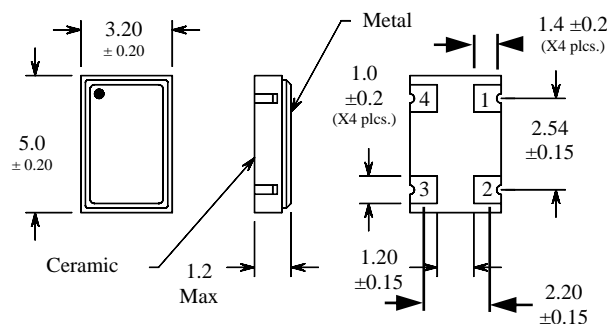
<b>Frequency Range</b>	1.544MHz to 156.250MHz / <b>32.768kHz @ 3.3V</b>	
<b>Operating Temperature Range</b>	-10°C to 70°C / -20°C to 70°C / -40°C to 85°C	
<b>Storage Temperature Range</b>	-55°C to 125°C	
<b>Supply Voltage</b>	A=1.8Vdc / B=2.5Vdc / BLANK=3.3Vdc ±10%	
<b>Input Current</b>	1.544MHz to 36.000MHz and <b>32.768kHz</b> 36.001MHz to 70.000MHz 70.001MHz to 125.000MHz	2mA Maximum 5mA Maximum 7mA Maximum
<b>Frequency Tolerance / Stability</b>	Inclusive of Operating Temperature Range, Supply Voltage and Load	±100ppm, ±50ppm, ±30ppm, ±25ppm, ±20ppm (±50ppm for <b>32.768kHz</b> only)
<b>Output Voltage Logic High (Voh)</b>	w/HCMOS or TTL Load	90% of Vdd Min. / Ioh=-8mA
<b>Output Voltage Logic Low (Vol)</b>	w/HCMOS or TTL Load	10% of Vdd Max. / Iol=8mA
<b>Rise / Fall Time</b>	10% to 90% of Waveform w/HCMOS Load; 0.4Vdc to 2.4V w/TTL Load / 6nSec Max.	
<b>Duty Cycle</b>	@1.4Vdc w/TTL Load; @50% w/HCMOS Load @1.4Vdc w/TTL Load or w/HCMOS Load	50 ±10% (Standard) 50±5% (Optional)
<b>Load Drive Capability</b>	<= 70.000MHz >70.000MHz <=70.000MHz (Optional)	10LSTTL Load or 15pF HCMOS Load 15pF HCMOS Load 10TTL Load or 50pF HCMOS Load
<b>Pin 1 Tristate Input Voltage</b>	No Connection VIH VIL	Enables Output 2.2Vdc Minimum to Enable Output +0.8Vdc Maximum to Disable Output
<b>Aging (@ 25°C)</b>	±5ppm / year Maximum	
<b>Start Up Time</b>	10mSeconds Maximum	
<b>Absolute Clock Jitter</b>	±250pSeconds Maximum	
<b>One Sigma Clock Jitter</b>	±50pSeconds Maximum	

## MECHANICAL DIMENSIONS

## Marking Guide

All Dimensions in mm.

**Application Note:**  
A 0.01uF bypass capacitor should be placed between Vdd (pin 4) and GND (pin 2) to minimize power supply line noise.



Line 1: A, B or Blank - Frequency  
Line 2: CEI YM

A = Voltage designator  
CEI = Caliber Electronics Inc.  
YM = Date Code (Year / Month)

Pin 1: Tri-State  
Pin 2: Case Ground

Pin 3: Output  
Pin 4: Supply Voltage

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