

## DIFFERENTIAL OUTPUT SILICON OSCILLATOR

### Features

- Quartz-free, MEMS-free, and PLL-free all-silicon oscillator
- Any-rate output frequencies from 0.9 to 200 MHz
- Short lead times
- Excellent temperature stability ( $\pm 20$  ppm)
- Highly reliable startup and operation
- High immunity to shock and vibration
- Low jitter:  $< 1.5$  ps
- 0 to 85 °C operation includes 10-year aging in hot environments
- Footprint compatible with industry-standard 3.2 x 5.0 mm XO's
- CMOS and SSTL versions available
- Driver stopped, tri-state, or powerdown operation
- RoHS compliant
- 1.8, 2.5, or 3.3 V options
- Low power
- More than 10x better fit rate than competing crystal solutions



### Specifications

Parameters	Condition	Min	Typ	Max	Units
Frequency Range		0.9	—	200	MHz
Frequency Stability	Temperature stability, 0 to +70 °C	—	$\pm 10$	—	ppm
	Temperature stability, 0 to +85 °C	—	$\pm 20$	—	ppm
	Total stability, 0 to +70 °C operation <sup>1</sup>	—	—	$\pm 150$	ppm
	Total stability, 0 to +85 °C operation <sup>2</sup>	—	—	$\pm 250$	ppm
Operating Temperature		0	—	+85	°C
Storage Temperature		-55	—	+125	°C
Supply Voltage	1.8 V option	1.71	—	1.98	V
	2.5 V option	2.25	—	2.75	V
	3.3 V option	2.97	—	3.63	V
Supply Current	LVPECL	—	34.0	36.0	mA
	Low Power LVPECL	—	19.3	22.2	mA
	LVDS	—	14.9	16.5	mA
	HCSL	—	25.3	29.3	mA
	Differential CMOS(3.3 V option, 10 pF, 200 MHz)	—	29.0	31.8	mA
	Differential SSTL-3	—	24.5	27.7	mA
	Differential SSTL-2	—	24.3	26.7	mA
	Differential SSTL-18	—	22.2	25	mA
	Tri-State	—	9.7	10.7	mA
Powerdown	—	1.0	1.9	mA	
Output Symmetry	$V_{DIFF} = 0$	46 – 13 ns/ $T_{CLK}$	—	54 + 13 ns/ $T_{CLK}$	%

#### Notes:

1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.
2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See “AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators” for further details regarding output clock termination recommendations.
4. Min column entries are minima of VOH. Max column entries are maxima of VOL.

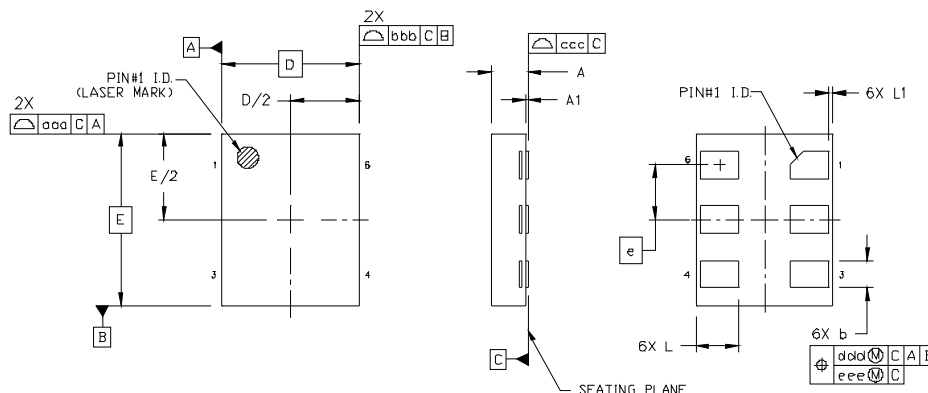
# Si500D

Parameters	Condition	Min	Typ	Max	Units
Rise and Fall Times (20/80%) <sup>3</sup>	LVPECL/LVDS	—	—	460	ps
	HCSL/Differential SSTL	—	—	800	ps
	Differential CMOS, 15 pF, ≥80 MHz	—	1.1	1.6	ns
LVPECL Output Option (DC coupling, 50 Ω to V <sub>DD</sub> – 2.0 V) <sup>3</sup>	Mid-level	V <sub>DD</sub> – 1.5	—	V <sub>DD</sub> – 1.34	V
	Diff swing	.720	—	.880	V <sub>PK</sub>
Low Power LVPECL Output Option (AC coupling, 100 Ω Differential Load) <sup>3</sup>	Mid-level	—	N/A	—	V
	Diff swing	.68	—	.95	V <sub>PK</sub>
LVDS Output Option (2.5/3.3 V) (R <sub>TERM</sub> = 100 Ω diff) <sup>3</sup>	Mid-level	1.15	—	1.26	V
	Diff swing	0.25	—	0.45	V <sub>PK</sub>
LVDS Output Option (1.8 V) (R <sub>TERM</sub> = 100 Ω diff) <sup>3</sup>	Mid-level	0.85	—	0.96	V
	Diff swing	0.25	—	0.45	V <sub>PK</sub>
HCSL Output Option <sup>3</sup>	Mid-level	0.35	—	0.425	V
	Diff swing	0.65	—	0.82	V <sub>PK</sub>
	DC termination per pad	45	—	55	Ω
CMOS Output Voltage <sup>3</sup>	V <sub>OH</sub> , sourcing 9 mA	V <sub>DD</sub> – 0.6	—	—	V
	V <sub>OL</sub> , sinking 9 mA	—	—	0.6	V
SSTL Output Voltage <sup>4</sup>	SSTL-18	.5 x V <sub>DD</sub> + 0.375	—	.5 x V <sub>DD</sub> – 0.375	V
	SSTL-2	.5 x V <sub>DD</sub> + 0.48	—	.5 x V <sub>DD</sub> – 0.48	V
	SSTL-3	.45 x V <sub>DD</sub> + 0.48	—	.45 V <sub>DD</sub> – 0.48	V
Powerup Time	From time V <sub>DD</sub> crosses min spec supply	—	—	2	ms
OE Deassertion to Clk Stop		—	—	250 + 3 x T <sub>CLK</sub>	ns
Return from Output Driver Stopped Mode		—	—	250 + 3 x T <sub>CLK</sub>	ns
Return From Tri-State Time		—	—	12 + 3 x T <sub>CLK</sub>	μs
Return From Powerdown Time		—	—	2	ms
Period Jitter (1-sigma)	Non-CMOS	—	1	2	ps RMS
	CMOS, C <sub>L</sub> = 7 pF	—	1	3	ps RMS
Integrated Phase Jitter	1.0 MHz – min(20 MHz, 0.4 x F <sub>OUT</sub> ), non-CMOS	—	0.6	1	ps RMS
	1.0 MHz – min(20 MHz, 0.4 x F <sub>OUT</sub> ), CMOS format	—	0.7	1.5	ps RMS

**Notes:**

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2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.
3. See “AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators” for further details regarding output clock termination recommendations.
4. Min column entries are minima of V<sub>OH</sub>. Max column entries are maxima of V<sub>OL</sub>.

## Package Specifications



**Table 1. Package Diagram Dimensions (mm)**

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.03	0.05
b	0.59	0.64	0.69
D	3.20 BSC.		
e	1.27 BSC.		
E	4.00 BSC.		
L	0.95	1.00	1.05

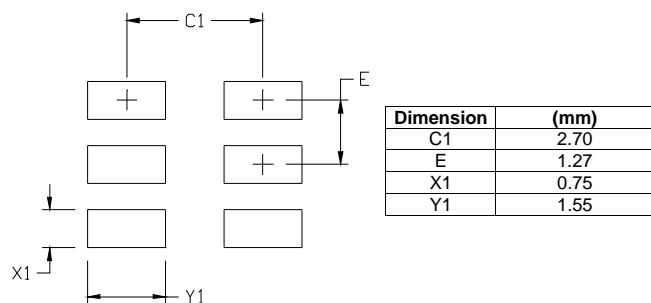
Dimension	Min	Nom	Max
L1	0.00	0.05	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

**Table 2. Pad Connections**

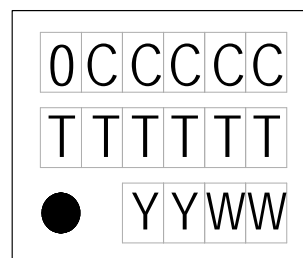
1	OE
2	NC—Make no external connection to this pin
3	GND
4	Output
5	Complementary Output
6	VDD

**Table 3. Tri-State/Powerdown/Driver Stopped Function on OE (3rd Option Code)**

	A	B	C	D	E	F
<b>Open</b>	Active	Active	Active	Active	Active	Active
<b>1 Level</b>	Active	Tri-State	Active	Power-down	Active	Driver Stopped
<b>0 Level</b>	Tri-State	Active	Power-down	Active	Driver Stopped	Active



**Figure 1. Recommended Land Pattern**



0 = Si500  
 CCCCC = mark code  
 TTTTTT = assembly manufacturing code  
 YY = year  
 WW = work week

**Figure 2. Top Mark**

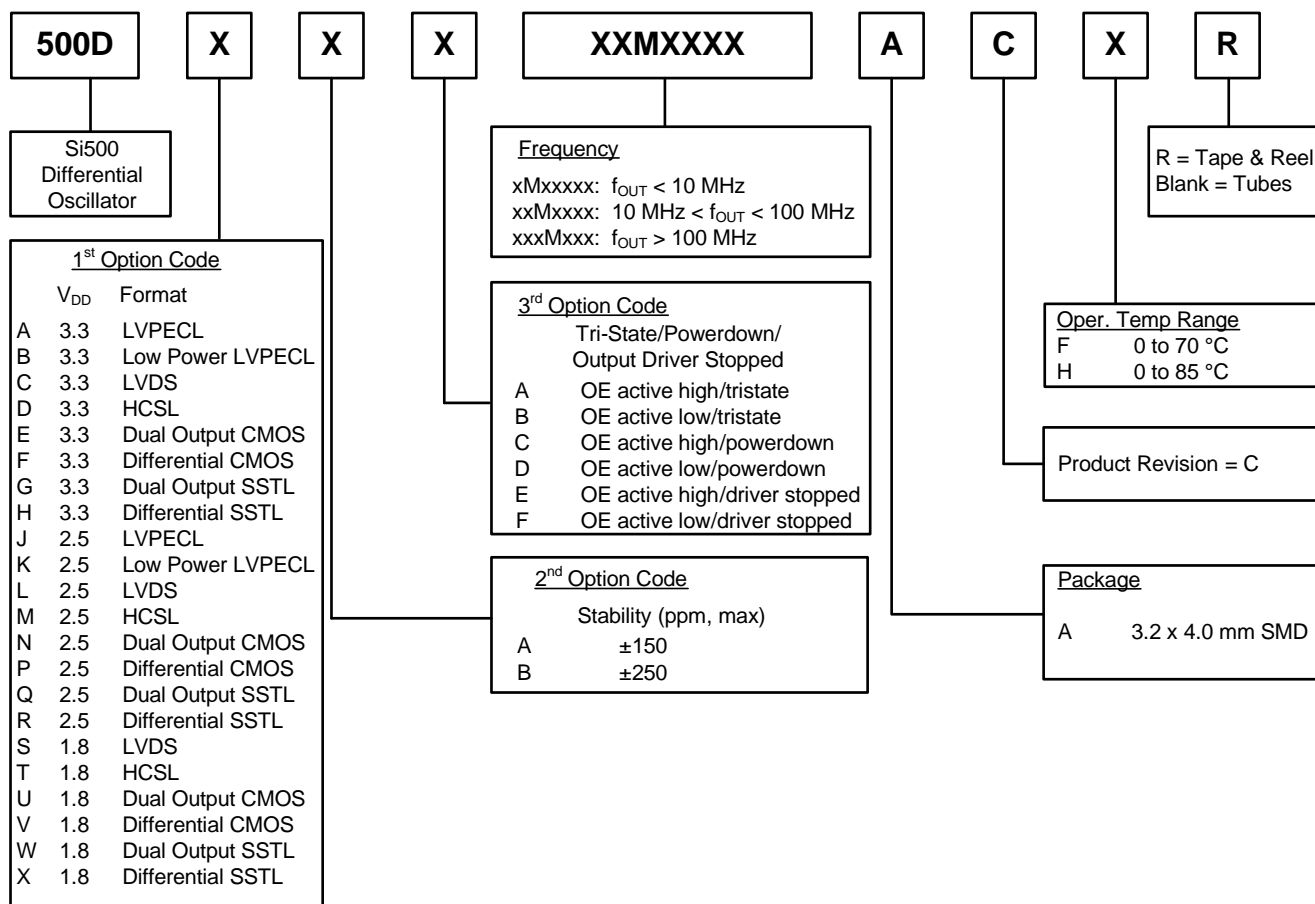
# Si500D

## Environmental Compliance

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002.4
Mechanical Vibration	MIL-STD-883, Method 2007.3 A
Resistance to Soldering Heat	MIL-STD-202, 260 C° for 8 seconds
Solderability	MIL-STD-883, Method 2003.8
Damp Heat	IEC 68-2-3
Moisture Sensitivity Level	J-STD-020, MSL 3

## Ordering Information

The Si500D supports a variety of options including frequency, output format, supply voltage, and tri-state/powerdown. Specific device configurations are programmed into the Si500D at time of shipment. Configurations are specified using the figure below. Silicon Labs provides a web-based part number utility that can be used to simplify part number configuration. Refer to [www.silabs.com/SiliconXOPartnumber](http://www.silabs.com/SiliconXOPartnumber) to access this tool. The Si500D XO series is supplied in a ROHS-compliant, Pb-free, 6-pad, 3.2 x 4.0 mm package. Tape and reel packaging is available as an ordering option.



## DOCUMENT CHANGE LIST

### Revision 0.2 to Revision 0.3

- Revision B to Revision C updated in Ordering Information
- 0 to 85 C° Operating Temperature Range option added

# Si500D

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## CONTACT INFORMATION

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