FAIRCHILD
A Schlumberger Company

F100136
4-Stage Counter/ Shift Register

F100K ECL Product

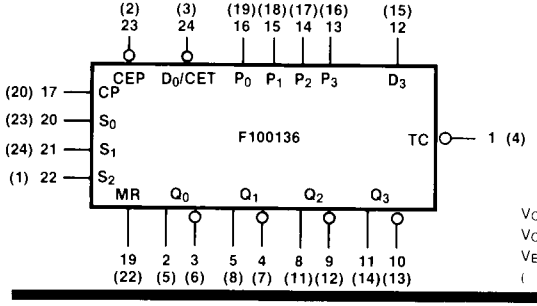
Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50K Ω pull-down resistors.

Pin Names

CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0-S_2	Select Inputs
MR	Master Reset Input
P_0-P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0-Q_3	Data Outputs
$\overline{Q_0}$-$\overline{Q_3}$	Complementary Data Outputs

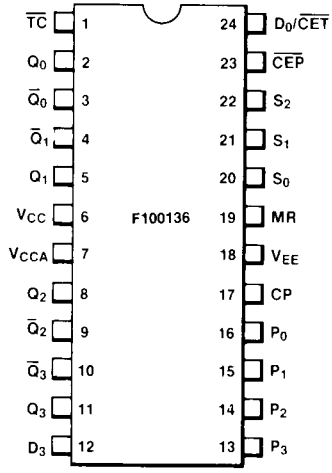
Logic Symbol



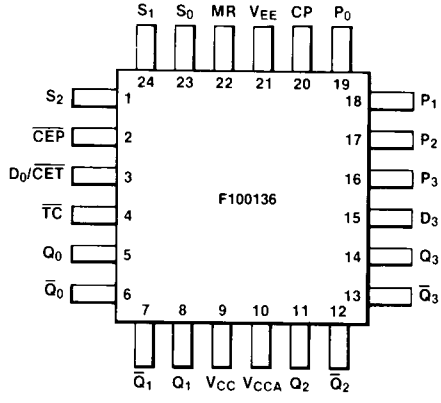
VCC = Pin 6 (9)
VCCA = Pin 7 (10)
VEE = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



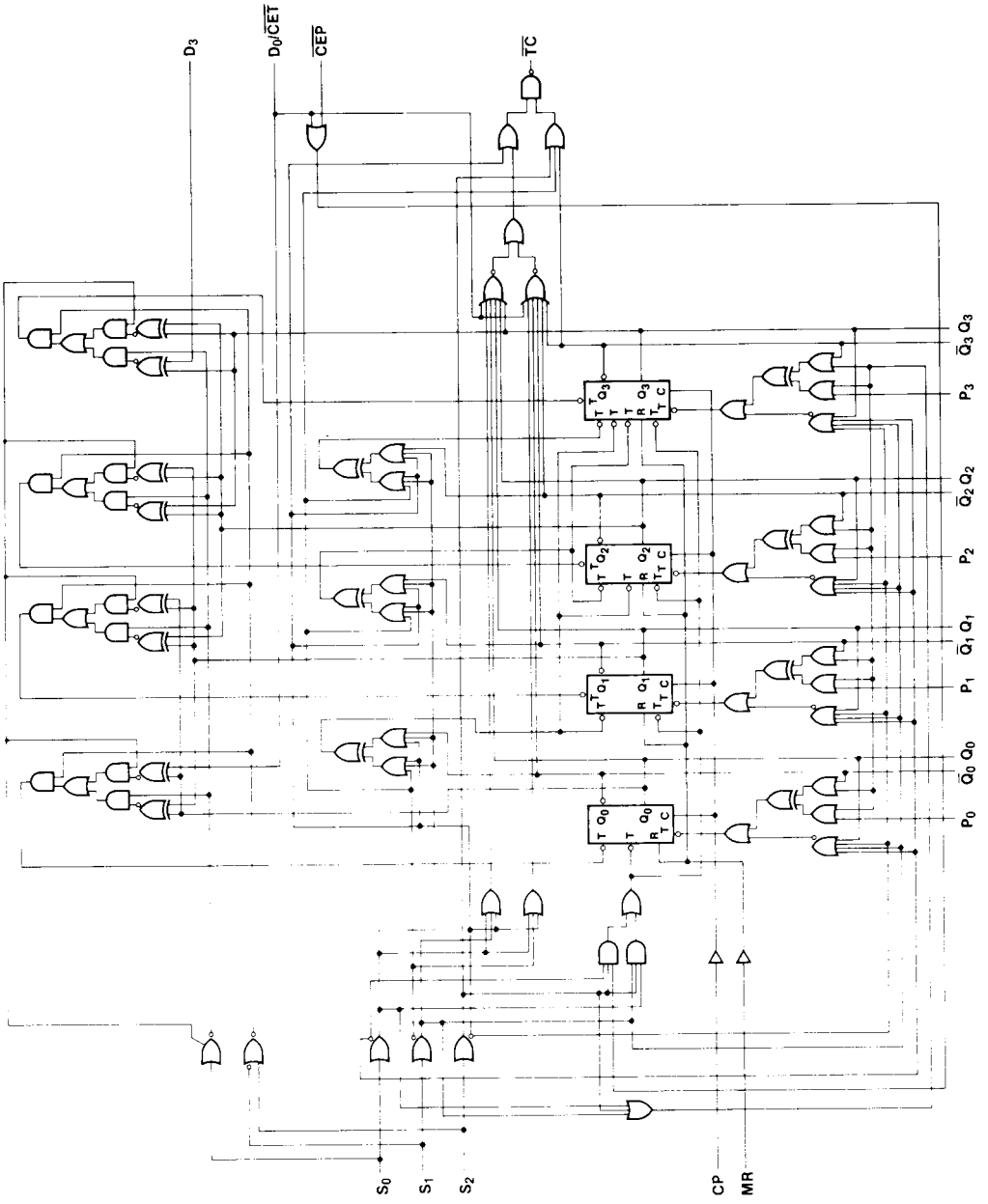
24-Pin Flatpak (Top View)



Ordering Information

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Diagram



Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Truth Table

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	⎍	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	X	X	X	⎍	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	L	H	L	X	X	X	⎍	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	X	X	X	⎍	D_0	Q_0	Q_1	Q_2	Q_3*	Shift Right
L	H	L	L	L	L	X	⎍	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	⎍	L	L	L	L	H	Clear
L	H	H	L	L	L	X	⎍	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0-Q_3 = LLLL
H if Q_0-$Q_3 \neq$ LLLL
② = L if Q_0-Q_3 = HHHH
H if Q_0-$Q_3 \neq$ HHHH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Transition

*Before the clock, $\overline{TC}$ is Q_3
After the clock, $\overline{TC}$ is Q_2

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current P_n, S_n $\overline{CEP}$ MR D_3 CP $D_0/\overline{CET}$			 180 200 240 280 390 530	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−283	−195	−136	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

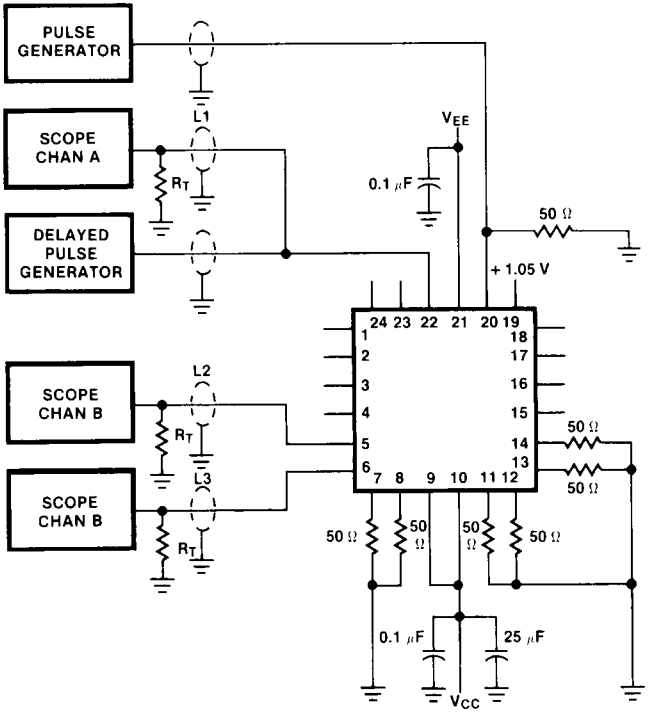
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	2.10	0.85	2.10	0.85	2.25	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.80	1.90	4.60	1.90	5.20	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.95	1.35	2.95	1.20	3.10	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.80	2.20	4.80	2.20	5.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.20	1.40	3.20	1.40	3.50	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.80	1.00	3.80	1.00	4.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	 1.20 1.70 1.45 3.30 2.60		 1.20 1.70 1.45 3.30 2.60		 1.20 1.70 1.45 3.30 2.60		ns	*Figure 6*
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	 0.20 0.10 0.20 −0.90		 0.20 0.10 0.20 −0.90		 0.20 0.10 0.20 −0.90		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

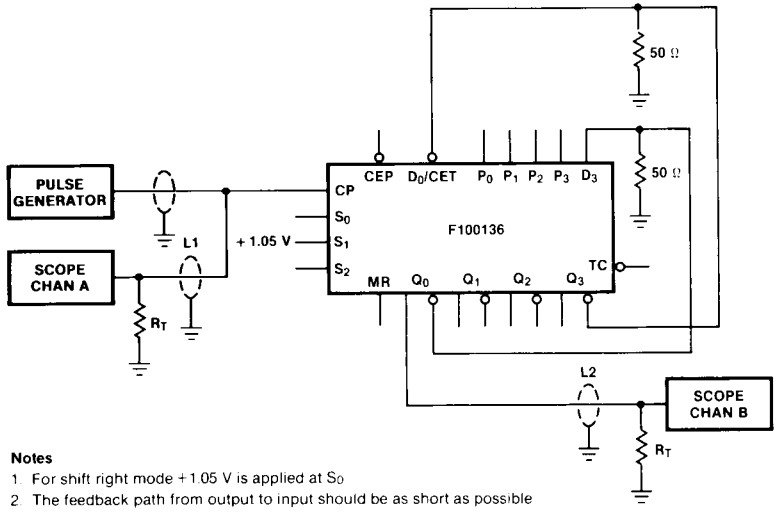
Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	1.90	0.85	1.90	0.85	2.05	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.60	1.90	4.40	1.90	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.75	1.35	2.75	1.20	2.90	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.60	2.20	4.60	2.20	5.10	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.00	1.40	3.00	1.40	3.30	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.60	1.00	3.60	1.00	4.10	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		ns	*Figure 6*
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Shift Frequency Test Circuit (Shift Left)



Notes
1. For shift right mode +1.05 V is applied at S_0
2. The feedback path from output to input should be as short as possible

Fig. 3 Propagation Delay (Clock) and Transition Times

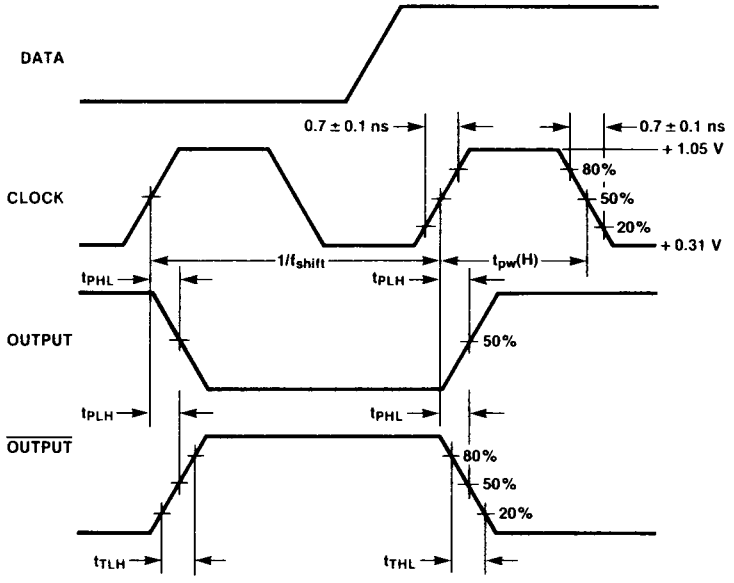


Fig. 4 Propagation Delay (Reset)

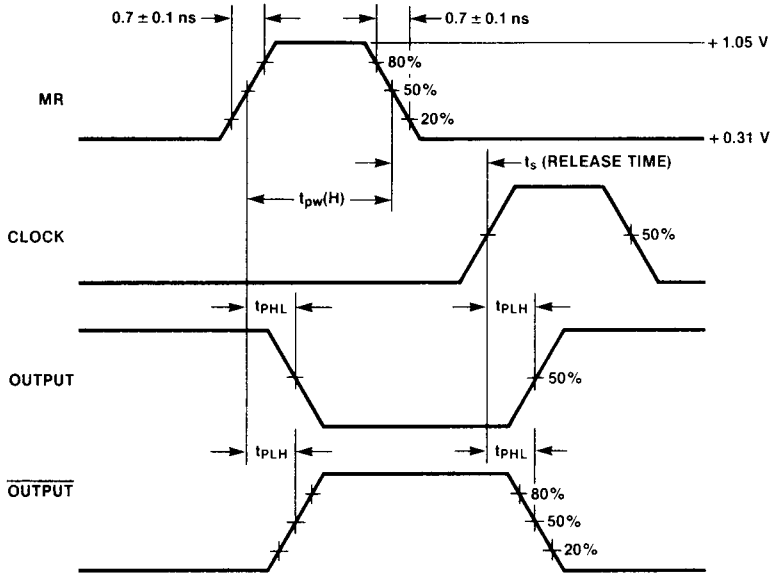


Fig. 5 Propagation Delay (Serial Data, Selects)

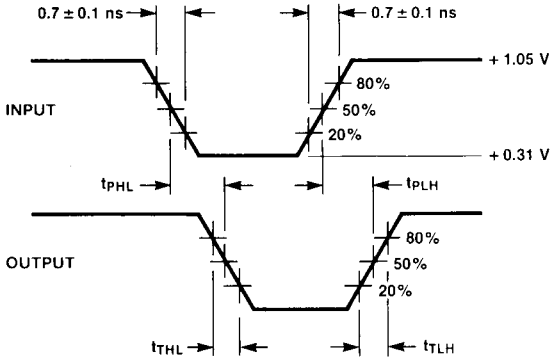
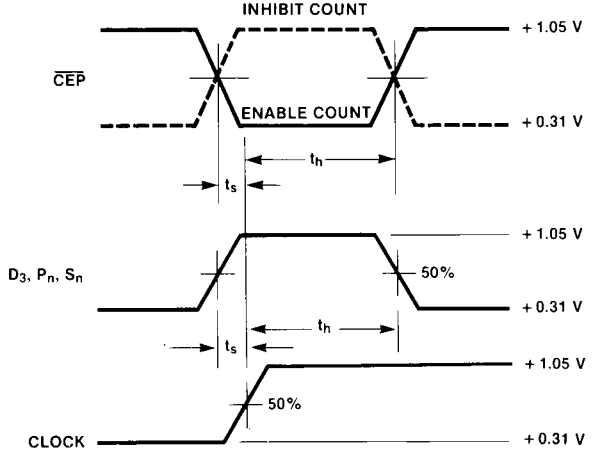


Fig. 6 Setup and Hold Time



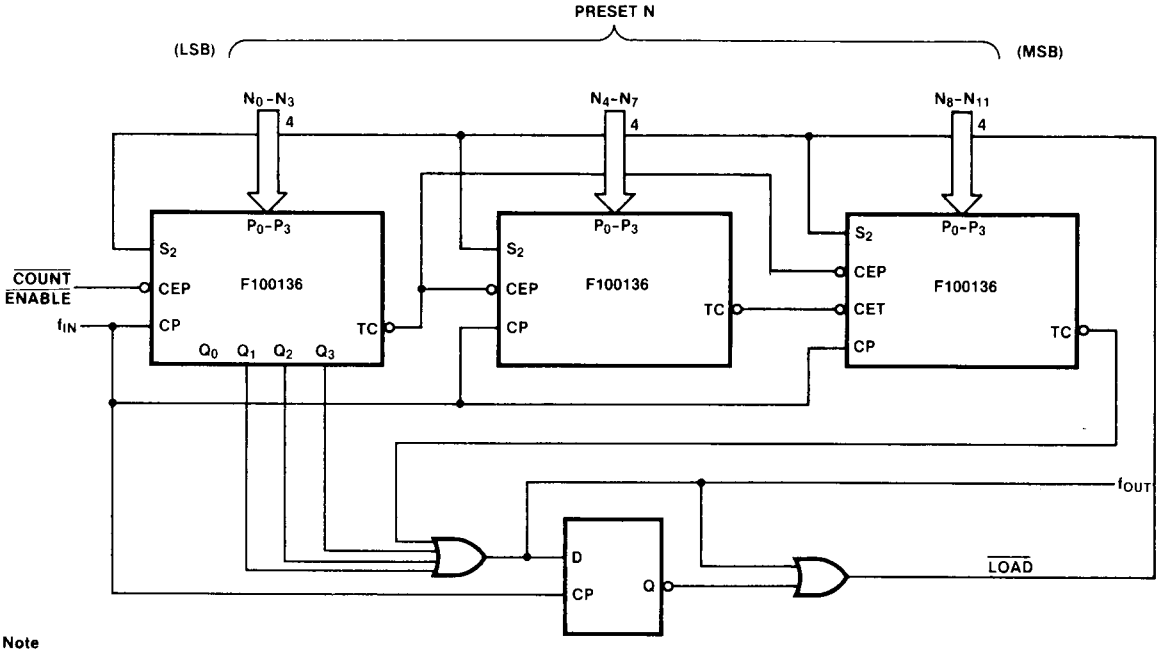
Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

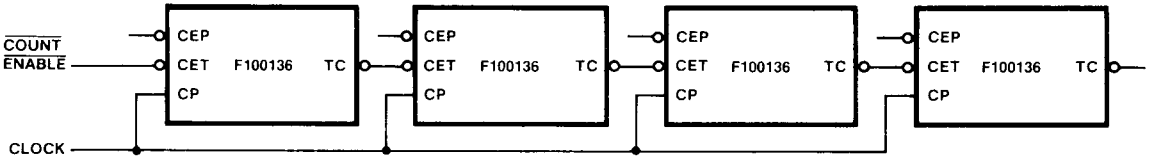
Application

3-Stage Divider, Preset Count Down Mode



Note
If $S_0 = S_1 = S_2 =$ LOW, then $T_C =$ LOW

Slow Expansion Scheme



Fast Expansion Scheme