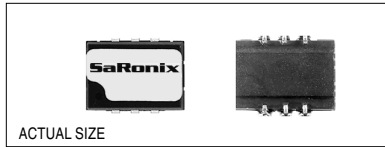


Technical Data

S1328 Series



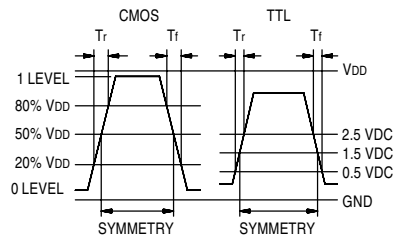
Description

A voltage controlled crystal oscillator, with output logic levels compatible with HCMOS and TTL logic families. The 6-pin, plastic molded SMD, J-lead package ("S" package) is ideal for today's automated assembly environments.

Applications

- For use with phase-locked loop (PLL) for clock and data recovery, frequency translation, or frequency synthesis applications in video, telephony, and data communication environments.
- Compact, plastic molded SMD package
- TTL and CMOS compatible
- Tri-state output

Output Waveform



Frequency Range:	1.5 MHz to 27 MHz
Frequency Stability:	±50 ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, with $V_C = 1.65V$
Aging:	±12ppm max in 10 Years @ +40°C
Temperature Range:	Operating: 0 to +70°C, -40 to +85°C Storage: -55 to +125°C
Supply Voltage:	Recommended Operating: 3.3V ±10%
Supply Current:	15mA max
Output:	Symmetry: 45/55% max @ 50% VDD Rise & Fall Times: 9ns max 20% to 80% VDD Logic 0: 10% VDD max Logic 1: 90% VDD min Load: 30pF Jitter: 20ps peak-to-peak max
Pull Characteristics:	Input Impedance: 50KΩ min Frequency Response (-3dB): 10kHz Pullability: ±25ppm, ±50ppm, ±75ppm APR* (See Part Numbering Guide) Control Voltage: 0.3 to 3V Transfer Function: Frequency increases when Control Voltage increases Linearity: 10% max Center Control Voltage: 1.65V
Mechanical:	Shock: MIL-STD-883, Method 2002, Condition B Solderability: MIL-STD-883, Method 2003 Terminal Strength: MIL-STD-883, Method 2004, Condition B2 Vibration: MIL-STD-883, Method 2007, Condition A Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J
Environmental:	Thermal Shock: MIL-STD-883, Method 1011, Condition A Moisture Resistance: MIL-STD-883, Method 1004

* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability) – (Aging)

Technical Data

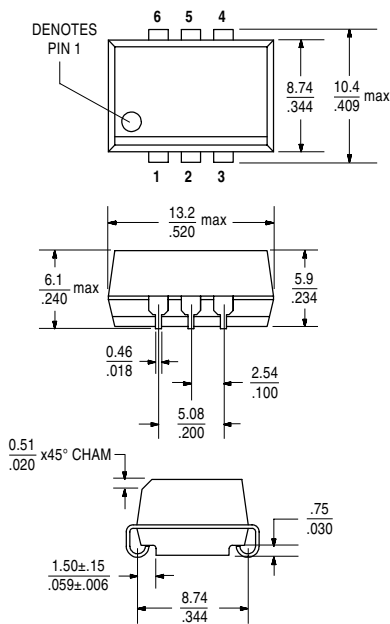
S1328 Series

Tri-State Logic Table

Pin 2 Input	Pin 4 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 2:
 Logic 1 = 2.4V min
 Logic 0 = 0.5V max

Package Details

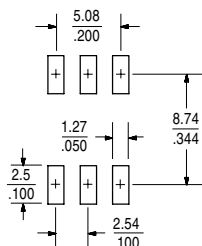


Pin Functions:

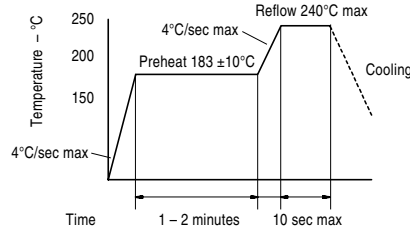
Pin 1: Control Voltage Pin 4: Output
 Pin 2: Tri-State Control Pin 5: N/C
 Pin 3: GND Pin 6: +3.3VDC

Scale: None (Dimensions in mm / inches)

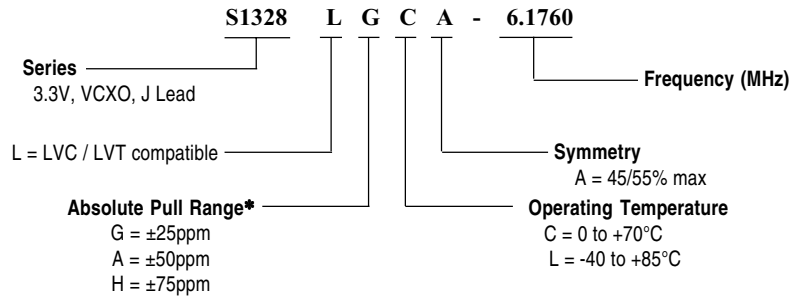
Recommended Land Pattern



Solder Reflow Guide

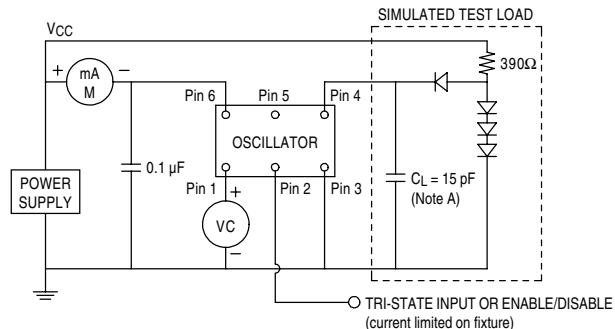


Part Numbering Guide

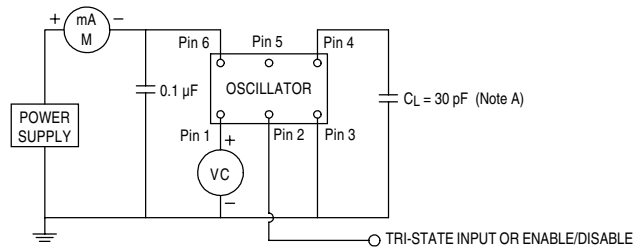


* APR = (VCXO Pull relative to specified Output Frequency) - (VCXO Frequency Stability) - (Aging)

Test Circuits



NOTE A: CL includes probe and jig capacitance.
TTL TEST CIRCUIT



NOTE A: CL includes probe and jig capacitance.
HCMOS TEST CIRCUIT

All specifications are subject to change without notice.

DS-194 REV A

5.10.2