

Document Title

1Mx16 bit Page Mode Uni-Transistor Random Access Memory

Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|---------------------|----------------|-------------------|---------------|
| 0.0                 | Initial Draft  | December 12, 2003 | Preliminary   |

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# K1S1616BCA

## 1M x 16 bit Page Mode Uni-Transistor CMOS RAM

### FEATURES

- Process Technology: CMOS
- Organization: 1M x16 bit
- Power Supply Voltage: 1.7~2.1V
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page read mode
- Package Type: 48-FBGA-6.00x7.00

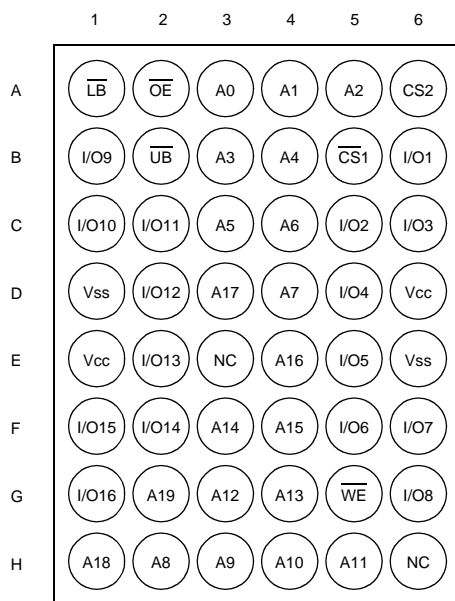
### GENERAL DESCRIPTION

The K1S1616BCA is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device support 4 page mode operation, Industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports deep power down mode for low standby current.

### PRODUCT FAMILY

| Product Family | Operating Temp.      | Vcc Range | Speed (trc) | Power Dissipation                 |                                     | PKG Type          |
|----------------|----------------------|-----------|-------------|-----------------------------------|-------------------------------------|-------------------|
|                |                      |           |             | Standby (I <sub>SB1</sub> , Max.) | Operating (I <sub>CC2</sub> , Max.) |                   |
| K1S1616BCA-I   | Industrial(-40~85°C) | 1.7~2.1V  | 70/85ns     | 80µA                              | 30mA                                | 48-FBGA-6.00x7.00 |

### PIN DESCRIPTION

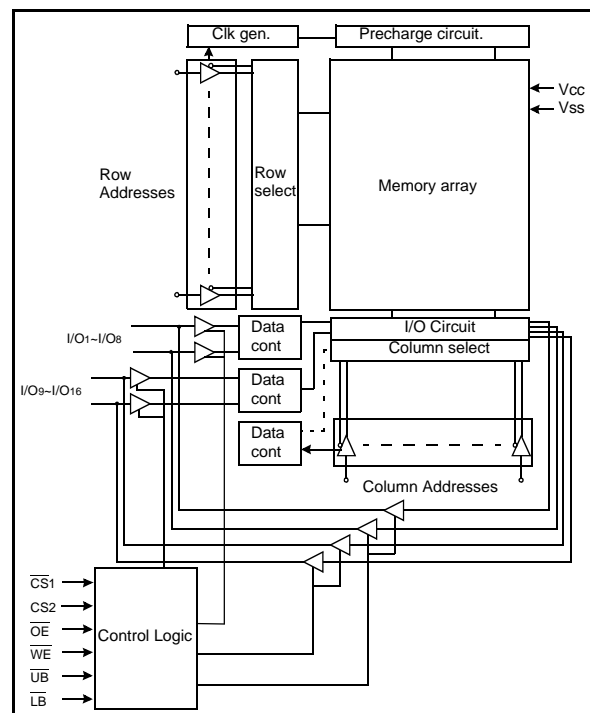


48-FBGA: Top View(Ball Down)

| Name            | Function            | Name            | Function                    |
|-----------------|---------------------|-----------------|-----------------------------|
| CS1,CS2         | Chip Select Inputs  | Vcc             | Power                       |
| $\overline{OE}$ | Output Enable Input | Vss             | Ground                      |
| $\overline{WE}$ | Write Enable Input  | $\overline{UB}$ | Upper Byte(I/O9~16)         |
| A0~A19          | Address Inputs      | $\overline{LB}$ | Lower Byte(I/O1~8)          |
| I/O1~I/O16      | Data Inputs/Outputs | NC              | No Connection <sup>1)</sup> |

1) Reserved for future use

### FUNCTIONAL BLOCK DIAGRAM



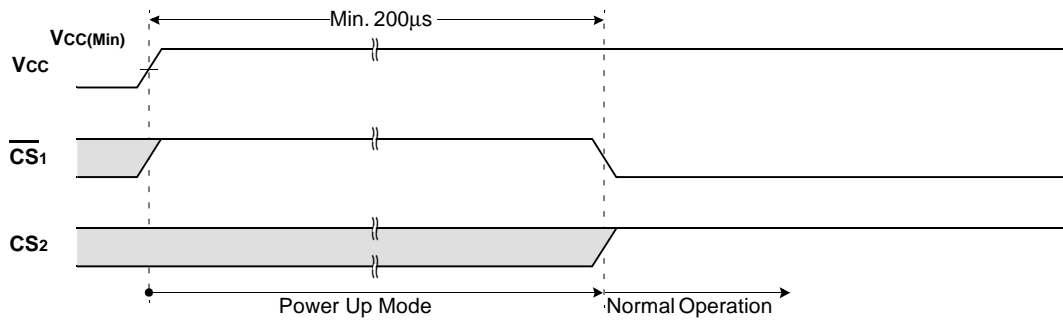
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# K1S1616BCA

## POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power ( $V_{CC} \text{ min.} = 1.7V$ ) for a minimum  $200\mu s$  with  $\overline{CS1} = \text{high}$  or  $CS2 = \text{low}$ .

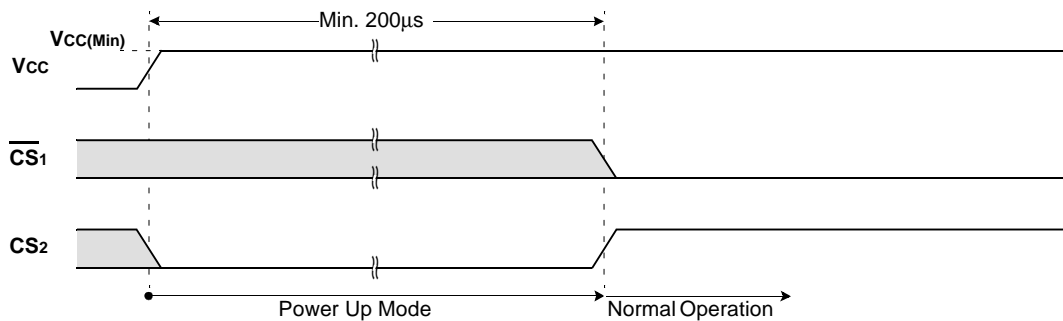
### TIMING WAVEFORM OF POWER UP(1) ( $\overline{CS1}$ controlled)



#### POWER UP(1)

1. After Vcc reaches Vcc(Min.), wait  $200\mu s$  with  $\overline{CS1}$  high. Then the device gets into the normal operation.

### TIMING WAVEFORM OF POWER UP(2) ( $CS2$ controlled)



#### POWER UP(2)

1. After Vcc reaches Vcc(Min.), wait  $200\mu s$  with CS2 low. Then the device gets into the normal operation.

**FUNCTIONAL DESCRIPTION**

| $\overline{CS1}$ | $CS2$           | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | $I/O_{1-8}$ | $I/O_{9-16}$ | Mode             | Power   |
|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------|--------------|------------------|---------|
| H                | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | High-Z      | High-Z       | Deselected       | Standby |
| X <sup>1)</sup>  | L               | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | High-Z      | High-Z       | Deselected       | Standby |
| X <sup>1)</sup>  | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | H               | H               | High-Z      | High-Z       | Deselected       | Standby |
| L                | H               | H               | H               | L               | X <sup>1)</sup> | High-Z      | High-Z       | Output Disabled  | Active  |
| L                | H               | H               | H               | X <sup>1)</sup> | L               | High-Z      | High-Z       | Output Disabled  | Active  |
| L                | H               | L               | H               | L               | H               | Dout        | High-Z       | Lower Byte Read  | Active  |
| L                | H               | L               | H               | H               | L               | High-Z      | Dout         | Upper Byte Read  | Active  |
| L                | H               | L               | H               | L               | L               | Dout        | Dout         | Word Read        | Active  |
| L                | H               | X <sup>1)</sup> | L               | L               | H               | Din         | High-Z       | Lower Byte Write | Active  |
| L                | H               | X <sup>1)</sup> | L               | H               | L               | High-Z      | Din          | Upper Byte Write | Active  |
| L                | H               | X <sup>1)</sup> | L               | L               | L               | Din         | Din          | Word Write       | Active  |

1. X means don't care.(Must be low or high state)

**ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>**

| Item                                  | Symbol                             | Ratings                       | Unit |
|---------------------------------------|------------------------------------|-------------------------------|------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>OUT</sub> | -0.2 to V <sub>CC</sub> +0.3V | V    |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub>                    | -0.2 to 2.5V                  | V    |
| Power Dissipation                     | P <sub>D</sub>                     | 1.0                           | W    |
| Storage temperature                   | T <sub>STG</sub>                   | -65 to 150                    | °C   |
| Operating Temperature                 | T <sub>A</sub>                     | -40 to 85                     | °C   |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

## PRODUCT LIST

| Industrial Temperature Product(-40~85°C) |                         |
|------------------------------------------|-------------------------|
| Part Name                                | Function                |
| K1S1616BCA-FI70                          | 48-FBGA-6.00x7.00, 70ns |
| K1S1616BCA-FI85                          | 48-FBGA-6.00x7.00, 85ns |
| K1S1616BCA-BI70 <sup>1)</sup>            | 48-FBGA-6.00x7.00, 70ns |
| K1S1616BCA-BI85 <sup>1)</sup>            | 48-FBGA-6.00x7.00, 85ns |

1. Lead Free Product

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

| Item               | Symbol          | Min                | Typ     | Max                                | Unit |
|--------------------|-----------------|--------------------|---------|------------------------------------|------|
| Supply voltage     | V <sub>CC</sub> | 1.7                | 1.8/2.0 | 2.1                                | V    |
| Ground             | V <sub>SS</sub> | 0                  | 0       | 0                                  | V    |
| Input high voltage | V <sub>IH</sub> | 1.4                | -       | V <sub>CC</sub> +0.3 <sup>2)</sup> | V    |
| Input low voltage  | V <sub>IL</sub> | -0.2 <sup>3)</sup> | -       | 0.4                                | V    |

1. T<sub>A</sub>=-40 to 85°C, otherwise specified.
2. Overshoot: V<sub>CC</sub>+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup>(f=1MHz, T<sub>A</sub>=25°C)

| Item                     | Symbol          | Test Condition      | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance        | C <sub>IN</sub> | V <sub>IN</sub> =0V | -   | 8   | pF   |
| Input/Output capacitance | C <sub>IO</sub> | V <sub>IO</sub> =0V | -   | 10  | pF   |

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

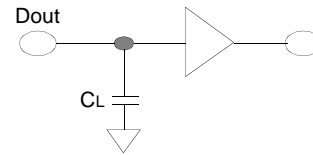
| Item                      | Symbol                         | Test Conditions                                                                                                                                                                    | Min | Typ <sup>1)</sup> | Max | Unit |
|---------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|-----|------|
| Input leakage current     | I <sub>LI</sub>                | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>                                                                                                                                | -1  | -                 | 1   | μA   |
| Output leakage current    | I <sub>LO</sub>                | $\overline{CS}=V_{IH}, \overline{ZZ}=V_{IH}, \overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}, V_{IO}=V_{SS}$ to V <sub>CC</sub>                                                     | -1  | -                 | 1   | μA   |
| Average operating current | I <sub>CC1</sub>               | Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS} \leq 0.2V$ , $\overline{ZZ} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V    | -   | -                 | 5   | mA   |
|                           | I <sub>CC2</sub>               | Cycle time=t <sub>RC</sub> +3t <sub>PC</sub> , I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}=V_{IL}, \overline{ZZ}=V_{IH}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> | -   | -                 | 30  | mA   |
| Output low voltage        | V <sub>OL</sub>                | I <sub>OL</sub> =0.1mA                                                                                                                                                             | -   | -                 | 0.2 | V    |
| Output high voltage       | V <sub>OH</sub>                | I <sub>OH</sub> =-0.1mA                                                                                                                                                            | 1.4 | -                 | -   | V    |
| Standby Current(CMOS)     | I <sub>SB1</sub> <sup>2)</sup> | $\overline{CS} \geq V_{CC}-0.2V, \overline{ZZ} \geq V_{CC}-0.2V$ , Other inputs=V <sub>SS</sub> to V <sub>CC</sub>                                                                 | -   | -                 | 80  | μA   |

1. Typical values are tested at V<sub>CC</sub>=1.8V, T<sub>A</sub>=25°C and not guaranteed.

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to  $V_{CC}-0.2V$   
 Input rising and falling time: 5ns  
 Input and output reference voltage:  $0.5 \times V_{CC}$   
 Output load (See right):  $C_L=50pF$



1. Including scope and jig capacitance

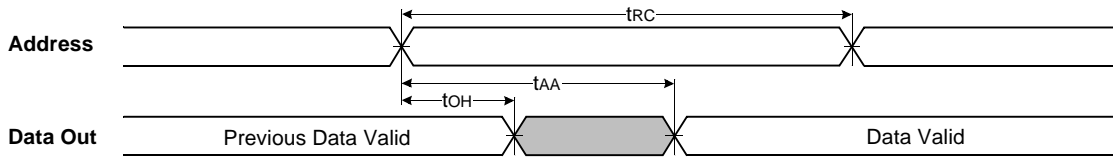
## AC CHARACTERISTICS ( $V_{CC}=1.7\sim 2.1V$ , $T_A=-40$ to $85^\circ C$ )

| Parameter List   |                                                            | Symbol           | Speed Bins       |     |                  |     | Units |
|------------------|------------------------------------------------------------|------------------|------------------|-----|------------------|-----|-------|
|                  |                                                            |                  | 70ns             |     | 85ns             |     |       |
|                  |                                                            |                  | Min              | Max | Min              | Max |       |
| Read             | Read Cycle Time                                            | t <sub>RC</sub>  | 70               | -   | 85               | -   | ns    |
|                  | Address Access Time                                        | t <sub>AA</sub>  | -                | 70  | -                | 85  | ns    |
|                  | Chip Select to Output                                      | t <sub>CO</sub>  | -                | 70  | -                | 85  | ns    |
|                  | Output Enable to Valid Output                              | t <sub>OE</sub>  | -                | 35  | -                | 40  | ns    |
|                  | $\overline{UB}$ , $\overline{LB}$ Access Time              | t <sub>BA</sub>  | -                | 70  | -                | 85  | ns    |
|                  | Chip Select to Low-Z Output                                | t <sub>LZ</sub>  | 10               | -   | 10               | -   | ns    |
|                  | $\overline{UB}$ , $\overline{LB}$ Enable to Low-Z Output   | t <sub>BLZ</sub> | 10               | -   | 10               | -   | ns    |
|                  | Output Enable to Low-Z Output                              | t <sub>OLZ</sub> | 5                | -   | 5                | -   | ns    |
|                  | Chip Disable to High-Z Output                              | t <sub>HZ</sub>  | 0                | 25  | 0                | 25  | ns    |
|                  | $\overline{UB}$ , $\overline{LB}$ Disable to High-Z Output | t <sub>BHZ</sub> | 0                | 25  | 0                | 25  | ns    |
|                  | Output Disable to High-Z Output                            | t <sub>OHZ</sub> | 0                | 25  | 0                | 25  | ns    |
|                  | Output Hold from Address Change                            | t <sub>OH</sub>  | 5                | -   | 5                | -   | ns    |
|                  | Page Cycle                                                 | t <sub>PC</sub>  | 25               | -   | 25               | -   | ns    |
| Page Access Time | t <sub>PA</sub>                                            | -                | 20               | -   | 20               | ns  |       |
| Write            | Write Cycle Time                                           | t <sub>WC</sub>  | 70               | -   | 85               | -   | ns    |
|                  | Chip Select to End of Write                                | t <sub>CW</sub>  | 60               | -   | 70               | -   | ns    |
|                  | Address Set-up Time                                        | t <sub>AS</sub>  | 0                | -   | 0                | -   | ns    |
|                  | Address Valid to End of Write                              | t <sub>AW</sub>  | 60               | -   | 70               | -   | ns    |
|                  | $\overline{UB}$ , $\overline{LB}$ Valid to End of Write    | t <sub>BW</sub>  | 60               | -   | 70               | -   | ns    |
|                  | Write Pulse Width                                          | t <sub>WP</sub>  | 55 <sup>1)</sup> | -   | 60 <sup>1)</sup> | -   | ns    |
|                  | Write Recovery Time                                        | t <sub>WR</sub>  | 0                | -   | 0                | -   | ns    |
|                  | Write to Output High-Z                                     | t <sub>WHZ</sub> | 0                | 25  | 0                | 25  | ns    |
|                  | Data to Write Time Overlap                                 | t <sub>DW</sub>  | 30               | -   | 35               | -   | ns    |
|                  | Data Hold from Write Time                                  | t <sub>DH</sub>  | 0                | -   | 0                | -   | ns    |
|                  | End Write to Output Low-Z                                  | t <sub>OW</sub>  | 5                | -   | 5                | -   | ns    |

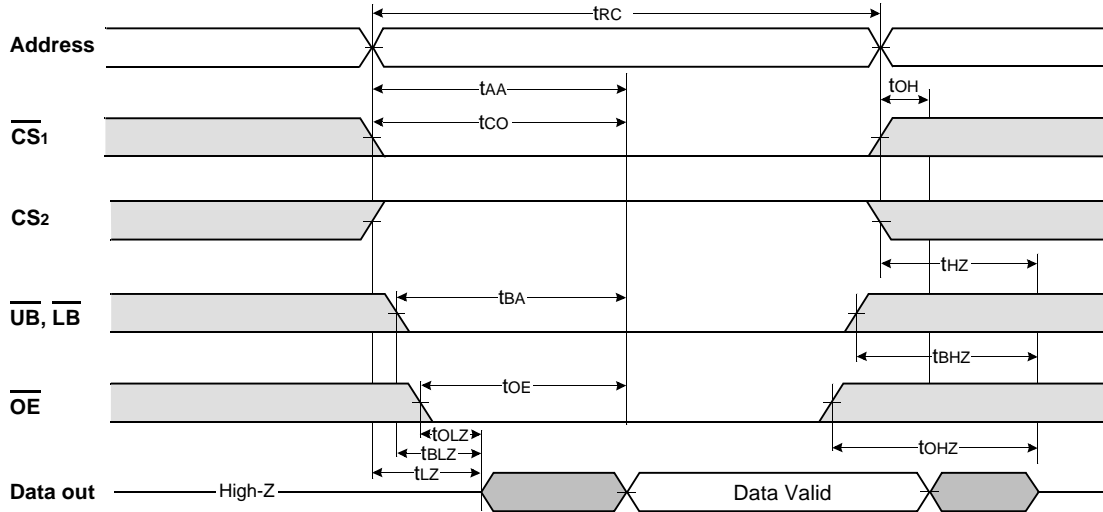
1. t<sub>WP</sub>(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

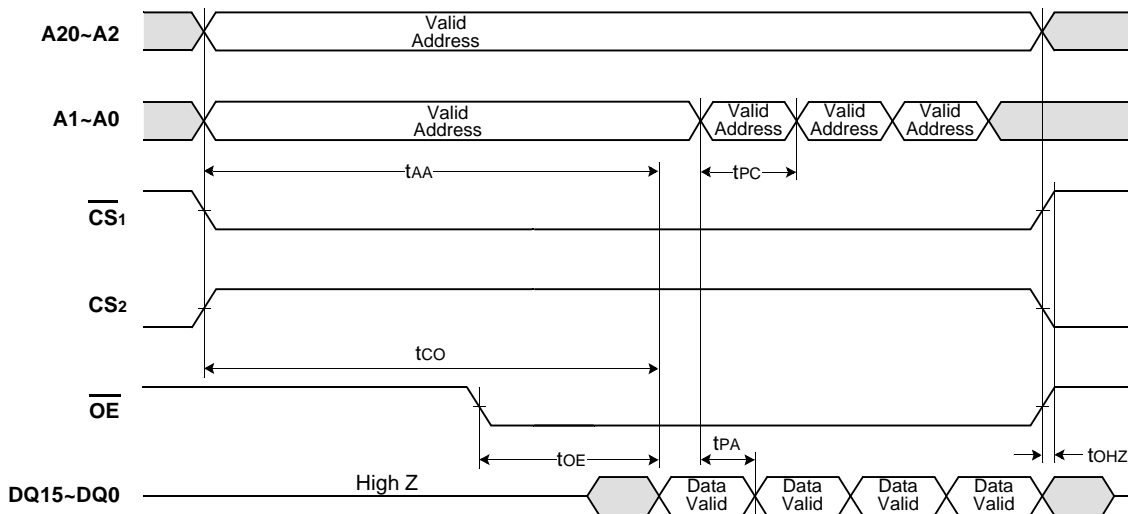
TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



TIMING WAVEFORM OF READ CYCLE(2)( $\overline{WE}=V_{IH}$ )



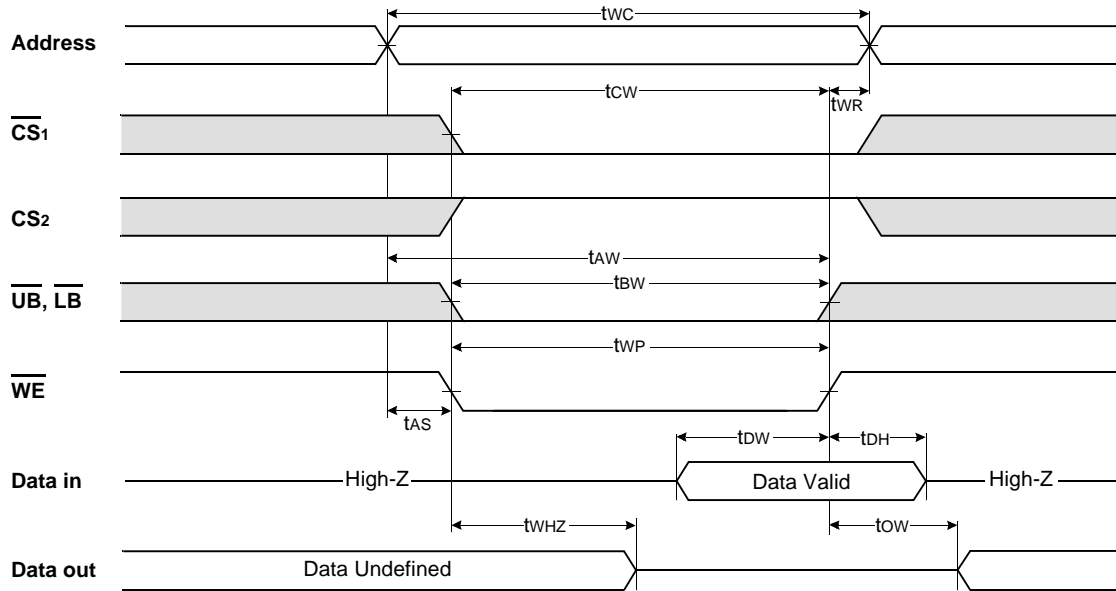
TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)



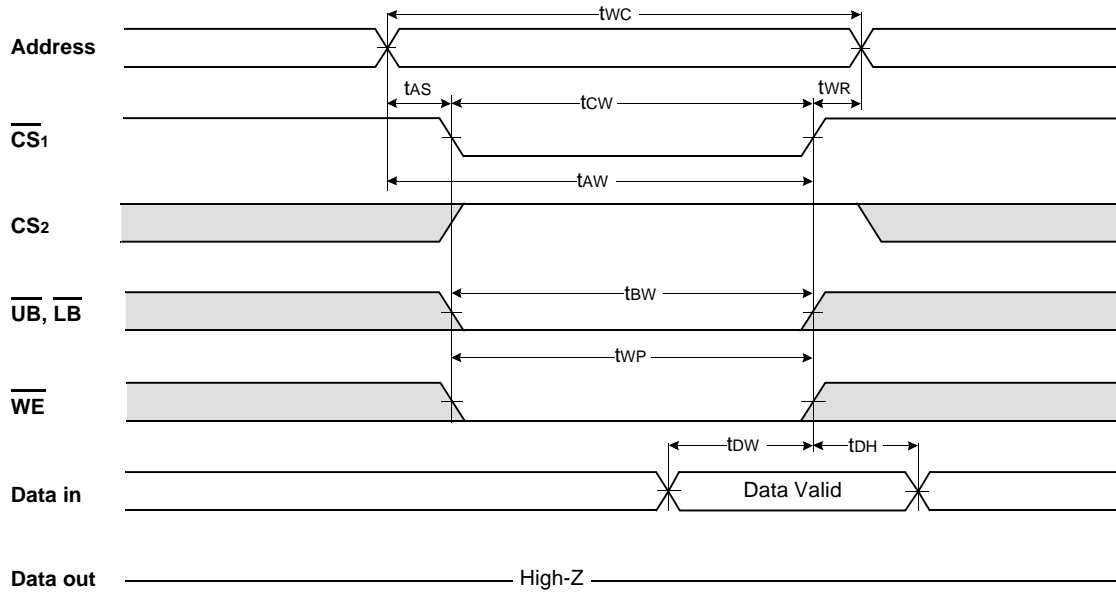
(READ CYCLE)

1.  $t_{HZ}$  and  $t_{OZH}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.
3.  $t_{OE}(\text{max})$  is met only when  $\overline{OE}$  becomes enabled after  $t_{AA}(\text{max})$ .
4. If invalid address signals shorter than min.  $t_{RC}$  are continuously repeated for over 4 $\mu\text{s}$ , the device needs a normal read timing( $t_{RC}$ ) or needs to sustain standby state for min.  $t_{RC}$  at least once in every 4 $\mu\text{s}$ .

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)

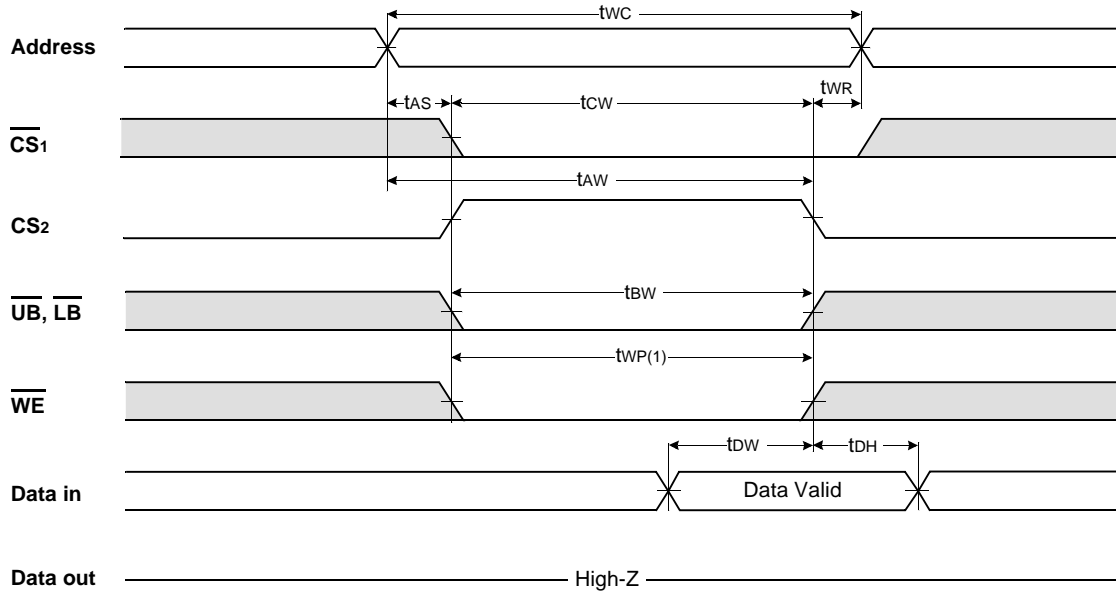


TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)

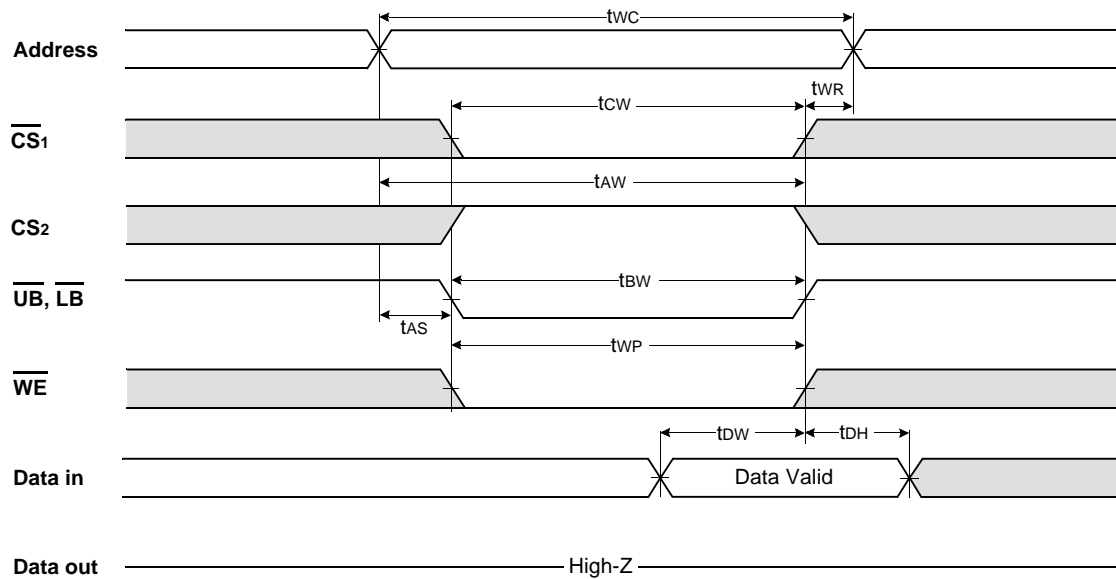




**TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)**



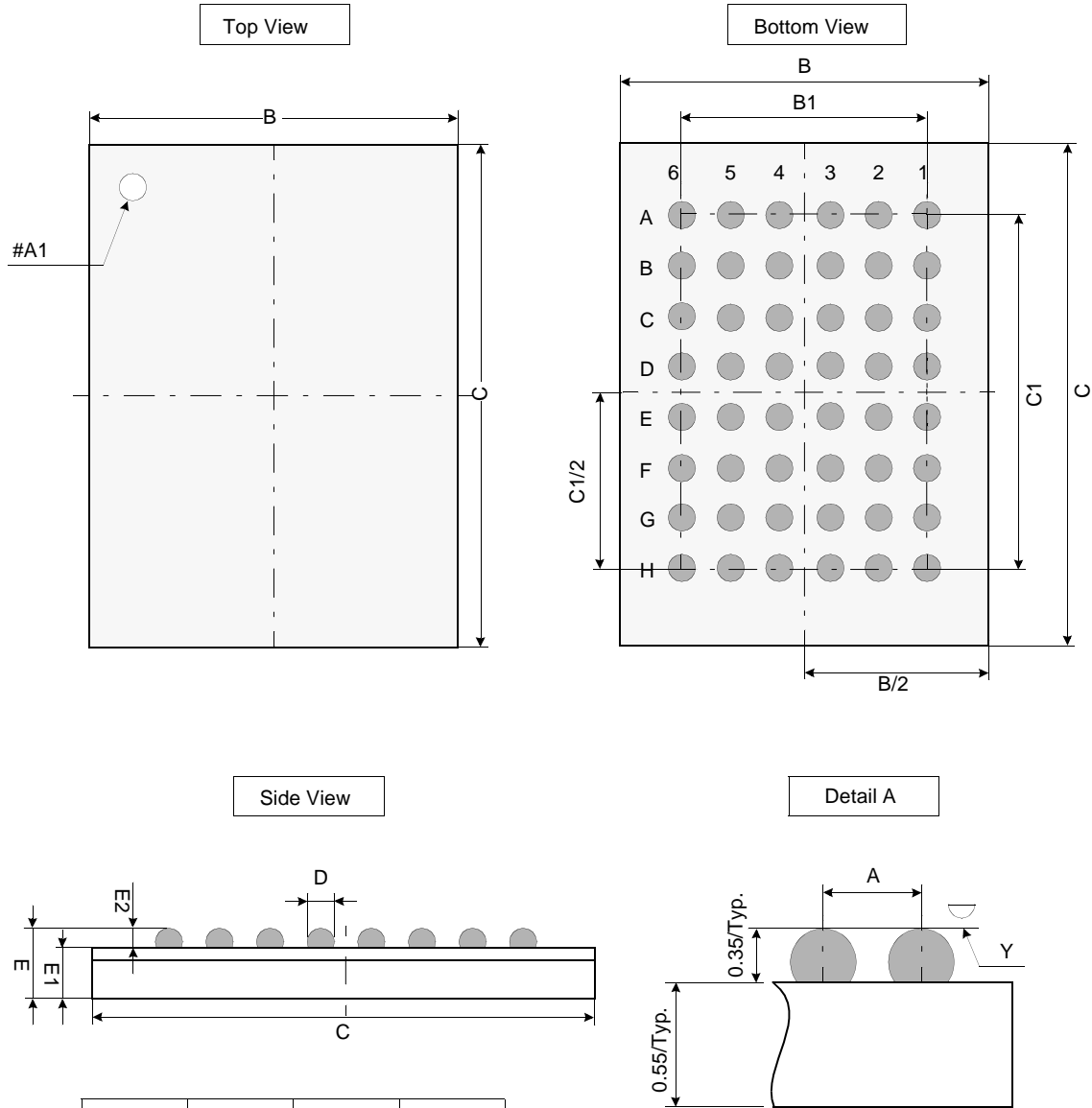
**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap(tWP) of low  $\overline{CS1}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS1}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS1}$  goes high and  $\overline{WE}$  goes high. The tWP is measured from the beginning of write to the end of write.
2. tcw is measured from the  $\overline{CS1}$  going low to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends with  $\overline{CS1}$  or  $\overline{WE}$  going high.

## PACKAGE DIMENSION

Unit: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)



|    | Min  | Typ  | Max  |
|----|------|------|------|
| A  | -    | 0.75 | -    |
| B  | 5.90 | 6.00 | 6.10 |
| B1 | -    | 3.75 | -    |
| C  | 7.90 | 8.00 | 8.10 |
| C1 | -    | 5.25 | -    |
| D  | 0.40 | 0.45 | 0.50 |
| E  | -    | 0.90 | 1.00 |
| E1 | -    | 0.55 | -    |
| E2 | 0.30 | 0.35 | 0.40 |
| Y  | -    | -    | 0.10 |

### Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are  $\pm 0.050$  unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.10(Max)