

**Features**

- 184 Pin Registered 67,108,864 x 72 bit Organization DDR SDRAM Modules
- Utilizes High Performance 64M x 4 DDR SDRAM in TSOPII-66 Packages
- Single +2.5V (± 0.2V) Power Supply
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are SSTL-2 Compatible
- 8192 Refresh Cycles every 64 ms
- Serial Presence Detect (SPD)
- DDR SDRAM Performance

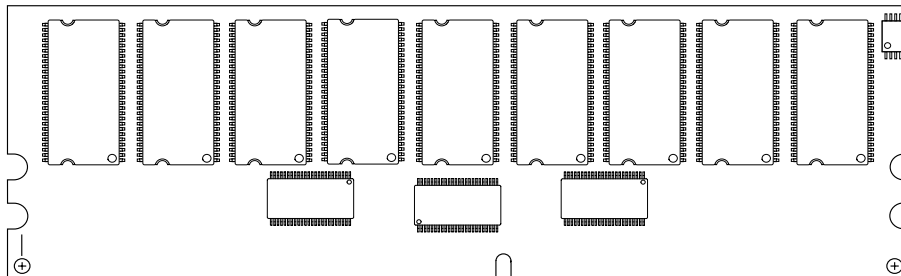
**Description**

The V827464N24S memory module is organized 67,108,864 x 72 bits in a 184 pin memory module. The 64M x 72 memory module uses 18 Mosel-Vitellic 64M x 4 DDR SDRAM. The x72 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

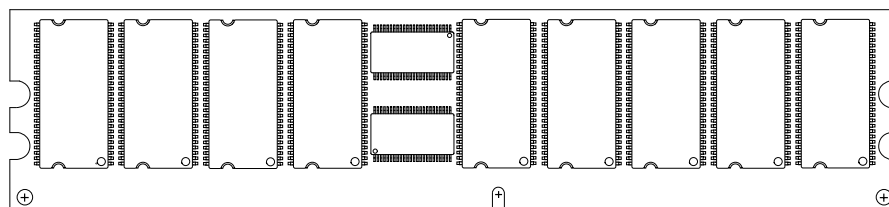
	<b>Component Used</b>	<b>-6</b>	<b>-7</b>	<b>-75</b>	<b>-8</b>
t <sub>CK</sub>	Clock Frequency (max.)	166 (PC333)	143 (PC266A)	133 (PC266B)	125 (PC200)
t <sub>AC</sub>	Clock Access Time CAS Latency = 2.5	6	7	7.5	8

<b>Module Speed</b>	
A1	PC1600 (100MHz @ CL2)
B0	PC2100B (133MHz @ CL2.5)
B1	PC2100A (133MHz @ CL2)
C0	PC2700 (166MHz @ CL2.5)

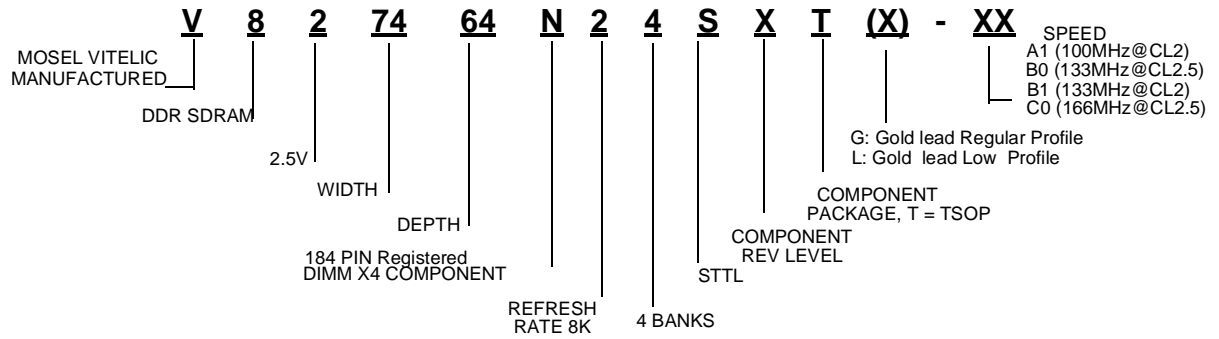
**Standard Module**



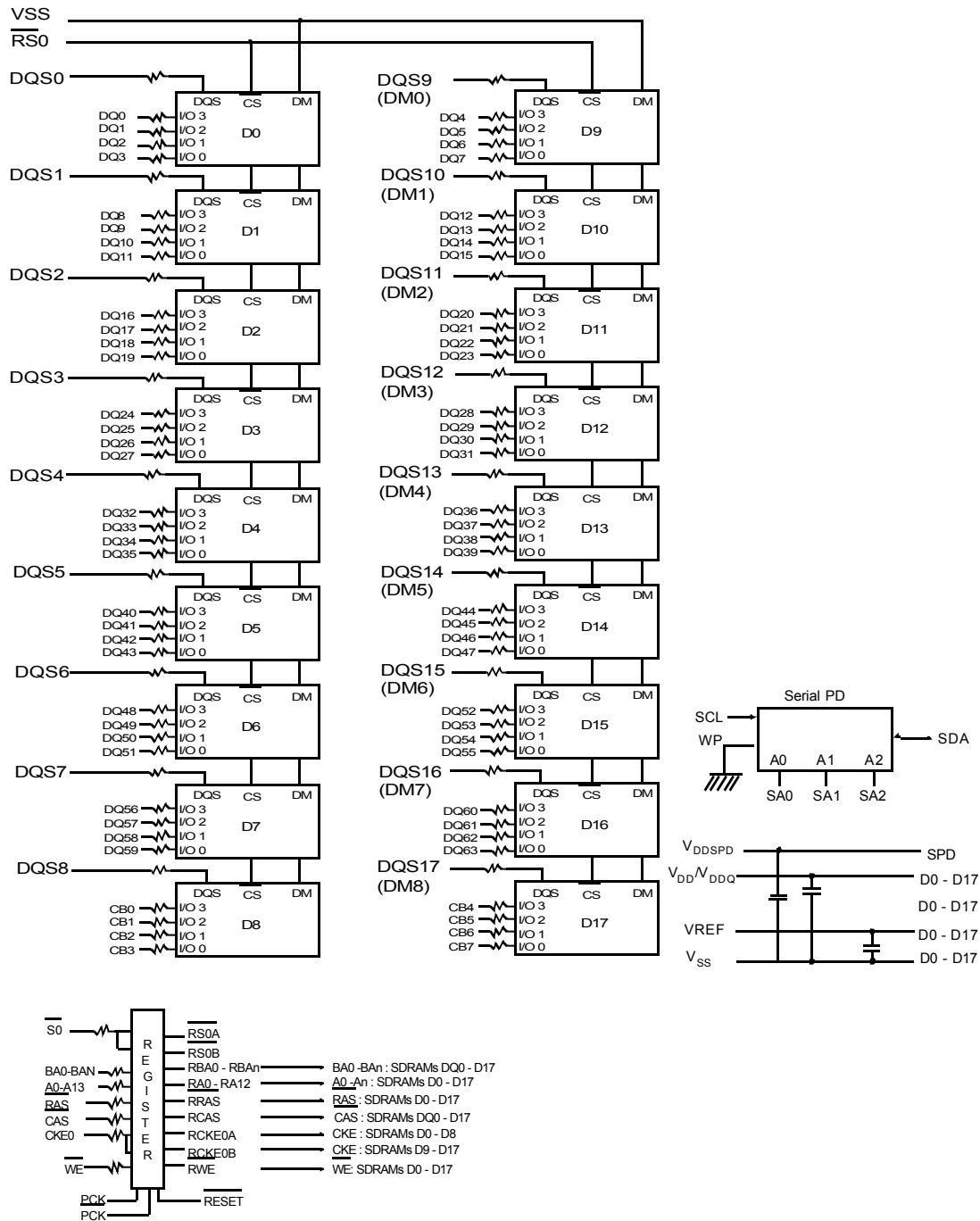
**Low Profile Module**



**Part Number Information**



Block Diagram



**Pin Configurations (Front Side/Back Side)**

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	RAS
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	A13*	134	CB4*	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5*	165	DQ52
13	DQ9	44	CB0*	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1*	75	$\overline{CK2}$	106	DQ13	137	$\overline{CK0}$ *	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	$\overline{CK0}$ *	168	VDD
16	CK1	47	DQS8*	77	VDDQ	108	VDD	139	VSS	169	DM6
17	$\overline{CK1}$	48	A0	78	DQS6	109	DQ14	140	DM8*	170	DQ54
18	VSS	49	CB2*	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6*	172	VDDQ
20	DQ11	51	CB3*	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7*	174	DQ60
22	VDDQ	Key		83	DQ56	114	DQ20	Key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

**Pin Names**

Pin	Pin Description
CK1, $\overline{CK1}$ , CK2, $\overline{CK2}$	Differential Clock Inputs
$\overline{CS0}$	Chip Select Input
CKE0	Clock Enable Input
RAS, $\overline{CAS}$ , $\overline{WE}$	Command Sets Inputs
A0 ~ A12	Address
BA0, BA1	Bank Address
DQ0~DQ63	Data Inputs/Outputs
DQS0~DQS7	Data Strobe Inputs/Outputs
DM0~DM7	Data-in Mask

Pin	Pin Description
VDD	Power Supply
VDDQ	DQs Power Supply
VSS	Ground
VREF	Reference Power Supply
VDDSPD	Power Supply for SPD
SA0~SA2	E <sup>2</sup> PROM Address Inputs
SCL	E <sup>2</sup> PROM Clock
SDA	E <sup>2</sup> PROM Data I/O
VDDID	VDD Identification Flag
DU	Do not Use
NC	No Connection

**Serial Presence Detect Information**

Bin Sort:

C0 (PC2700 @ CL2.5)

A1 (PC1600 @ CL2)

B0 (PC2100B @ CL2.5)

B1 (PC2100A @ CL2)

Byte #	Function described	Function Supported				Hex value			
		A1	B0	B1	C0	A1	B0	B1	C0
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes				80h			
1	Total # of Bytes of SPD memory device	256bytes				08h			
2	Fundamental memory type	SDRAM DDR				07h			
3	# of row address on this assembly	13				0Dh			
4	# of column address on this assembly	11				0Bh			
5	# of module Rows on this assembly	1 Bank				01h			
6	Data width of this assembly	72 bits				48h			
7	.....Data width of this assembly	-				00h			
8	VDDQ and interface standard of this assembly	SSTL 2.5V				04h			
9	DDR SDRAM cycle time at CAS Latency =2.5	8ns	7.5ns	7ns	6ns	80h	75h	70h	60h
10	DDR SDRAM Access time from clock at CL=2.5	±0.8ns	±0.75n	±0.75n	±0.70n	80h	75h	75h	70h
11	DIMM configuration type(Non-parity, Parity, ECC)	Non-parity, ECC				02h			
12	Refresh rate & type	7.8us & Self refresh				82h			
13	Primary DDR SDRAM width	x4				04h			
14	Error checking DDR SDRAM data width	x4				04h			
15	Minimum clock delay for back-to-back random column address	t <sub>CCD</sub> =1CLK				01h			
16	DDR SDRAM device attributes : Burst lengths supported	2,4,8				0Eh			
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	4 banks				04h			
18	DDR SDRAM device attributes : CAS Latency supported	2,2.5				0Ch			
19	DDR SDRAM device attributes : CS Latency	0CLK				01h			
20	DDR SDRAM device attributes : WE Latency	1CLK				02h			
21	DDR SDRAM module attributes	Registered address & control inputs and On-card DLL				26h			
22	DDR SDRAM device attributes : General	+/-0.2V voltage tolerance				00h			
23	DDR SDRAM cycle time at CL =2	10ns	10ns	7.5ns	7.5ns	A0h	A0h	75h	75h
24	DDR SDRAM Access time from clock at CL =2	±0.8ns	±0.75ns	±0.75ns	±0.70ns	80h	75h	75h	70h
25	DDR SDRAM cycle time at CL =1.5	-	-	-	-	00h			
26	DDR SDRAM Access time from clock at CL =1.5	-	-	-	-	00h			
27	Minimum row precharge time (=t <sub>RP</sub> )	20ns	20ns	20ns	18ns	50h	50h	50h	48h

**Serial Presence Detect Information (cont.)**

Byte #	Function described	Function Supported				Hex value			
		A1	B0	B1	C0	A1	B0	B1	C0
28	Minimum row activate to row active delay(=t <sub>RRD</sub> )	15ns	15ns	15ns	12ns	3Ch	3Ch	38h	30h
29	Minimum RAS to CAS delay(=t <sub>RCD</sub> )	20ns	20ns	20ns	18ns	50h	50h	48h	48h
30	Minimum active to precharge time(=t <sub>RAS</sub> )	50ns	45ns	45ns	42ns	32h	2Dh	2Dh	2Ah
31	Module Row density	256MB				40h			
32	Command and address signal input setup time	1.1ns	0.9ns	0.9ns	0.75ns	B0h	90h	90h	75h
33	Command and address signal input hold time	1.1ns	0.9ns	0.9ns	0.75ns	B0h	90h	90h	75h
34	Data signal input setup time	0.6ns	0.5ns	0.5ns	0.45ns	60h	50h	50h	45h
35	Data signal input hold time	0.6ns	0.5ns	0.5ns	0.45ns	60h	50h	50h	45h
36-40	Superset information (may be used in future)	-				00h			
41	SDRAM device minimum active to active/auto-refresh time (=t <sub>RC</sub> )	70ns	65ns	65ns	60ns	46h	41h	3Ch	3Ch
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t <sub>RFC</sub> )	80ns	75ns	75ns	72ns	50h	4Bh	4Bh	48h
43	SDRAM device maximum device cycle time (=t <sub>CK MAX</sub> )	12ns	12ns	12ns	12ns	30h	30h	30h	30h
44	SDRAM device maximum skew between DQS and DQ signals (=t <sub>DQSQ</sub> )	0.6ns	0.5ns	0.5ns	0.45ns	3Ch	32h	32h	2Dh
45	SDRAM device maximum read datahold skew factor (=t <sub>QHS</sub> )	1ns	0.75ns	0.75ns	0.60ns	A0h	75h	75h	60h
62	SPD data revision code	Initial release				00h			
63	Checksum for Bytes 0 ~ 62	-				38h	73h	2Ah	9Ch
64	Manufacturer JEDEC ID code	Mosel Vitelic				40h			
65 -71	..... Manufacturer JEDEC ID code					00h			
72	Manufacturing location	02=Taiwan 05=China 0A=S-CH							
73-90	Module part number (ASCII)	V827464N24S							
91	Manufacturer revision code (For PCB)	0				00			
92	Manufacturer revision code (For component)	0				00			
93	Manufacturing date (Week)	-				-			
94	Manufacturing date (Year)	-				-			
95~98	Assembly serial #	-				-			
99~127	Manufacturer specific data (may be used in future)	Undefined				00h			
128~255	Open for customer use	Undefined				00h			

**DC Operating Conditions**

( $T_A = 0$  to  $70^\circ\text{C}$ , Voltage referenced to  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V	
Power Supply Voltage	$V_{DDQ}$	2.3	2.5	2.7	V	1
Input High Voltage	$V_{IH}$	$V_{REF} + 0.15$	-	$V_{DDQ} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3	-	$V_{REF} - 0.15$	V	2
I/O Termination Voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	
Reference Voltage	$V_{REF}$	1.15	1.25	1.35	V	3
Input Leakage Current	$I_I$	-2	-	2	$\mu\text{A}$	
Output Leakage Current	$IO_z$	-5	-	5	$\mu\text{A}$	
Output High Current ( $V_{OUT} = 1.95\text{V}$ )	$IO_H$	-16.8	-	-	mA	
Output Low Current ( $V_{OUT} = 0.35\text{V}$ )	$IO_L$	16.8	-	-	mA	

- Notes:**
- $V_{DDQ}$  must not exceed the level of  $V_{DD}$ .
  - $V_{IL}$  (min) is acceptable -1.5V AC pulse width with  $\delta$  5ns of duration.
  - The value of  $V_{REF}$  is approximately equal to  $0.5V_{DDQ}$ .

**AC Operating Conditions**

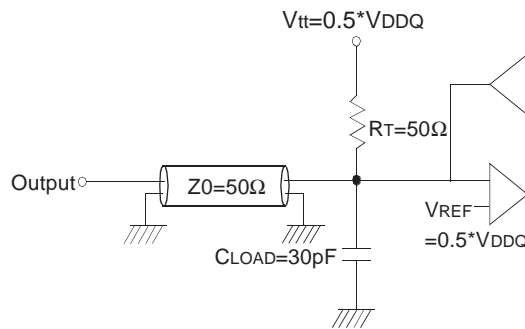
( $T_A = 0$  to  $70^\circ\text{C}$ , Voltage referenced to  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	$V_{REF} + 0.31$		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL(AC)}$		$V_{REF} - 0.31$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	$V_{DDQ} + 0.6$	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	$0.5 \cdot V_{DDQ} - 0.2$	$0.5 \cdot V_{DDQ} + 0.2$	V	2

- Notes:**
- $V_{ID}$  is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .
  - The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.

**AC Operating Test Conditions** ( $T_A = 0$  to  $70^\circ\text{C}$ , Voltage referenced to  $V_{SS} = 0\text{V}$ )

Parameter	Value	Unit
Reference Voltage	$V_{DDQ} \times 0.5$	V
Termination Voltage	$V_{DDQ} \times 0.5$	V
AC Input High Level Voltage ( $V_{IH, \text{min}}$ )	$V_{REF} + 0.31$	V
AC Input Low Level Voltage ( $V_{IL, \text{max}}$ )	$V_{REF} - 0.31$	V
Input Timing Measurement Reference Level Voltage	$V_{REF}$	V
Output Timing Measurement Reference Level Voltage	$V_{TT}$	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor ( $R_T$ )	50	Ohm
Series Resistor ( $R_S$ )	25	Ohm
Output Load Capacitance for Access Time Measurement ( $C_L$ )	30	pF



Output Load Circuit (SSTL\_2)

**Input/Output Capacitance**

( $V_{DD} = 2.5\text{V}$ ,  $V_{DDQ} = 2.5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Min	Max	Unit
Input capacitance ( $A_0 \sim A_{11}$ , $BA_0 \sim BA_1$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{IN1}$	60	75	pF
Input capacitance ( $CKE_0$ )	$C_{IN2}$	40	48	pF
Input capacitance ( $\overline{CS}_0$ )	$C_{IN3}$	40	48	pF
Input capacitance ( $CLK_1$ , $CLK_2$ )	$C_{IN4}$	30	32	pF
Data & DQS input/output capacitance ( $DQ_0 \sim DQ_{63}$ )	$C_{OUT}$	10	12	pF
Input capacitance ( $DM_0 \sim DM_8$ )	$C_{IN5}$	10	12	pF



**DDR SDRAM I<sub>DD</sub> SPEC TABLE**

Symbol		A1 PC1600@CL2	B0 PC2100B@CL2.5	B1 PC2100A@CL2	C0 PC2700@CL2.5	Unit
IDD0		1640	1860	1860	1990	mA
IDD1		1860	2180	2180	2540	mA
IDD2P		280	380	380	460	mA
IDD2F		640	640	640	280	mA
IDD2Q		640	740	740	190	mA
IDD3P		280	380	380	370	mA
IDD3N		1100	1280	1280	550	mA
IDD4R		2700	3440	3440	1700	mA
IDD4W		2360	3080	3080	1600	mA
IDD5		3260	3440	3440	1800	mA
IDD6	Normal	54	54	54	30	mA
	Low power	33	33	33	33	mA
IDD7		4600	5400	5400	6400	mA

\* Module I<sub>DD</sub> was calculated on the basis of component I<sub>DD</sub> and can be differently measured according to DQ loading cap.

**Detailed test conditions for DDR SDRAM IDD1 & IDD**

**IDD1 : Operating current: One bank operation**

1. Typical Case : V<sub>dd</sub> = 2.5V, T=25' C
2. Worst Case : V<sub>dd</sub> = 2.7V, T= 10' C
3. Only one bank is accessed with t<sub>RC</sub>(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I<sub>out</sub> = 0mA
4. Timing patterns
  - DDR200(100Mhz, CL=2) : t<sub>CK</sub> = 10ns, CL2, BL=4, t<sub>RCD</sub> = 2\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
 Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing  
 \*50% of data changing at every burst
  - DDR266B(133Mhz, CL=2.5) : t<sub>CK</sub> = 7.5ns, CL=2.5, BL=4, t<sub>RCD</sub> = 3\*t<sub>CK</sub>, t<sub>RC</sub> = 9\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
 Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing  
 \*50% of data changing at every burst
  - DDR266A (133Mhz, CL=2) : t<sub>CK</sub> = 7.5ns, CL=2, BL=4, t<sub>RCD</sub> = 3\*t<sub>CK</sub>, t<sub>RC</sub> = 9\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
 Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing  
 \*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

**AC Characteristics** (AC operating conditions unless otherwise noted)

Parameter	Symbol	(PC333)		(PC266A)		(PC266B)		(PC200)		Unit	Note	
		Min	Max	Min	Max	Min	Max	Min	Max			
Row Cycle Time	t <sub>RC</sub>	60	-	65	-	65	-	70	-	ns		
Auto Refresh Row Cycle Time	t <sub>RFC</sub>	72	-	75	-	75	-	80	-	ns		
Row Active Time	t <sub>RAS</sub>	42	120K	45	120K	45	120K	50	120K	ns		
Row Address to Column Address Delay	t <sub>RCD</sub>	18	-	20	-	20	-	20	-	ns		
Row Active to Row Active Delay	t <sub>RRD</sub>	12	-	15	-	15	-	15	-	ns		
Column Address to Column Address Delay	t <sub>CCD</sub>	1	-	1	-	1	-	1	-	CLK		
Row Precharge Time	t <sub>RP</sub>	18	-	20	-	20	-	20	-	ns		
Write Recovery Time	t <sub>WR</sub>	12	-	15	-	15	-	15	-	ns		
Last Data-In to Read Command	t <sub>DRL</sub>	1	-	1	-	1	-	1	-	CLK		
Auto Precharge Write Recovery + Precharge Time	t <sub>DAL</sub>	35	-	35	-	35	-	35	-	ns		
System Clock Cycle Time	t <sub>CK</sub>	$\overline{\text{CAS}}$ Latency = 2.5	6	12	7	12	7.5	12	8	12	ns	
		$\overline{\text{CAS}}$ Latency = 2	7.5	12	7.5	12	10	12	10	12	ns	
Clock High Level Width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK		
Clock Low Level Width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK		
Data-Out edge to Clock edge Skew	t <sub>AC</sub>	-0.75	0.75	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns		
DQS-Out edge to Clock edge Skew	t <sub>DQSCK</sub>	-0.75	0.75	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns		
DQS-Out edge to Data-Out edge Skew	t <sub>DQSQ</sub>	-	0.45	-	0.5	-	0.5	-	0.6	ns		
Data-Out hold time from DQS	t <sub>QH</sub>	t <sub>HPmin</sub> -0.75ns	-	t <sub>HPmin</sub> -0.75ns	-	t <sub>HPmin</sub> -0.75ns	-	t <sub>HPmin</sub> -0.75ns	-	ns	1	
Clock Half Period	t <sub>HP</sub>	t <sub>CH/L</sub> min	-	t <sub>CH/L</sub> min	-	t <sub>CH/L</sub> min	-	t <sub>CH/L</sub> min	-	ns	1	
Input Setup Time (fast slew rate)	t <sub>IS</sub>	0.75	-	0.9	-	0.9	-	1.1	-	ns	2,3,5,6	
Input Hold Time (fast slew rate)	t <sub>IH</sub>	0.75	-	0.9	-	0.9	-	1.1	-	ns	2,3,5,6	
Input Setup Time (slow slew rate)	t <sub>IS</sub>	0.8	-	1.0	-	1.0	-	1.1	-	ns	2,4,5,6	
Input Hold Time (slow slew rate)	t <sub>IH</sub>	0.8	-	1.0	-	1.0	-	1.1	-	ns	2,4,5,6	
Input Pulse Width	t <sub>IPW</sub>	0.4	0.6	2.2	-	2.2	-	-	-	ns	6	
Write DQS High Level Width	t <sub>DQSH</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK		
Write DQS Low Level Width	t <sub>DQSL</sub>	0.75	1.25	0.4	0.6	0.4	0.6	0.4	0.6	CLK		
CLK to First Rising edge of DQS-In	t <sub>DQSS</sub>	0.45	-	0.75	1.25	0.75	1.25	0.75	1.25	CLK		
Data-In Setup Time to DQS-In (DQ & DM)	t <sub>DS</sub>	0.45	-	0.5	-	0.5	-	0.6	-	ns	7	
Data-in Hold Time to DQS-In (DQ & DM)	t <sub>DH</sub>	1.75	-	0.5	-	0.5	-	0.6	-	ns	7	
DQ & DM Input Pulse Width	t <sub>DIPW</sub>	0.9	1.1	1.75	-	1.75	-	2	-	ns		
Read DQS Preamble Time	t <sub>RPRE</sub>	0.4	0.6	0.9	1.1	0.9	1.1	0.9	1.1	CLK		
Read DQS Postamble Time	t <sub>RPST</sub>	0	-	0.4	0.6	0.4	0.6	0.4	0.6	CLK		

**AC Characteristics (cont.)**

Parameter	Symbol	(PC333)		(PC266A)		(PC266B)		(PC200)		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write DQS Preamble Setup Time	t <sub>WPRES</sub>	0.25	-	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time	t <sub>WPREH</sub>	0.4	0.6	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time	t <sub>WPST</sub>	2	-	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Mode Register Set Delay	t <sub>MRD</sub>	10	-	2	-	2	-	2	-	CLK	
Power Down Exit Time	t <sub>PDEX</sub>	75	-	10	-	10	-	10	-	ns	
Exit Self Refresh to Non-Read Command	t <sub>XSNR</sub>	200	-	75	-	75	-	80	-	ns	
Exit Self Refresh to Read Command	t <sub>XSRD</sub>	200	-	200	-	200	-	200	-	CLK	8
Average Periodic Refresh Interval	t <sub>REFI</sub>	-	7.8	-	7.8	-	7.8	-	7.8	us	

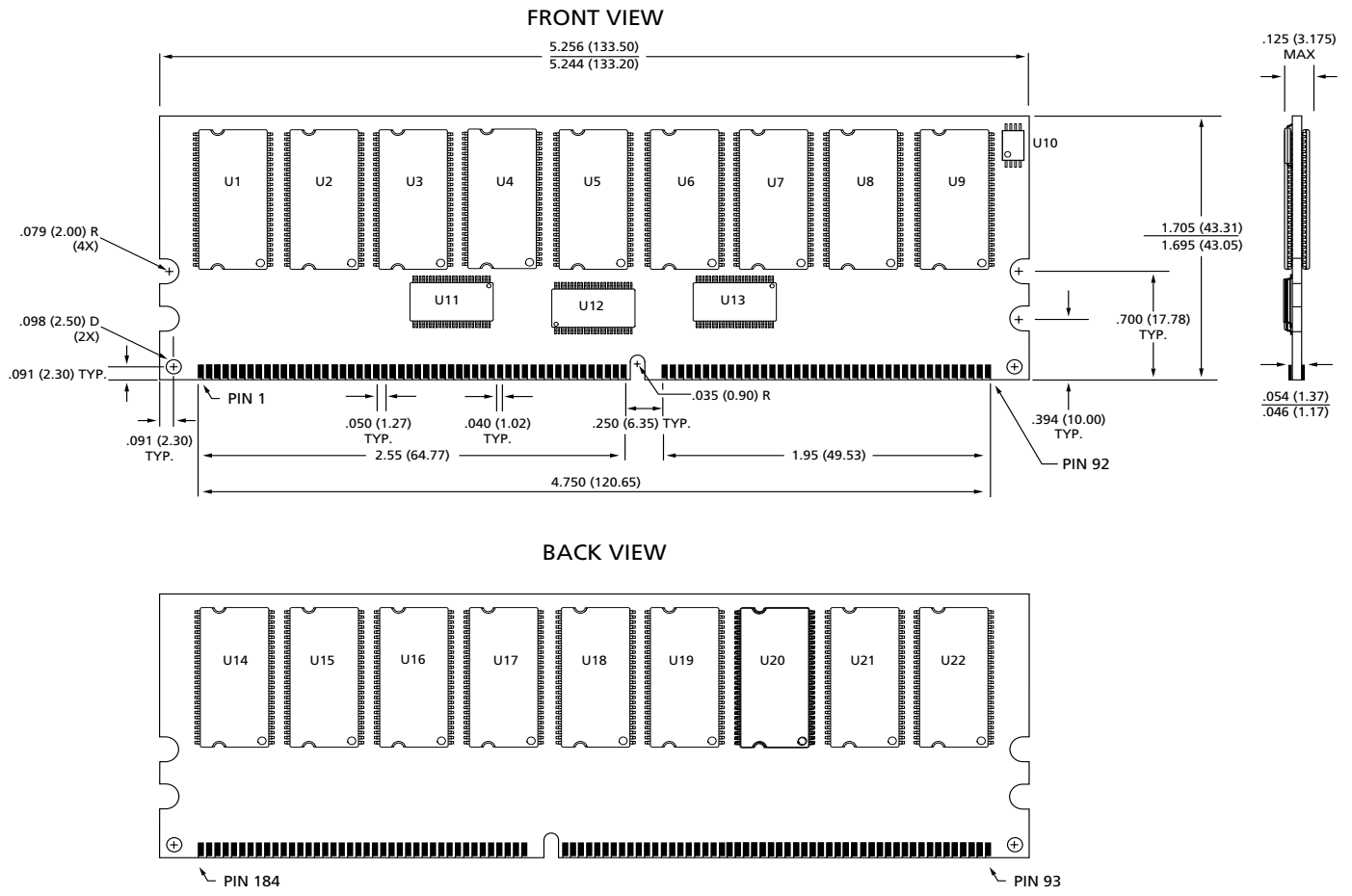
- Notes:**
1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
  2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, CS, RAS, CAS, WE.
  3. For command/address input slew rate >=1.0V/ns
  4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
  5. CK,  $\overline{CK}$  slew rates are >=1.0V/ns
  6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
  7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
  8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Ambient Temperature	T <sub>A</sub>	0 ~ 70	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ 125	°C
Voltage on Any Pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 ~ 3.6	V
Voltage on V <sub>DD</sub> relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.5 ~ 3.6	V
Voltage on V <sub>DDQ</sub> relative to V <sub>SS</sub>	V <sub>DDQ</sub>	-0.5 ~ 3.6	V
Output Short Circuit Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub>	8	W
Soldering Temperature • Time	T <sub>SOLDER</sub>	260 • 10	°C • Sec

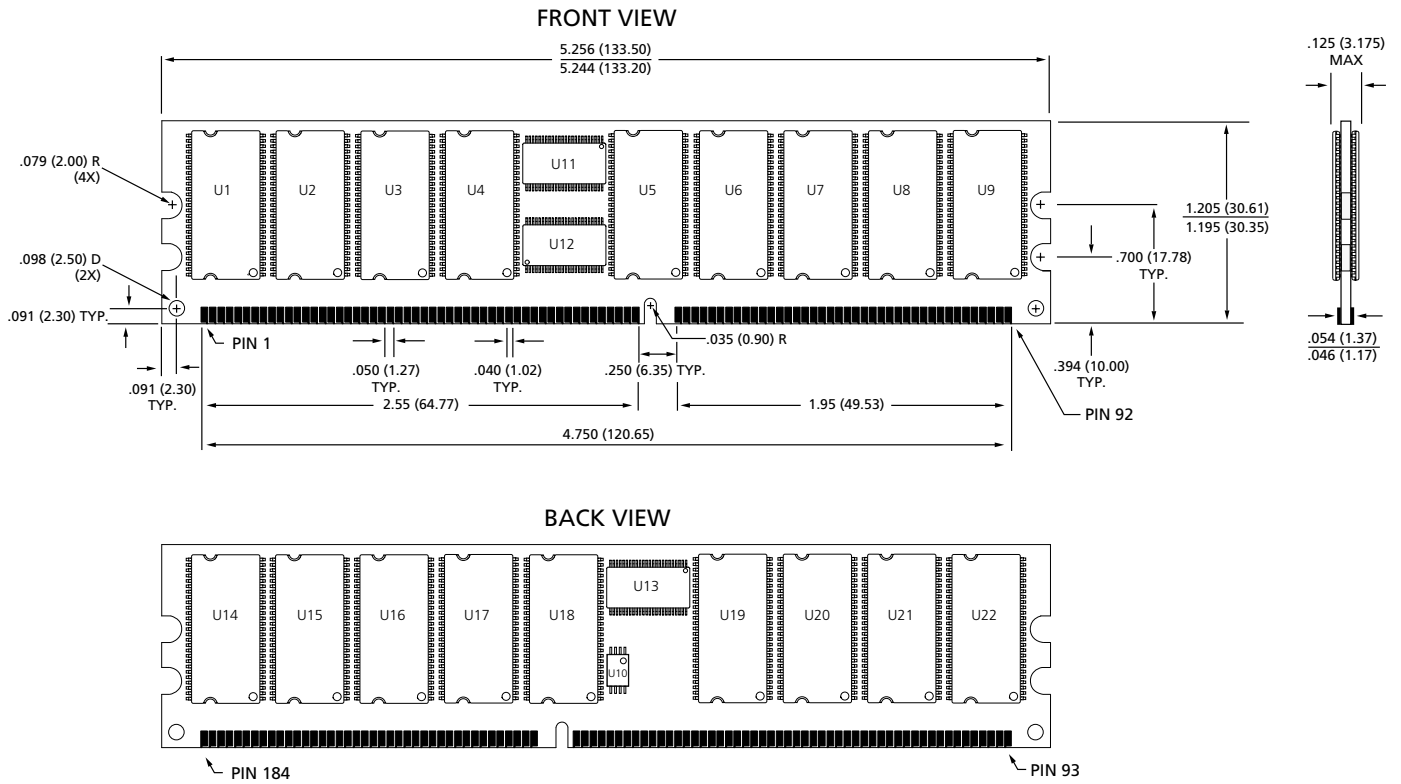
**Note:** Operation at above absolute maximum rating can adversely affect device reliability

**Module Dimensions (Standard)**



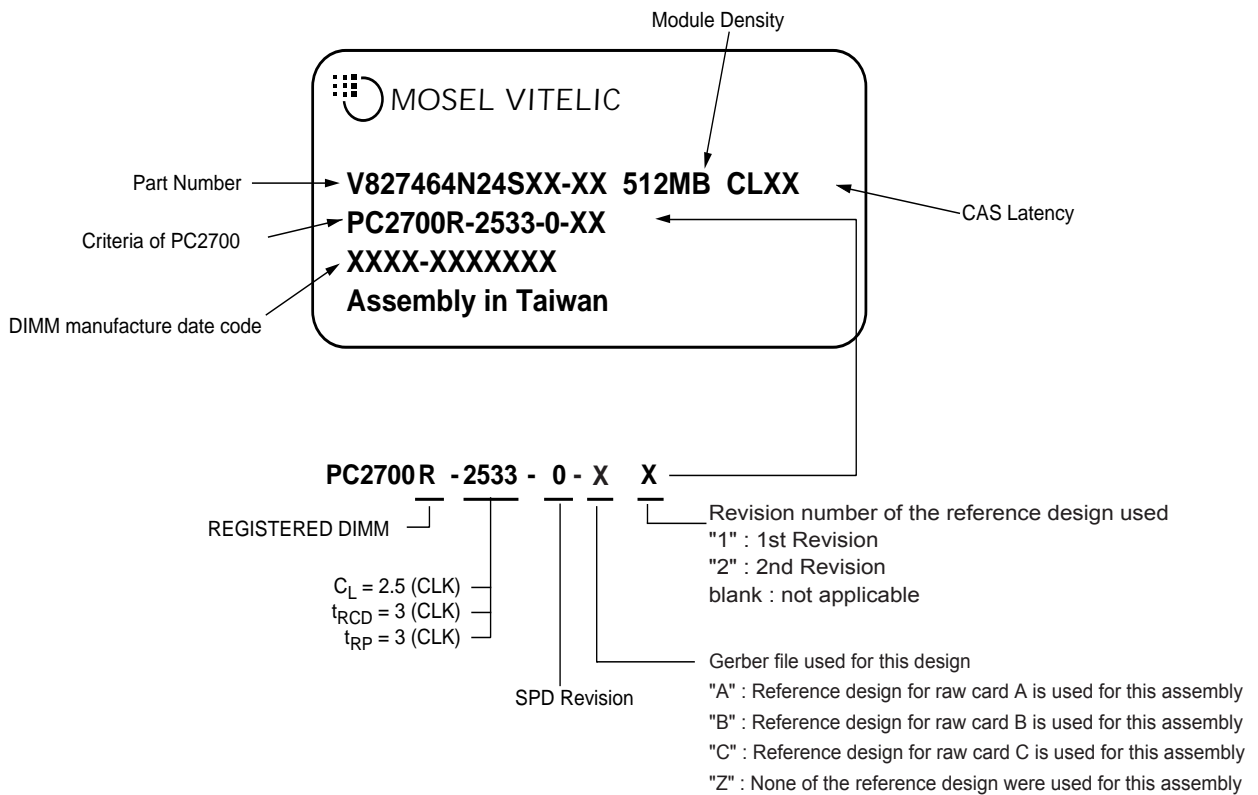
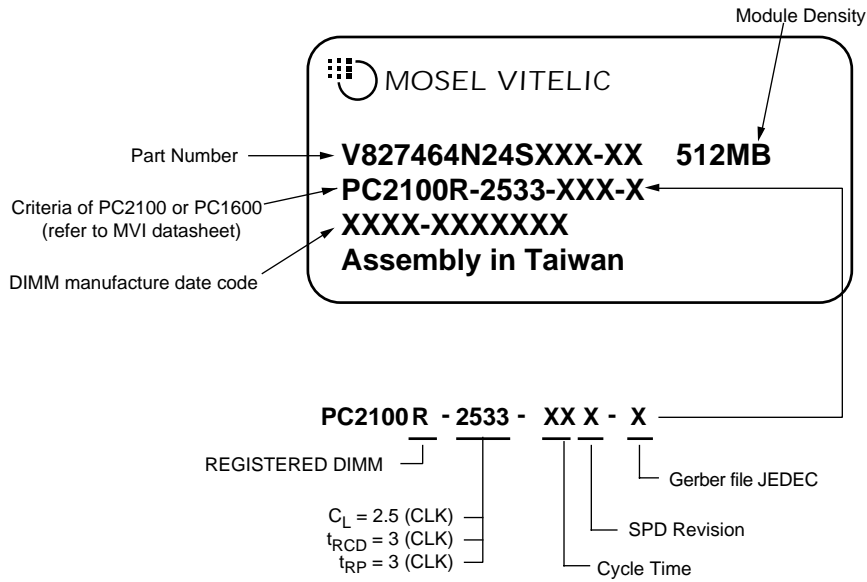
**NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

**Module Dimensions (Low Profile)**



**NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

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