



## Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

### General Description

The MAX4066/MAX4066A quad, SPST, CMOS analog switches are designed to provide superior performance over the industry-standard devices. These new switches feature guaranteed operation from +2.0V to +16V and are fully specified at 3V, 5V, and 12V. Both parts offer 45Ω on-resistance and 2Ω channel-to-channel matching at 12V, plus 4Ω flatness over the specified signal range.

Each device is controlled by TTL/CMOS input levels and can be used as a bilateral switch or multiplexer/demultiplexer.

Low off leakage current (100pA for the MAX4066A) and low power consumption (0.5μW) make the MAX4066/MAX4066A ideal for battery-operated equipment. These parts are also suitable for low-distortion audio applications. Both devices are available in 14-pin DIP and SO packages, as well as a 16-pin QSOP. ESD protection is greater than 2000V per Method 3015.7.

### Applications

Battery-Operated Equipment  
Audio and Video Signal Routing  
Low-Voltage Data-Acquisition Systems  
Sample-and-Hold Circuits  
Communication Circuits

### Features

- ♦ Pin Compatible with 74HC4066
- ♦ Guaranteed On-Resistance:  
170Ω max (3V supply)  
45Ω max (12V supply)
- ♦ Guaranteed Match Between Channels:  
4Ω max (MAX4066)  
2Ω max (MAX4066A)
- ♦ Guaranteed Low Leakage Currents:  
1nA at +25°C (MAX4066)  
100pA at +25°C (MAX4066A)
- ♦ Single-Supply Operation from +2.0V to +16V
- ♦ V+ to GND Signal Handling
- ♦ TTL/CMOS-Logic Compatible
- ♦ Low Power Consumption: 0.5μW
- ♦ Low Crosstalk: -86dB
- ♦ Low Off Isolation: -58dB
- ♦ Low Distortion: 0.03%
- ♦ Wide Bandwidth: > 100MHz

MAX4066/MAX4066A

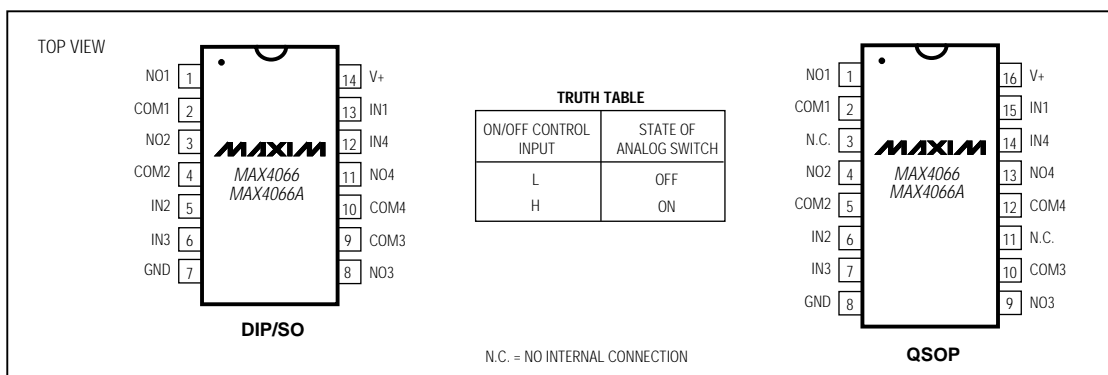
### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4066CPD	0°C to +70°C	14 Plastic DIP
MAX4066CSD	0°C to +70°C	14 Narrow SO
MAX4066CEE	0°C to +70°C	16 QSOP
MAX4066C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

\* Contact factory for dice specifications.

### Pin Configurations/Truth Table



# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

V+	.....-0.3V to +17V	CERDIP (derate 9.09mW/°C above +70°C).....727mW
V <sub>IN</sub> , V <sub>COM</sub> , V <sub>NO</sub> (Note 1)	.....-0.3V to (V + +0.3V)	Operating Temperature Ranges
Current (any terminal)	.....30mA	MAX4066C_/MAX4066AC_.....0°C to +70°C
Peak Current (any terminal)	.....100mA	MAX4066E_/MAX4066AE_.....-40°C to +85°C
ESD per Method 3015.7	.....>2000V	MAX4066MJD/MAX4066AMJD.....-55°C to +125°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Storage Temperature Range.....-65°C to +150°C
Plastic DIP (derate 10.00mW/°C above +70°C)	.....800mW	Lead Temperature (soldering, 10sec).....+300°C
Narrow SO (derate 8.00mW/°C above +70°C)	.....640mW	
QSOB (derate 9.52mW/°C above +70°C)	.....762mW	

**Note 1:** Signals on NO<sub>-</sub>, COM<sub>-</sub>, or IN<sub>-</sub> exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = 12V ±10%, GND = 0V, V<sub>INH</sub> = 4.0V, V<sub>INL</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	V <sub>COM</sub> , V <sub>NO</sub>	(Note 3)		0		V+	V
On-Resistance	R <sub>ON</sub>	V+ = 12V, I <sub>COM</sub> = 2mA, V <sub>NO</sub> = 10V	T <sub>A</sub> = +25°C		16	45	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E		55	
				M		75	
On-Resistance Match Between Channels (Note 4)	ΔR <sub>ON</sub>	V+ = 12V, I <sub>COM</sub> = 2mA, V <sub>NO</sub> = 10V	T <sub>A</sub> = +25°C	MAX4066	0.5	4	Ω
				MAX4066A	0.5	2	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			6	
On-Resistance Flatness (Note 5)	R <sub>FLAT(ON)</sub>	V+ = 12V, I <sub>COM</sub> = 2mA, V <sub>NO</sub> = 10V, 5V, 1V	T <sub>A</sub> = +25°C		2	4	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			6	
NO or NC Off Leakage Current (Note 6)	I <sub>NO(OFF)</sub>	V+ = 12V, V <sub>COM</sub> = 0V, V <sub>NO</sub> = 10V	T <sub>A</sub> = +25°C	MAX4066	-1	1	nA
				MAX4066A	-0.1	0.1	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-6	6	
M	-100	100					
COM Off Leakage Current (Note 6)	I <sub>COM(OFF)</sub>	V+ = 12V, V <sub>COM</sub> = 0V, V <sub>NO</sub> = 10V	T <sub>A</sub> = +25°C	MAX4066	-1	1	nA
				MAX4066A	-0.1	0.1	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-6	6	
M	-100	100					
COM On Leakage Current (Note 6)	I <sub>COM(ON)</sub>	V+ = 12V, V <sub>COM</sub> = 10V, V <sub>NO</sub> = 10V	T <sub>A</sub> = +25°C	MAX4066	-2	2	nA
				MAX4066A	-0.2	0.2	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-12	12	
M	-200	200					

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### ELECTRICAL CHARACTERISTICS—Single +12V Supply (continued)

(V+ = 12V ±10%, GND = 0V, VINH = 4.0V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS	
<b>LOGIC INPUT</b>							
Input Current with Input Voltage High	I <sub>INH</sub>	IN = 5.0V, all others = 0.8V	-0.5	0.005	0.5	μA	
Input Current with Input Voltage Low	I <sub>INL</sub>	IN = 0.8V, all others = 5.0V	-0.5	0.005	0.5	μA	
<b>DYNAMIC</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>COM</sub> = 10V, Figure 2	TA = +25°C	25	100	ns	
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>		150		
Turn-Off Time	t <sub>OFF</sub>	V <sub>COM</sub> = 10V, Figure 2	TA = +25°C	15	75	ns	
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>		100		
On-Channel Bandwidth	BW	Signal = 0dbm, Figure 4, 50Ω in and out	TA = +25°C	100		MHz	
Charge Injection (Note 3)	V <sub>CTE</sub>	CL = 1.0nF, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0Ω, Figure 3	TA = +25°C	1	10	pC	
Off Isolation (Note 7)	V <sub>ISO</sub>	RL = 50Ω, CL = 5pF, f = 1MHz, Figure 4	TA = +25°C	-58		dB	
Crosstalk (Note 8)	V <sub>CT</sub>	RL = 50Ω, CL = 5pF, f = 1MHz, Figure 5	TA = +25°C	-86		dB	
NO Capacitance	C <sub>(OFF)</sub>	f = 1MHz, Figure 6	TA = +25°C	9		pF	
COM Off Capacitance	C <sub>COM(OFF)</sub>	f = 1MHz, Figure 6	TA = +25°C	9		pF	
COM On Capacitance	C <sub>COM(ON)</sub>	f = 1MHz, Figure 6	TA = +25°C	22		pF	
<b>SUPPLY</b>							
Power-Supply Range						V	
Supply Current	I+	V <sub>IN</sub> = 0V or V+, all channels on or off	TA = T <sub>MIN</sub> to T <sub>MAX</sub>	-1	0.001	1	μA
Total Harmonic Distortion	THD		TA = T <sub>MIN</sub> to T <sub>MAX</sub>	0.03			%

MAX4066/MAX4066A

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

MAX4066/MAX4066A

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 5V ±10%, V- = 0V ±10%, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	VCOM, VNO	(Note 3)		0		V+	V
On-Resistance	RON	V+ = 4.5V, ICOM = -1.0mA, VNO = 3.5V	TA = +25°C		45	75	Ω
			TA = TMIN to TMAX	C, E	52	100	
				M		125	
On-Resistance Match Between Channels (Note 4)	ΔRON	V+ = 5V, ICOM = -1.0mA, VNO = 3V	TA = +25°C		0.3	4	Ω
			TA = TMIN to TMAX			12	
On-Resistance Flatness (Notes 3, 5)	RELAT(ON)	V+ = 5V, ICOM = -1.0mA, VNO = 1V, 3V	TA = +25°C		4	6	Ω
			TA = TMIN to TMAX			8	
NO Off Leakage Current (Note 6)	INO(OFF)	V+ = 5.5V, VCOM = 0V, VNO = 4.5V	TA = +25°C	MAX4066	-1	1	nA
				MAX4066A	-0.1	0.1	
			TA = TMIN to TMAX	C, E	-6	6	
				M	-100	100	
COM Off Leakage Current (Note 6)	ICOM(OFF)	V+ = 5.5V, VCOM = 0V, VNO = 4.5V	TA = +25°C	MAX4066	-1	1	nA
				MAX4066A	-0.1	0.1	
			TA = TMIN to TMAX	C, E	-6	6	
				M	-100	100	
COM On Leakage Current (Note 6)	ICOM(ON)	V+ = 5.5V, VCOM = 5V, VNO = 4.5V	TA = +25°C	MAX4066	-2	2	nA
				MAX4066A	-0.2	0.2	
			TA = TMIN to TMAX	C, E	-12	12	
				M	-200	200	
<b>DYNAMIC</b>							
Turn-On Time	tON	VNO = 3V	TA = +25°C		43	125	ns
			TA = TMIN to TMAX			175	
Turn-Off Time	tOFF	VNO = 3V	TA = +25°C		18	75	ns
			TA = TMIN to TMAX			125	
On-Channel Bandwidth	BW	Signal = 0dBm, 50Ω in and out, Figure 4			100		MHz
Charge Injection (Note 3)	Q	VGEN = 0V, RGEN = 0V, CL = 1.0nF, Figure 3		TA = +25°C	2	10	pC
<b>SUPPLY</b>							
Positive Supply Current	I+	V+ = 5.5V, VIN = 0V or V+, all channels on or off			-1	1	μA

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

MAX4066/MAX4066A

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

( $V_+ = 2.7V$  to  $3.3V \pm 10\%$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range	$V_{COM}$ , $V_{NO}$	(Note 3)		0		$V_+$	V
Channel On-Resistance	$R_{ON}$	$V_+ = 3V$ , $I_{COM} = -1.0mA$ , $V_{NO} = 1.5V$	$T_A = +25^\circ C$			170	$\Omega$
			$T_A = T_{MIN}$ to $T_{MAX}$			225	
<b>DYNAMIC</b>							
Turn-On Time (Note 3)	$t_{ON}$	$V_+ = 3V$ , $V_{NO}$ or $V_{NC} = 1.5V$	$T_A = +25^\circ C$	80	185		ns
			$T_A = T_{MIN}$ to $T_{MAX}$				
Turn-Off Time (Note 3)	$t_{OFF}$	$V_+ = 3V$ , $V_{NO}$ or $V_{NC} = 1.5V$	$T_A = +25^\circ C$	28	150		ns
			$T_A = T_{MIN}$ to $T_{MAX}$				
Charge Injection (Note 3)	$Q$	$C_L = 1.0nF$ , $V_{GEN} = 0V$ , $R_{GEN} = 0V$	$T_A = +25^\circ C$	2	10		pC
<b>SUPPLY</b>							
Positive Supply Current	$I_+$	$V_+ = 3.6V$ , $V_{IN} = 0V$ or $V_+$ , all channels on or off		-1	0.001	1	$\mu A$

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:**  $\Delta R_{ON} = R_{ON}(\text{max}) - R_{ON}(\text{min})$ .

**Note 5:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

**Note 6:** Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at  $+25^\circ C$ .

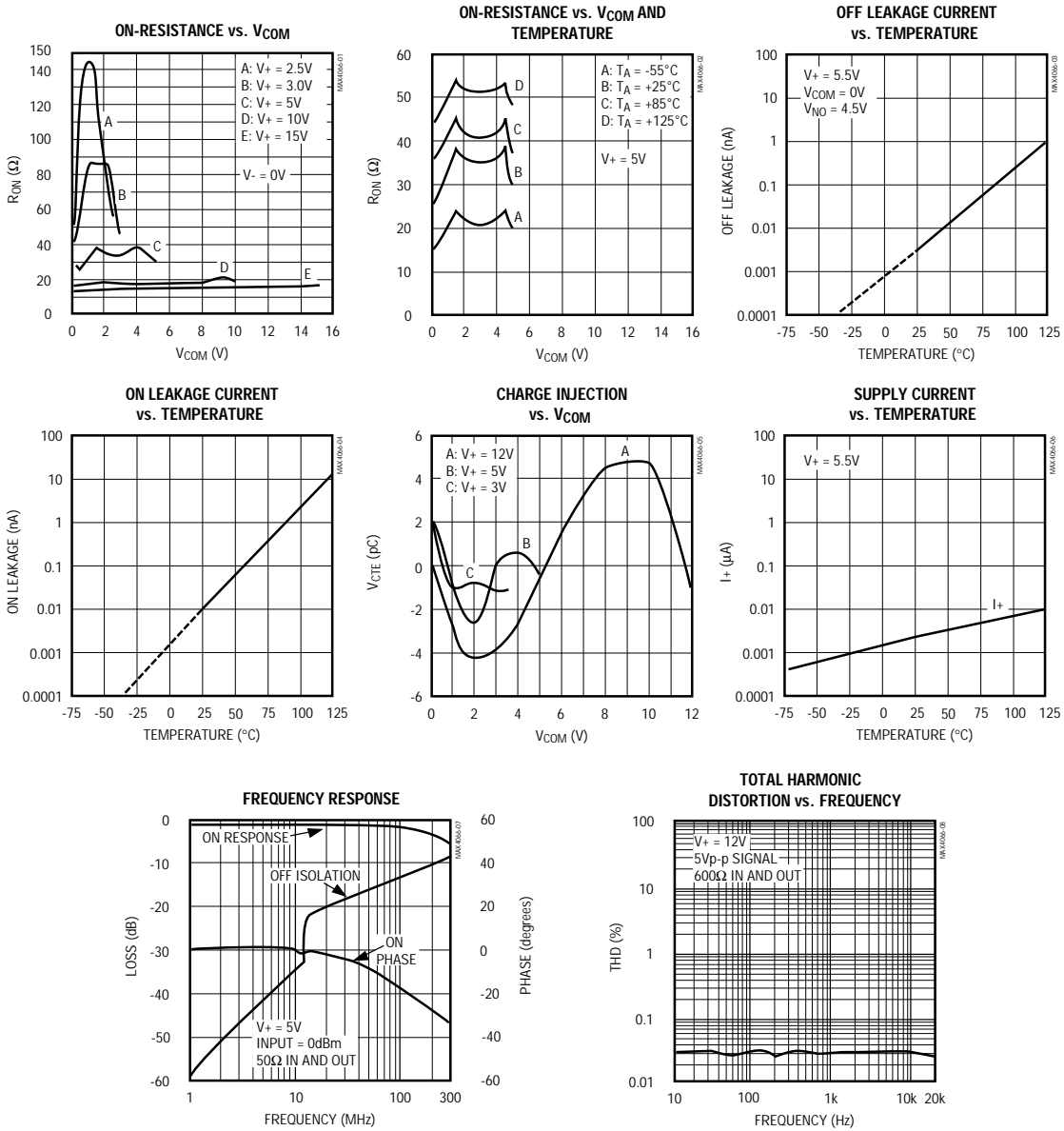
**Note 7:** Off Isolation =  $20\log_{10}(V_{COM} / V_{NO})$ ,  $V_{COM}$  = output,  $V_{NO}$  = input to off switch.

**Note 8:** Between any two switches.

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

## Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted.)



# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

## Pin Description

PIN		NAME	FUNCTION
DIP/SO	QSOP		
1, 3, 8, 11	1, 4, 9, 13	NO1–NO4	Analog Switch Normally Open Terminal (bidirectional)
2, 4, 9, 10	2, 5, 10, 12	COM1–COM4	Analog Switch Common Terminal (bidirectional)
—	3, 11	N.C.	Not internally connected
13, 5, 6, 12	15, 6, 7, 14	IN1–IN4	Logic Control Inputs
7	8	GND	Ground
14	16	V+	Positive Supply Voltage

MAX4066/MAX4066A

## Applications Information

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by the logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above GND, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and GND should not exceed 17V.

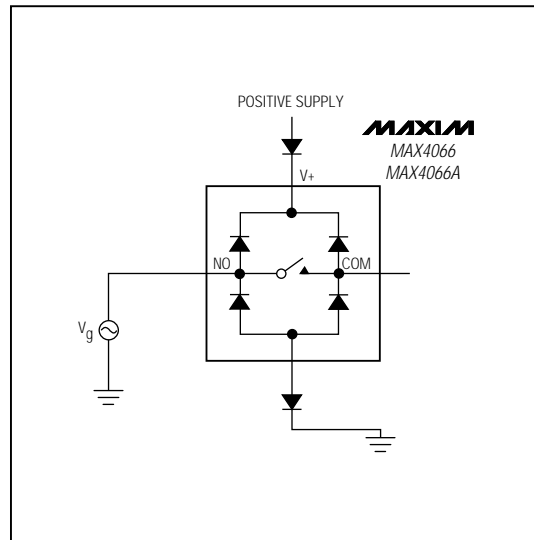


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

## Test Circuits/Timing Diagrams

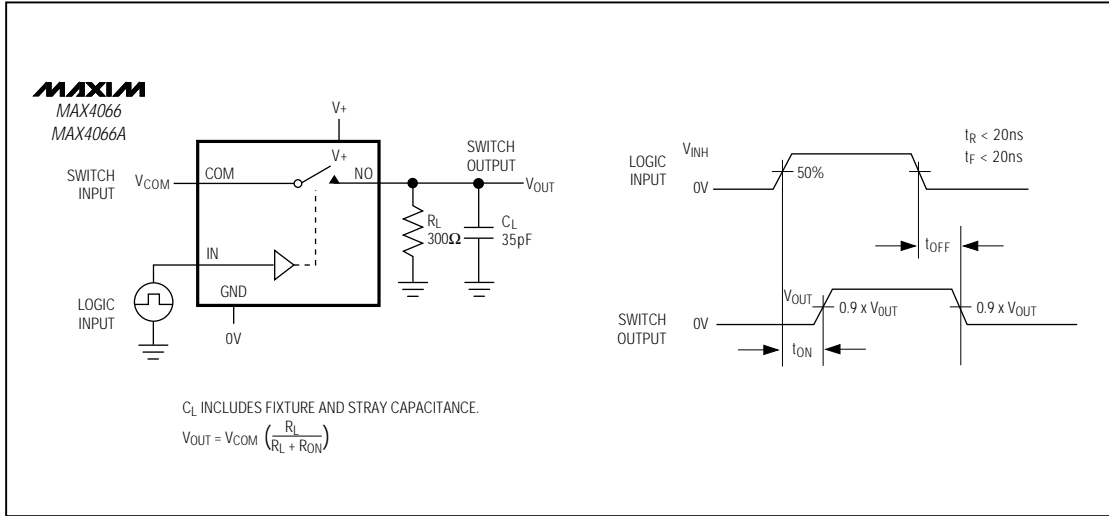


Figure 2. Switching Time

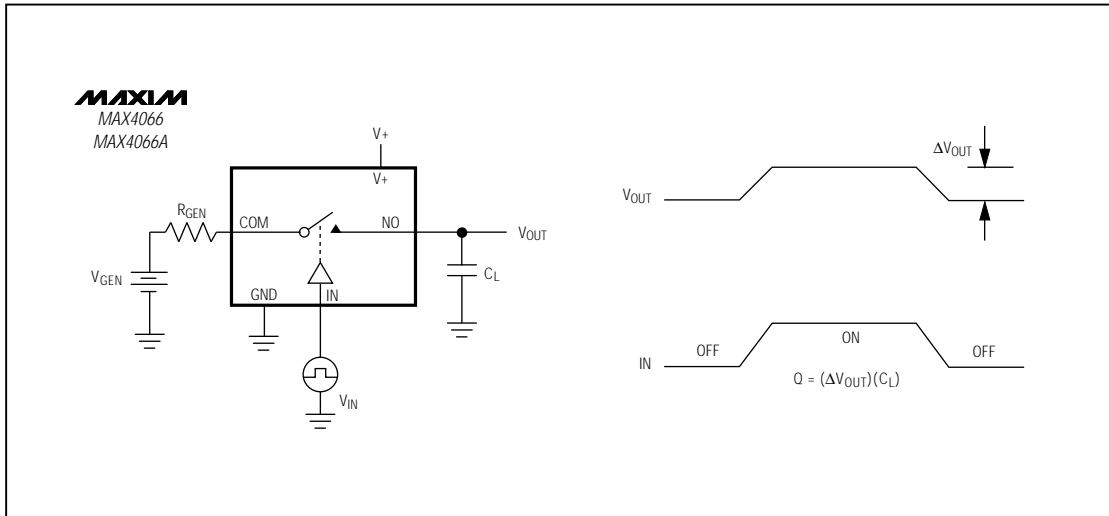


Figure 3. Charge Injection



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Test Circuits (continued)

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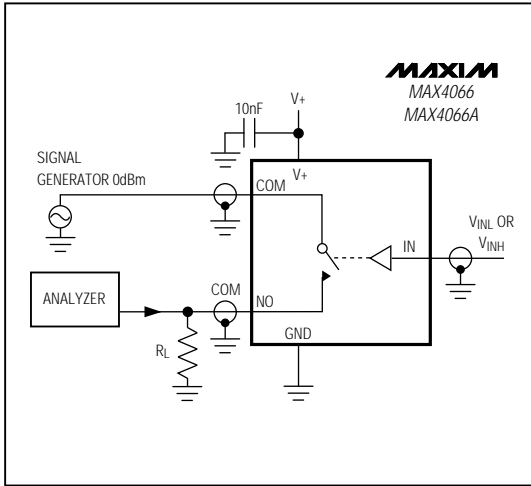


Figure 4. Off Isolation/On-Channel Bandwidth

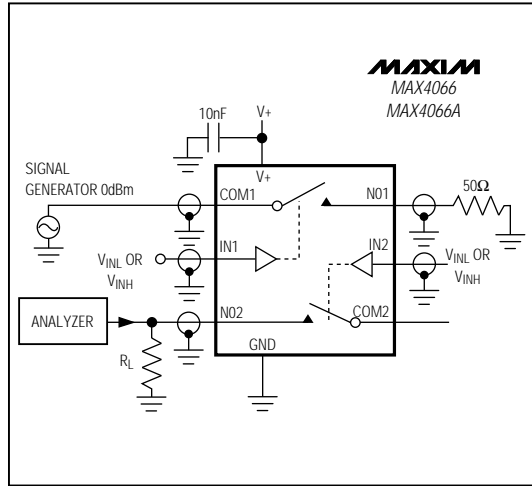


Figure 5. Crosstalk

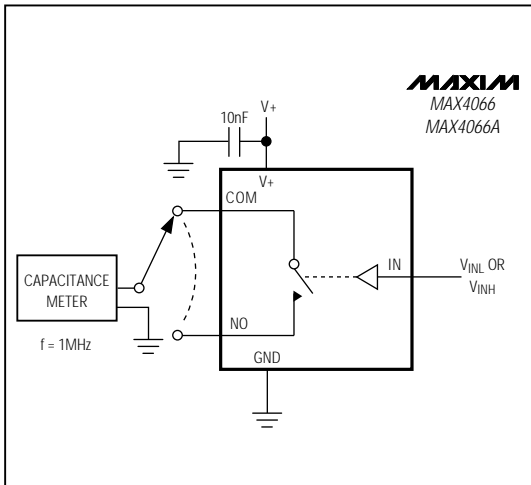


Figure 6. Channel Off/On Capacitance

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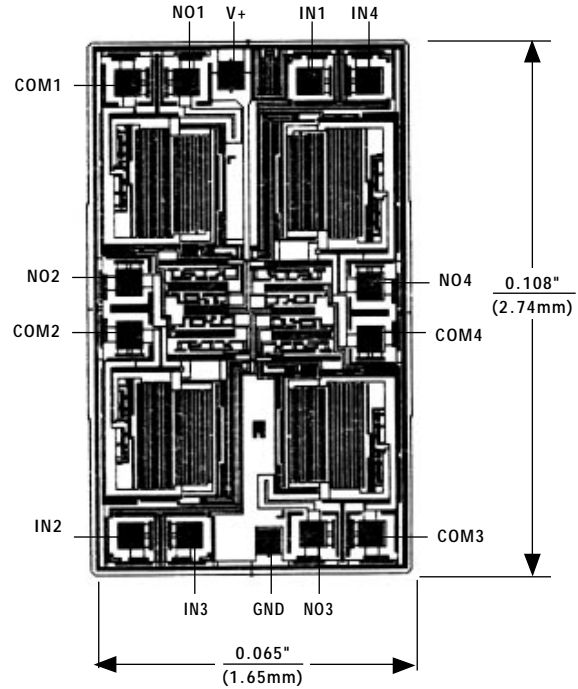
\_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4066EPD	-40°C to +85°C	14 Plastic DIP
MAX4066ESD	-40°C to +85°C	14 Narrow SO
MAX4066MJD	-55°C to +125°C	14 CERDIP**
<b>MAX4066</b> ACPD	0°C to +70°C	14 Plastic DIP
MAX4066ACSD	0°C to +70°C	14 Narrow SO
MAX4066ACEE	0°C to +70°C	16 QSOP
MAX4066AC/D	0°C to +70°C	Dice*
MAX4066AEPD	-40°C to +85°C	14 Plastic DIP
MAX4066AESD	-40°C to +85°C	14 Narrow SO
MAX4066AEEE	-40°C to +85°C	16 QSOP
MAX4066AMJD	-55°C to +125°C	14 CERDIP**

\* Contact factory for dice specifications.

\*\* Contact factory for availability.

Chip Topography

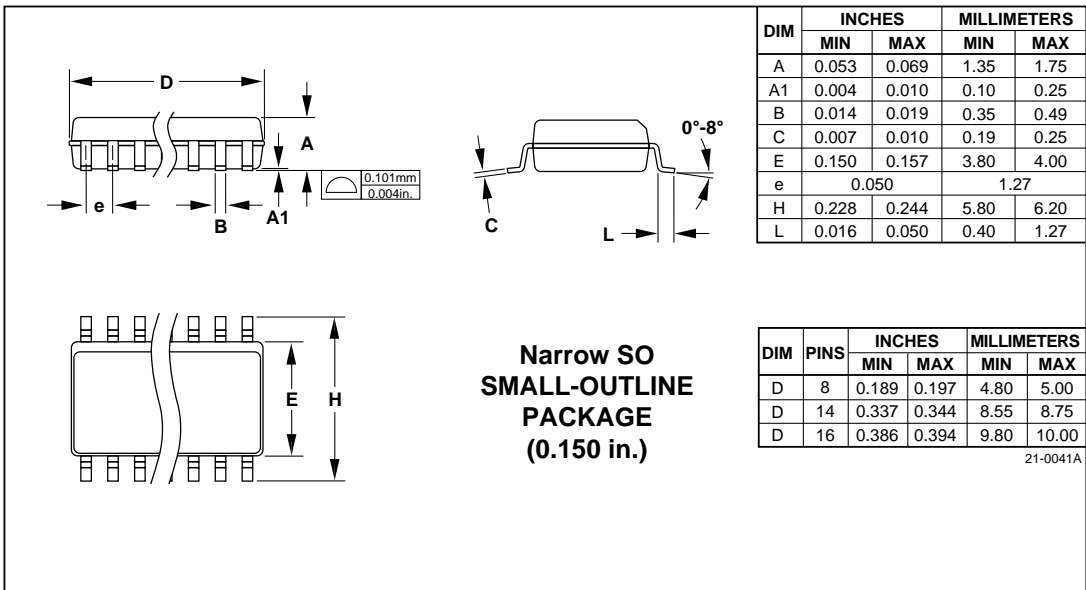
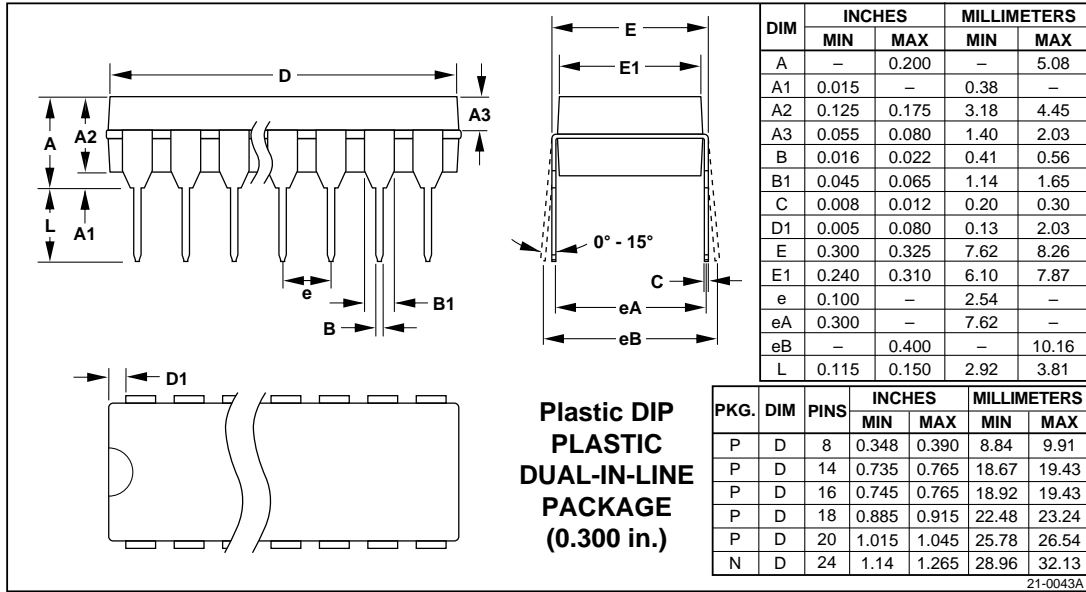


TRANSISTOR COUNT: 69  
 SUBSTRATE CONNECTED TO V+

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

## Package Information

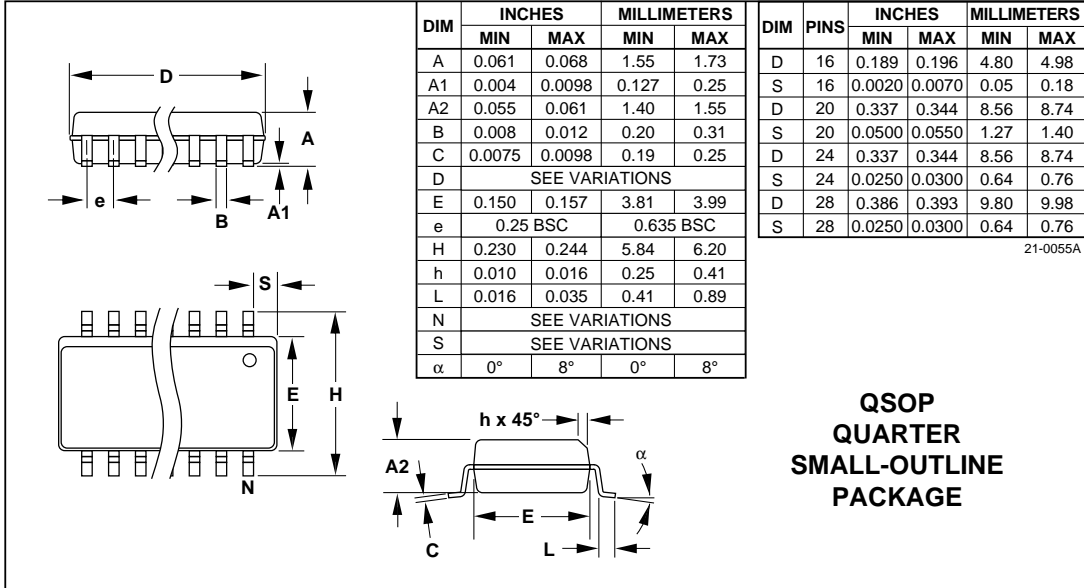
MAX4066/MAX4066A



MAX4066/MAX4066A

# Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switches

Package Information (continued)



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