



QUAD/DUAL P-CHANNEL MATCHED MOSFET ARRAY

GENERAL DESCRIPTION

The ALD1107/ALD1117 are monolithic quad/dual P-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1107/ALD1117 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for precision analog switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC operating environment. The ALD1107/ALD1117 are building blocks for differential amplifier input stages, transmission gates, multiplexer applications, current sources, current mirrors and other precision analog circuits.

FEATURES

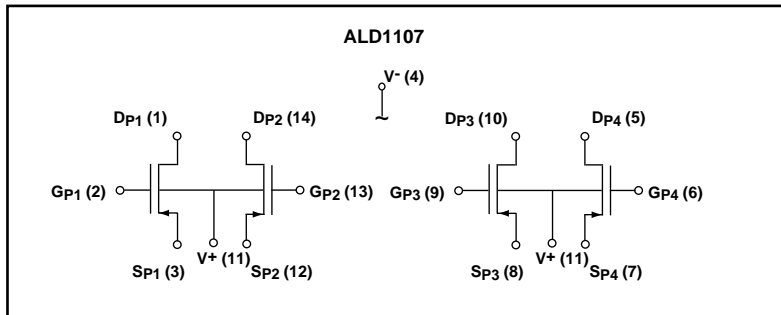
- Low threshold voltage of -0.7
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- 10¹⁴Ω typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10⁹
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin CERDIP Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1117 DA	ALD1117PA	ALD1117 SA
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1107 DB	ALD1107 PB	ALD1107 SB

* Contact factory for industrial temperature range.

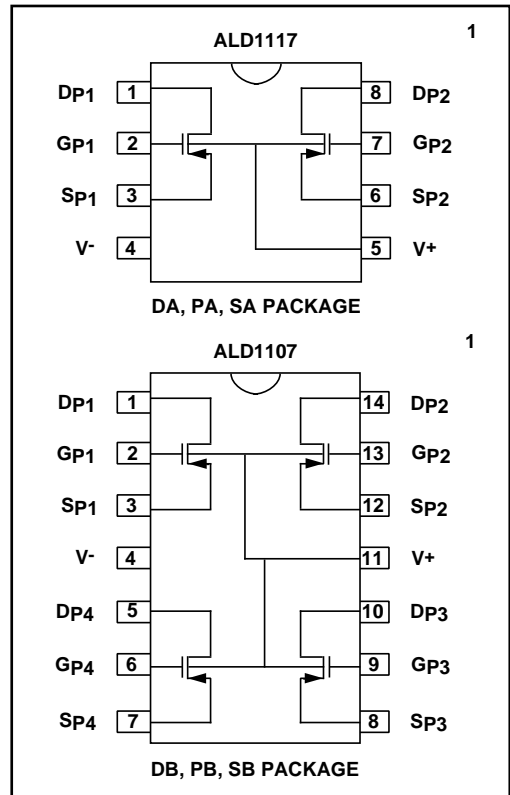
BLOCK DIAGRAM



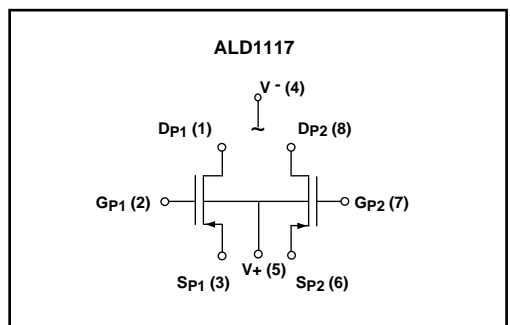
APPLICATIONS

- Precision current sources
- Precision current mirrors
- Voltage Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Precision analog signal processing

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V_{DS}	_____	-13.2V
Gate-source voltage, V_{GS}	_____	-13.2V
Power dissipation	_____	500 mW
Operating temperature range	PA, SA, PB, SB package _____	0°C to +70°C
	DA, DB package _____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

OPERATING ELECTRICAL CHARACTERISTICS

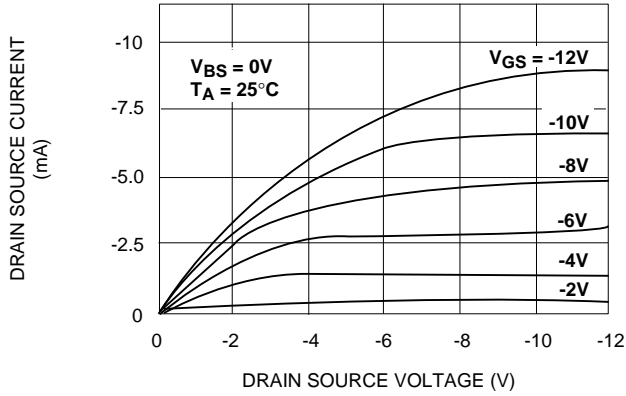
$T_A = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	ALD1107			ALD1117			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	V_T	-0.4	-0.7	-1.0	-0.4	-0.7	-1.0	V	$I_{DS} = -1.0\mu\text{A}$ $V_{GS} = V_{DS}$
Offset Voltage $V_{GS1}-V_{GS2}$	V_{OS}		2	10		2	10	mV	$I_{DS} = -10\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift ²	TC_{VT}		-1.3			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	-1.3	-2		-1.3	-2		mA	$V_{GS} = V_{DS} = -5V$
Transconductance	G_{IS}	0.25	0.67		0.25	0.67		mmho	$V_{DS} = -5V$ $I_{DS} = -10\text{mA}$
Mismatch	ΔG_{IS}		0.5			0.5		%	
Output Conductance	G_{OS}		40			40		μmho	$V_{DS} = -5V$ $I_{DS} = -10\text{mA}$
Drain Source On Resistance	$R_{DS(ON)}$		1200	1800		1200	1800	Ω	$V_{DS} = -0.1V$ $V_{GS} = -5V$
Drain Source On Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5			0.5		%	$V_{DS} = -0.1V$ $V_{GS} = -5V$
Drain Source Breakdown Voltage	BV_{DSS}	-12			-12			V	$I_{DS} = -1.0\mu\text{A}$ $V_{GS} = 0V$
Off Drain Current ¹	$I_{DS(OFF)}$		10	400 4		10	400 4	pA nA	$V_{DS} = -12V$ $V_{GS} = 0V$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	I_{GSS}		0.1	10 1		0.1	10 1	pA nA	$V_{DS} = 0V$ $V_{GS} = -12V$ $T_A = 125^\circ\text{C}$
Input Capacitance ²	C_{ISS}		1	3		1	3	pF	

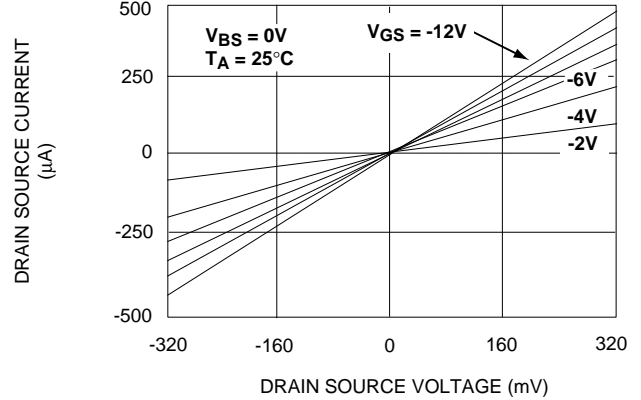
Notes: ¹ Consists of junction leakage currents
² Sample tested parameters

TYPICAL PERFORMANCE CHARACTERISTICS

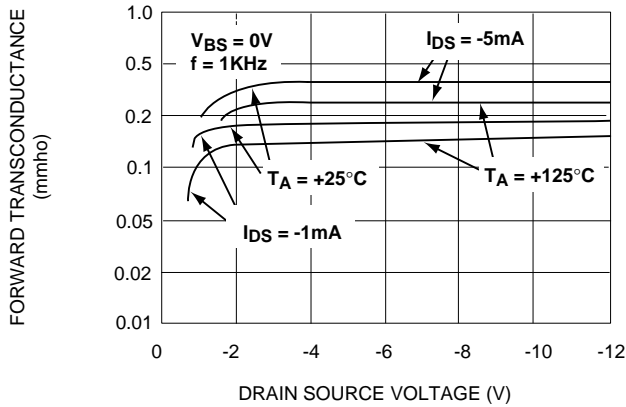
OUTPUT CHARACTERISTICS



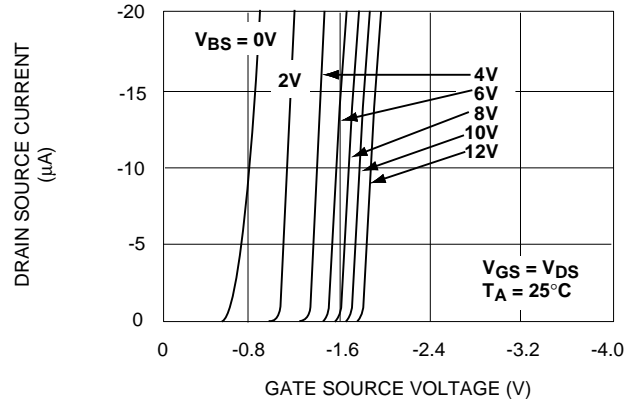
LOW VOLTAGE OUTPUT CHARACTERISTICS



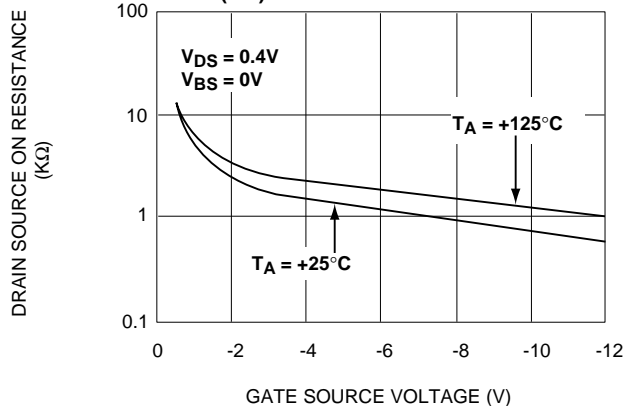
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



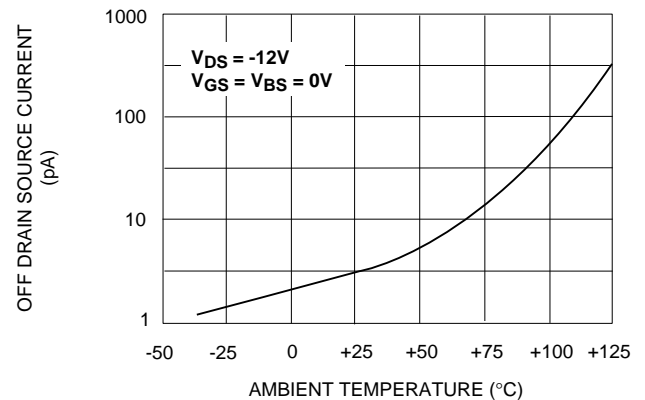
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE $R_{DS(ON)}$ vs. GATE SOURCE VOLTAGE

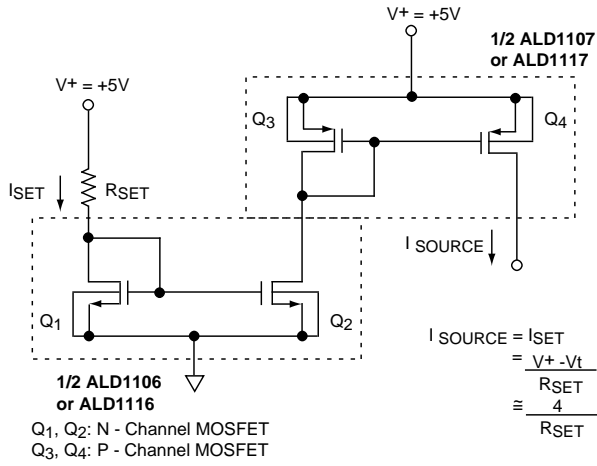


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

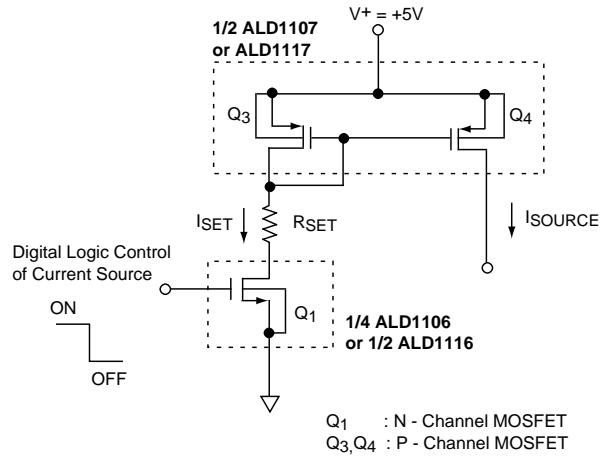


TYPICAL APPLICATIONS

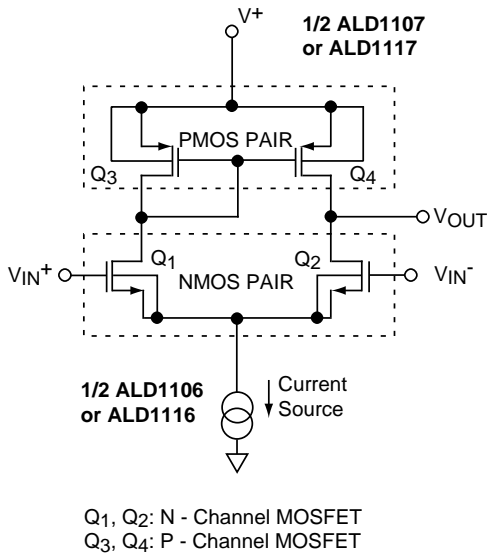
CURRENT SOURCE MIRROR



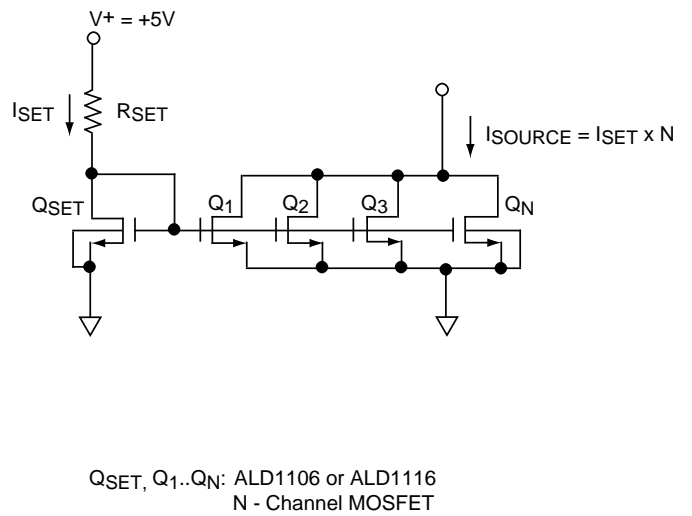
CURRENT SOURCE WITH GATE CONTROL



DIFFERENTIAL AMPLIFIER



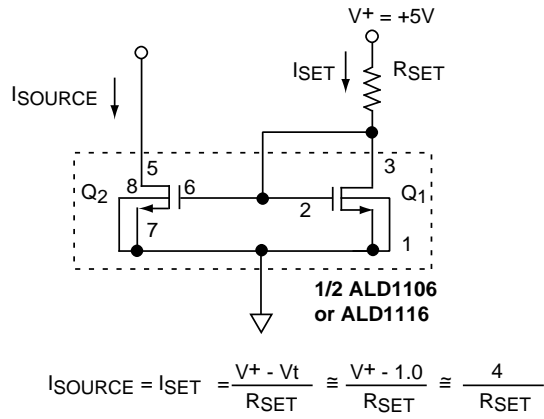
CURRENT SOURCE MULTIPLICATION



TYPICAL APPLICATIONS

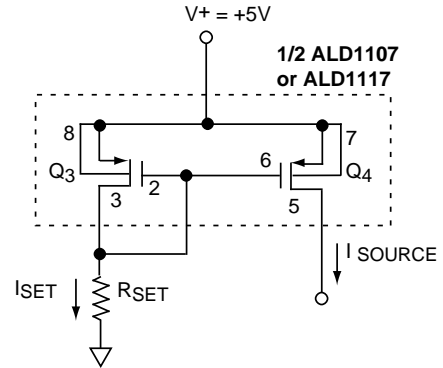
BASIC CURRENT SOURCES

N- CHANNEL CURRENT SOURCE



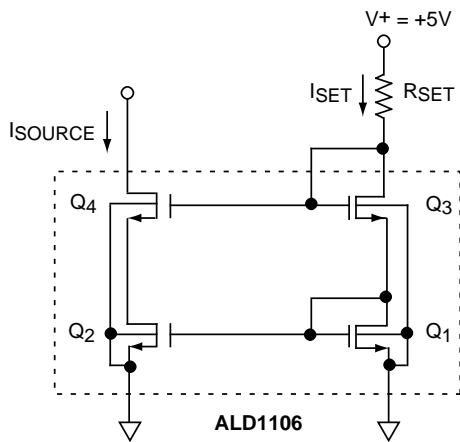
Q1, Q2 : N - Channel MOSFET

P- CHANNEL CURRENT SOURCE

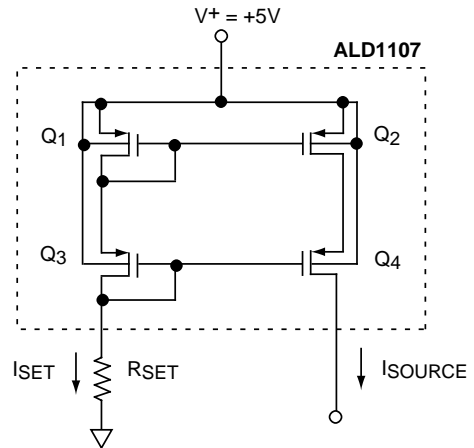


Q3, Q4: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q1, Q2, Q3, Q4: N - Channel MOSFET
(ALD1101 or ALD1103)



$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2V_t}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET
(ALD1102 or ALD1103)

