

4-By-4 Register Files with 3-State Outputs

LS670

FEATURES

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
 - Scratch-Pad Memory
 - Buffer Storage Between Processors
 - Bit Storage in Fast Multiplication Designs
- 3-State Outputs

DESCRIPTION

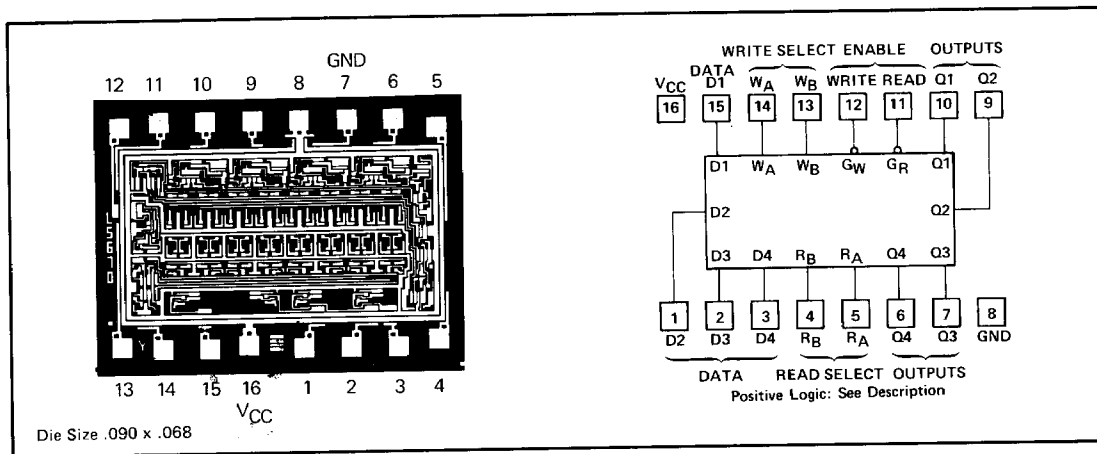
The LS670 and MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in

its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R , is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.



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LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

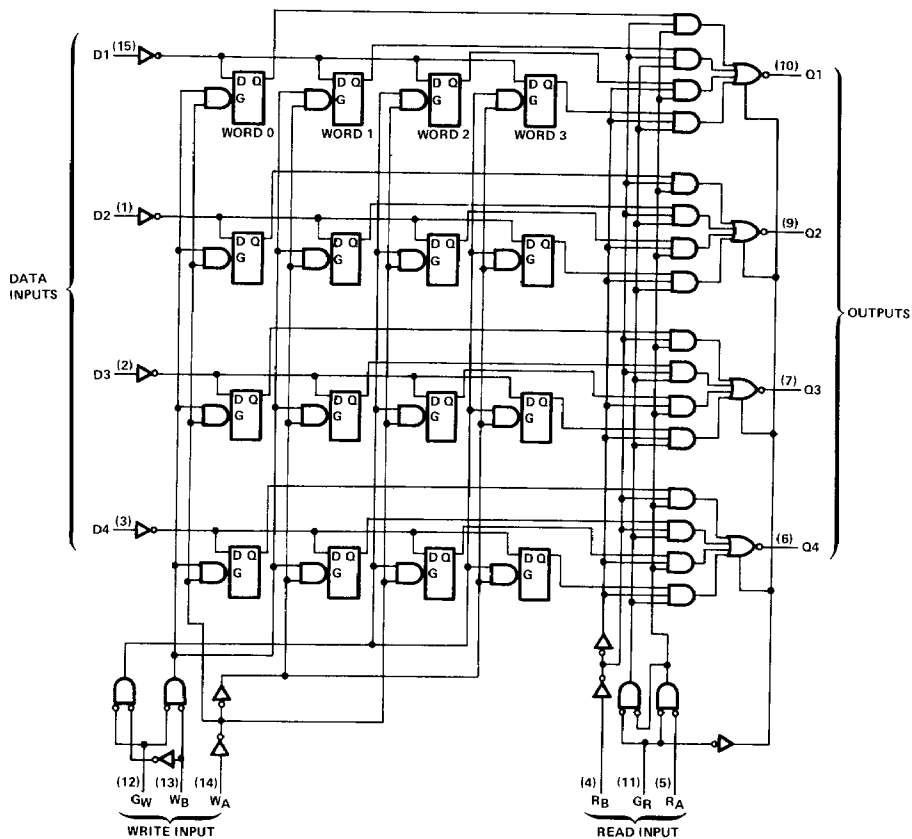
| WRITE INPUTS | | | WORD | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| W _B | W _A | G _W | 0 | 1 | 2 | 3 |
| L | L | L | Q = D | Q ₀ | Q ₀ | Q ₀ |
| L | H | L | Q ₀ | Q = D | Q ₀ | Q ₀ |
| H | L | L | Q ₀ | Q ₀ | Q = D | Q ₀ |
| H | H | L | Q ₀ | Q ₀ | Q ₀ | Q = D |
| X | X | H | Q ₀ | Q ₀ | Q ₀ | Q ₀ |

READ FUNCTION TABLE (SEE NOTES A AND D)

| READ INPUTS | | | OUTPUTS | | | |
|----------------|----------------|----------------|---------|------|------|------|
| R _B | R _A | G _R | Q1 | Q2 | Q3 | Q4 |
| L | L | L | W0B1 | W0B2 | W0B3 | W0B4 |
| L | H | L | W1B1 | W1B2 | W1B3 | W1B4 |
| H | L | L | W2B1 | W2B2 | W2B3 | W2B4 |
| H | H | L | W3B1 | W3B2 | W3B3 | W3B4 |
| X | X | H | Z | Z | Z | Z |

- NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
 C. Q₀ = the level of Q before the indicated input conditions were established.
 D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



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Recommended Operating Conditions

| | | 9LS/54LS | | | 9LS/74LS | | | Unit |
|------------------------------------------------------------------|-----------------------------------------------------------|----------|------|------|----------|------|------|------|
| | | Min. | Nom. | Max. | Min. | Nom. | Max. | |
| Supply voltage, V_{CC} | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | | -1 | | | -2.6 | mA |
| Low-level output current, I_{OL} | | | | 4 | | | 8 | mA |
| Width of write-enable or read-enable pulse, t_W | | 25 | | | 25 | | | ns |
| Setup times, high- or low-level data (see Figure 2) | Data input with respect to write enable, $t_{setup}(D)$ | 10 | | | 10 | | | ns |
| | Write select with respect to write enable, $t_{setup}(W)$ | 15 | | | 15 | | | ns |
| Hold times, high- or low-level data (see Note 2 and Figure 2) | Data input with respect to write enable, $t_{hold}(D)$ | 15 | | | 15 | | | ns |
| | Write select with respect to write enable, $t_{hold}(W)$ | 5 | | | 5 | | | ns |
| Latch time for new data, t_{latch} (see Note 3) | | 25 | | | 25 | | | ns |
| Operating free-air temperature range, T_A | | -55 | | 125 | 0 | | 70 | °C |

- NOTES
1. Voltage values are with respect to network ground terminal.
 2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold}(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
 3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

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Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

| Parameter | Test Conditions† | 9LS/54LS | | | 9LS/74LS | | | Unit |
|----------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------------|------|------|----------|------|------|---------------|
| | | Min. | Typ‡ | Max. | Min. | Typ‡ | Max. | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| V_I Input clamp voltage | $V_{CC} = \text{MIN.}$, $I_I = -18\text{mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN.}$, $V_{IH} = 2\text{V}$, $V_{IL} = V_{IL\text{max}}$ | $I_{OH} = -1\text{mA}$ | 2.4 | 3.4 | | | | V |
| | | $I_{OH} = -2.6\text{mA}$ | | | 2.4 | 3.1 | | |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN.}$, $V_{IH} = 2\text{V}$, $V_{IL} = V_{IL\text{max}}$ | $I_{OL} = 4\text{mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 8\text{mA}$ | | | | 0.35 | 0.5 | |
| I_{OZH} Off-state output current, high-level voltage applied | $V_{CC} = \text{MAX.}$, $V_{IH} = 2\text{V}$, $V_O = 2.7\text{V}$ | | | 20 | | | 20 | μA |
| I_{OZL} Off-state output current, low-level voltage applied | $V_{CC} = \text{MAX.}$, $V_{IH} = 2\text{V}$, $V_O = 0.4\text{V}$ | | | -20 | | | -20 | μA |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX.}$, $V_I = 7\text{V}$ | Any D, R, or W | | | 0.1 | | 0.1 | mA |
| | | GW | | | 0.2 | | 0.2 | |
| | | GR | | | 0.3 | | 0.3 | |
| I_{IH} High-level input current | $V_{CC} = \text{MAX.}$, $V_I = 2.7\text{V}$ | Any D, R, or W | | | 20 | | 20 | μA |
| | | GW | | | 40 | | 40 | |
| | | GR | | | 60 | | 60 | |
| | | Any D, R, or W | | | -0.4 | | -0.4 | |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX.}$ | GW | | | -0.8 | | -0.8 | mA |
| | | GR | | | -1.2 | | -1.2 | |
| I_{OS} Short-circuit output current ‡ | $V_{CC} = \text{MAX.}$ | -30 | | -130 | -30 | | -130 | mA |
| I_{CC} Supply current | $V_{CC} = \text{MAX.}$, See Note 4 | | 30 | 50 | | 30 | 50 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

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Switching Characteristics $V_{CC} = 5.0V$ Over Recommended Free-Air Temperature Range.

| Parameter | From (Input) | To (Output) | -55° C | | | +25° C | | | +125° C | | | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|--------|------|------|--------|------|------|---------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Test Conditions: $C_L = 15pF$, $R_L = 2.0k\Omega$ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. A on page 2-174) | | | | | | | | | | | | |
| t_{PLH} | Read | Any Q | | 26 | 44 | | 23 | 40 | | 26 | 45 | ns |
| t_{PHL} | Select | | | 28 | 49 | | 25 | 45 | | 28 | 50 | |
| t_{PLH} | Write enable | Any Q | | 30 | 49 | | 26 | 45 | | 30 | 50 | ns |
| t_{PHL} | | | | | 31 | 54 | | 28 | 50 | | 31 | |
| t_{PLH} | Data | Any Q | | 28 | 49 | | 25 | 45 | | 28 | 50 | ns |
| t_{PHL} | | | | | 26 | 44 | | 23 | 40 | | 26 | |
| Test Conditions: $C_L = 5pF$, $R_L = 2.0k\Omega$ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. C on page 2-174) | | | | | | | | | | | | |
| t_{ZH} | Read enable | Any Q | | 18 | 39 | | 15 | 35 | | 18 | 40 | ns |
| t_{ZL} | | | | 25 | 44 | | 22 | 40 | | 25 | 45 | |
| t_{HZ} | | | | 33 | 54 | | 30 | 50 | | 33 | 55 | |
| t_{LZ} | | | | 19 | 39 | | 16 | 35 | | 19 | 40 | |
| Test Conditions: $C_L = 50pF$, $R_L = 2.0k\Omega$ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. A on page 2-174) | | | | | | | | | | | | |
| t_{PLH} | Read | Any Q | | 30 | 49 | | 27 | 44 | | 31 | 50 | ns |
| t_{PHL} | Select | | | 32 | 54 | | 29 | 49 | | 33 | 55 | |
| t_{PLH} | Write enable | Any Q | | 34 | 54 | | 30 | 49 | | 35 | 55 | ns |
| t_{PHL} | | | | | 35 | 59 | | 32 | 54 | | 36 | |
| t_{PLH} | Data | Any Q | | 32 | 53 | | 29 | 49 | | 33 | 55 | ns |
| t_{PHL} | | | | | 30 | 49 | | 27 | 44 | | 31 | |

Note: AC specification shown under -55° C and +125° C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

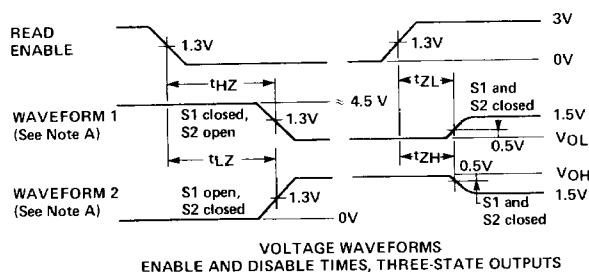
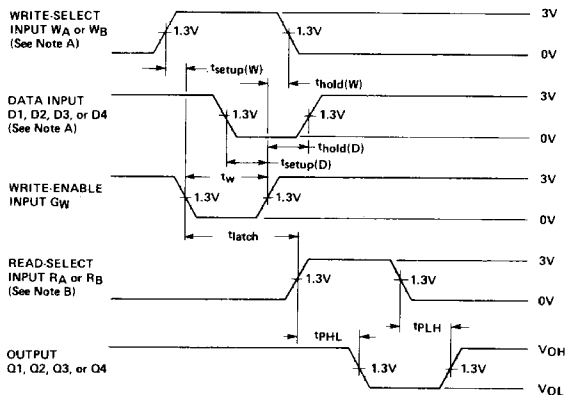


FIGURE 1

- NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
- B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
- C. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

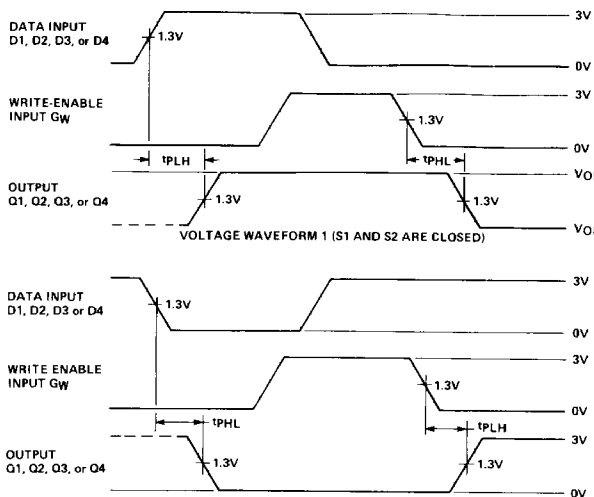
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

FIGURE 2

- NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
 B. When measuring delay times from a read select input, the read-enable input is low.
 C. Input waveforms are supplied by generators having the following characteristics: PRR \leq 2 MHz, $Z_{out} \approx 50 \Omega$, duty cycle \leq 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

FIGURE 3

- NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
 B. Input waveforms are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle \leq 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.