N-Channel Depletion-Mode Vertical DMOS FETs

Ordering Information

BV_{DSX} / BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Order Number / Package			
			TO-92	TO-220	TO-243AA*	Die
350V	25Ω	150mA	DN2535N3	DN2535N5	—	DN2535ND
400V	25Ω	150mA	DN2540N3	DN2540N5	DN2540N8	DN2540ND

* Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

Features

- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Normally-on switches
- ☐ Solid state relays
- ☐ Converters
- ☐ Linear amplifiers
- ☐ Constant current sources
- ☐ Power supply circuits
- ☐ Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

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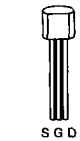
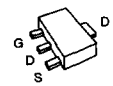
These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

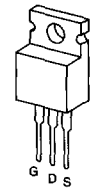
Package Options



TO-92



TO-243AA
(SOT-89)



TO-220
TAB: DRAIN

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	120mA	500mA	1.0W	125	170	120mA	500mA
TO-220	500mA	500mA	15.0W	8.3	70	500mA	500mA
TO-243AA	170mA	500mA	1.6W (T_A = 25°)†	15	78†	170mA	500mA

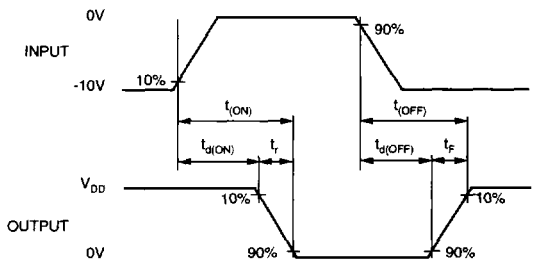
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate. T_A = 25°C

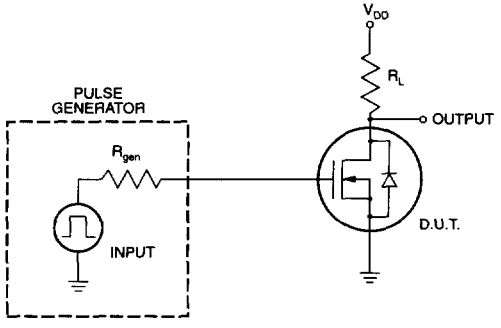
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	DN2540	400			V	V_{GS} = -5V, I_D = 100µA
		DN2535	350				
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage		-1.5		-3.5	V	V_{DS} = 25V, I_D= 10µA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature				4.5	mV/°C	V_{DS} = 25V, I_D= 10µA
I_{GSS}	Gate Body Leakage Current				100	nA	V_{GS} = ± 20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-Source Leakage Current				10	µA	V_{GS} = -10V, V_{DS} = Max Rating
					1	mA	V_{GS} = -10V, V_{DS} = 0.8 Max Rating T_A = 125°C
I_{DSS}	Saturated Drain-to-Source Current		150			mA	V_{GS} = 0V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			17	25	Ω	V_{GS} = 0V, I_D = 120mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.1	%/°C	V_{GS} = 0V, I_D = 120mA
G_{FS}	Forward Transconductance			325		m℧	I_D = 100mA, V_{DS} = 10V
C_{ISS}	Input Capacitance			200	300	pF	V_{GS} = -10V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			12	30		
C_{RSS}	Reverse Transfer Capacitance			1	5		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = -10V, I_{SD} = 120mA
t_{rr}	Reverse Recovery Time			800		ns	V_{GS} = -10V, I_{SD} = 1A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

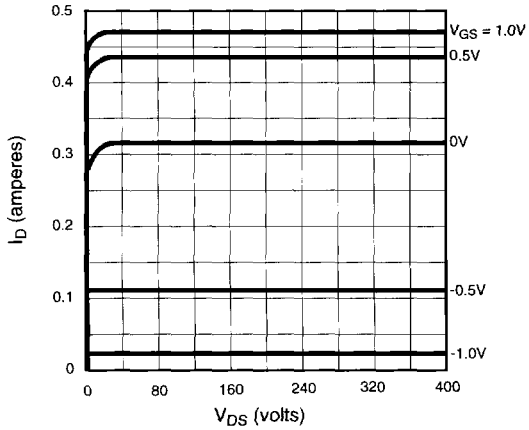
Switching Waveforms and Test Circuit



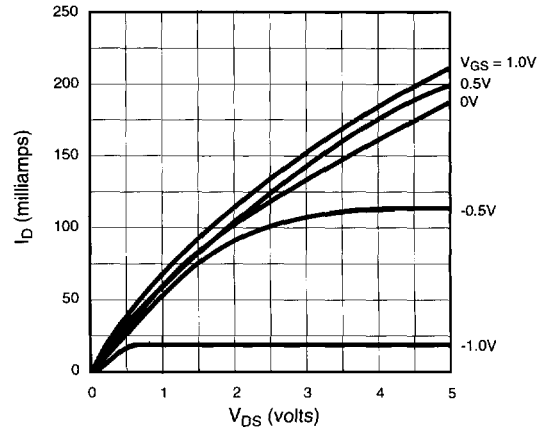


Typical Performance Curves

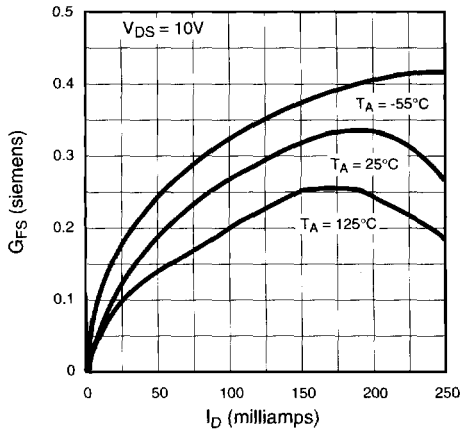
Output Characteristics



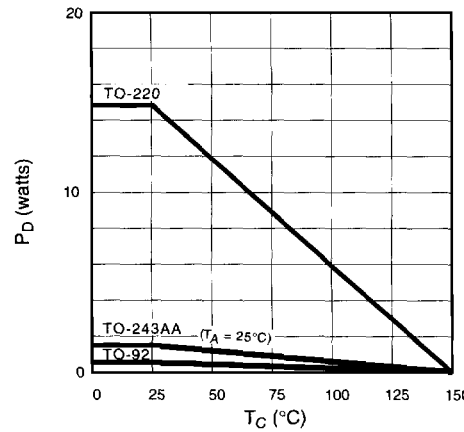
Saturation Characteristics



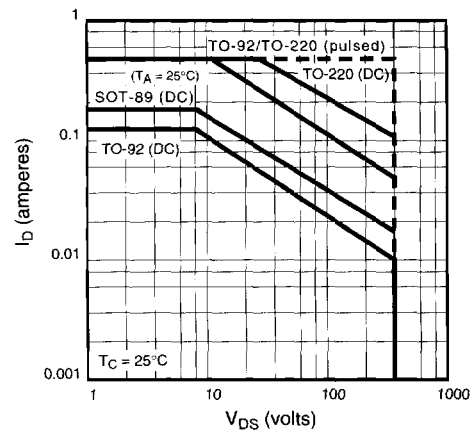
Transconductance vs. Drain Current



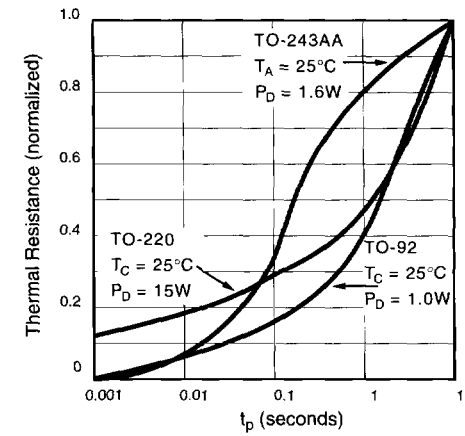
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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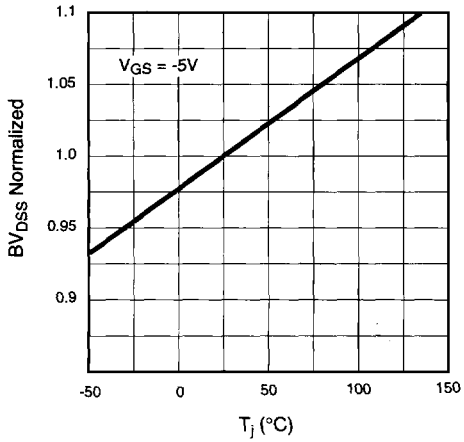
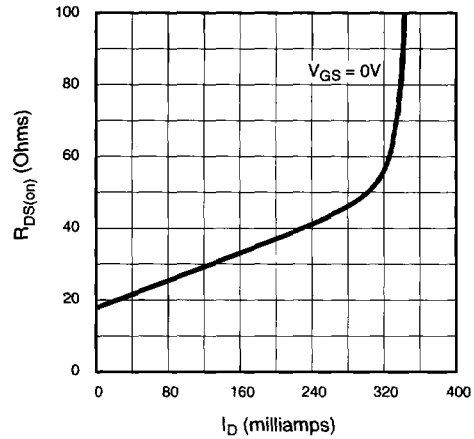
Typical Performance Curves

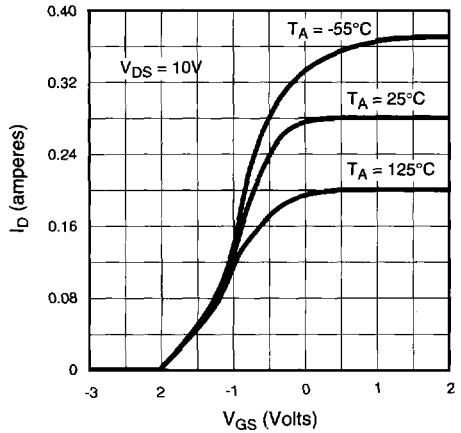
BV$_{DSS}$ Variation with Temperature



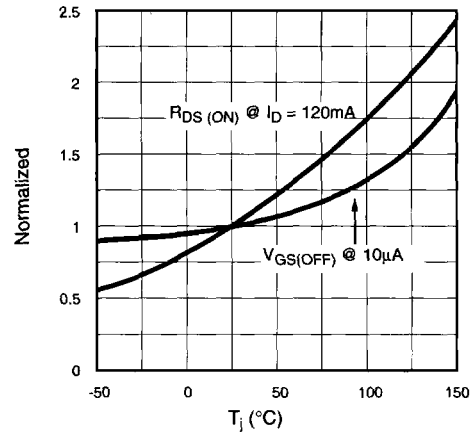
On-Resistance vs. Drain Current



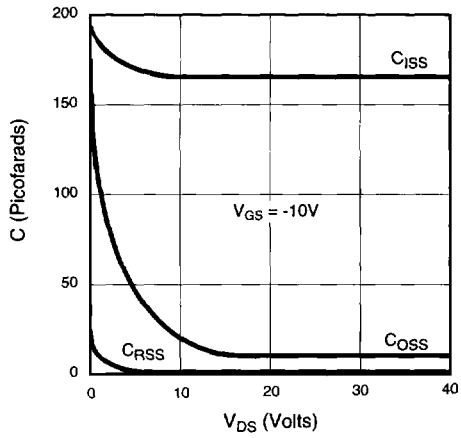
Transfer Characteristics



VGS(off) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics