

FEATURES

- ❑ High-Speed (15ns), Low Power 16-bit Cascadable ALU
- ❑ Extended Function Set (32 Advanced ALU Functions)
- ❑ All Registers Have a Bypass Path for Complete Flexibility
- ❑ Replaces IDT7383
- ❑ 68-pin PLCC, J-Lead

DESCRIPTION

The **L4C383** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit. The L4C383 is capable of performing up to 32 different arithmetic or logic functions.

The L4C383 can be cascaded to perform 32-bit or greater operations. See "Cascading the L4C383" on the next page.

ARCHITECTURE

The L4C383 operates on two 16-bit operands (A and B) and produces a 16-

bit result (F). Five select lines control the ALU and provide 19 arithmetic and 13 logical functions. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one or both of the ALU inputs, accommodating chain operations and accumulation.

ALU OPERATIONS

The S4-S0 lines specify the operation to be performed. The ALU functions and their select codes are shown in Table 1.

ALU STATUS

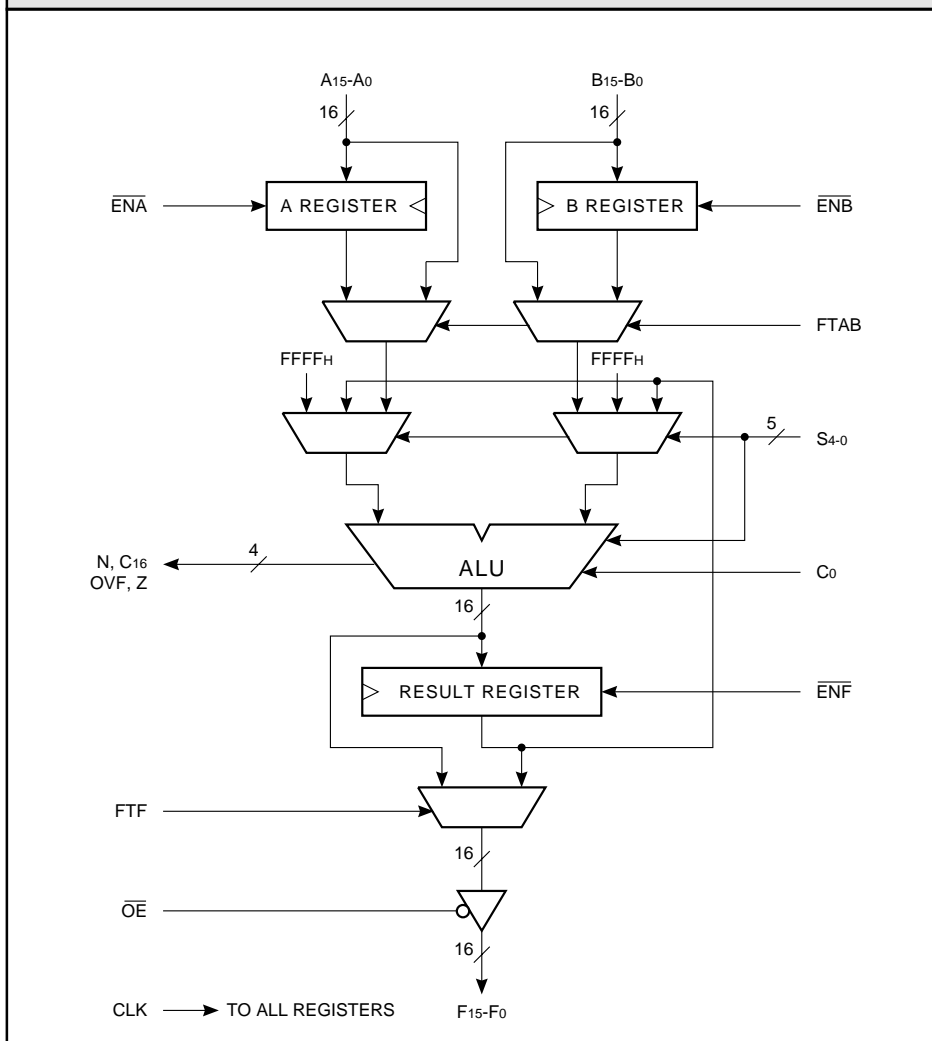
The ALU provides Overflow and Zero status bits. A Carry output is also provided for cascading multiple devices, however it is only defined for the 19 arithmetic functions. The ALU sets the Zero output when all 16 output bits are zero. The N, C16 and OVF flags for the arithmetic operations are defined in Table 2.

OPERAND REGISTERS

The L4C383 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. The A register is enabled for input by setting the $\overline{\text{ENA}}$ control LOW, and the B register is enabled for input by setting the $\overline{\text{ENB}}$ control LOW. When either the $\overline{\text{ENA}}$ control or $\overline{\text{ENB}}$ control is HIGH, the data in the corresponding input register will not change.

This architecture allows the L4C383 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line.

L4C383 BLOCK DIAGRAM



16-bit Cascadable ALU (Extended Set)

TABLE 1. ALU FUNCTIONS	
S4-S0	FUNCTION
00000	A + B + C ₀
00001	A OR B
00010	A + \bar{B} + C ₀
00011	\bar{A} + B + C ₀
00100	A + C ₀
00101	\bar{A} OR F
00110	A - 1 + C ₀
00111	\bar{A} + C ₀
01000	A + F + C ₀
01001	A OR F
01010	A + \bar{F} + C ₀
01011	\bar{A} + F + C ₀
01100	F + B + C ₀
01101	\bar{A} OR B
01110	F + \bar{B} + C ₀
01111	\bar{F} + B + C ₀
10000	A XOR B
10001	A AND B
10010	\bar{A} AND B
10011	A XNOR B
10100	A XOR F
10101	A AND F
10110	\bar{A} AND F
10111	ALL 1's + C ₀
11000	B + C ₀
11001	A AND \bar{B}
11010	\bar{B} + C ₀
11011	B - 1 + C ₀
11100	F + C ₀
11101	A OR \bar{B}
11110	F - 1 + C ₀
11111	\bar{F} + C ₀

When the FTAB control is asserted (FTAB = HIGH), data is routed around the A and B input registers; however, they continue to function normally via the ENA and ENB controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

TABLE 2. ALU STATUS FLAGS	
Bit Carry Generate	= $g_i = A_i B_i$ for $i = 0 \dots 15$
Bit Carry Propagate	= $p_i = A_i + B_i$ for $i = 0 \dots 15$
P ₀	= p_0
P _i	= $p_i (P_{i-1})$ for $i = 1 \dots 15$
and	
G ₀	= g_0
G _i	= $g_i + p_i (G_{i-1})$ for $i = 1 \dots 15$
C _i	= $G_{i-1} + P_{i-1} (C_0)$ for $i = 1 \dots 15$
then	
C ₁₆	= $G_{15} + P_{15} C_0$
OVF	= $C_{15} \text{ XOR } C_{16}$
Zero	= All Output Bits Equal Zero
N	= Sign Bit of ALU Operation

OUTPUT REGISTER

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. When the \overline{ENF} control is LOW, data from the ALU will be clocked into the output register. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the \overline{OE} input allow the L4C383 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal (FTF = HIGH). When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the \overline{ENF} control. The contents of the output register will again be available on the output pins if FTF is released.

CASCADING THE L4C383

Cascading the L4C383 to 32 bits is accomplished simply by connecting the C₁₆ output of the least significant slice to the C₀ input of the most significant slice. The S₄-S₀, \overline{ENA} , \overline{ENB} , and \overline{ENF} lines are

common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C₁₆ outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C₁₆ output of the lower slice. Add this number to the delay from the C₀ input of the upper slice to the output of interest (of the C₀ setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C₁₆ output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 4A through 4D.

Cascading to greater than 32 bits can be accomplished by simply connecting the C₁₆ output of each slice to the C₀ input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C₀ to C₁₆ delays for all intermediate slices must be added to the overall delay for each path.

16-bit Cascadable ALU (Extended Set)

FIGURE 4A. FTAB = 0, FTF = 0

From	To	Calculated Specification Limit
Clock	→ F	= Same as 16-bit case
Clock	→ Other	= (Clock → C16) + (C0 → Out)
C0	→ Other	= (C0 → C16) + (C0 → Out)
S4-S0	→ Other	= (S4-S0 → C16) + (C0 → Out)
A, B	Setup time	= Same as 16-bit case
C0	Setup time	= (C0 → C16) + (C0 Setup time)
S4-S0	Setup time	= (S4-S0 → C16) + (C0 Setup time)
ENA, ENB, ENF	Setup time	= Same as 16-bit case
Minimum cycle time		= (Clock → C16) + (C0 Setup time)

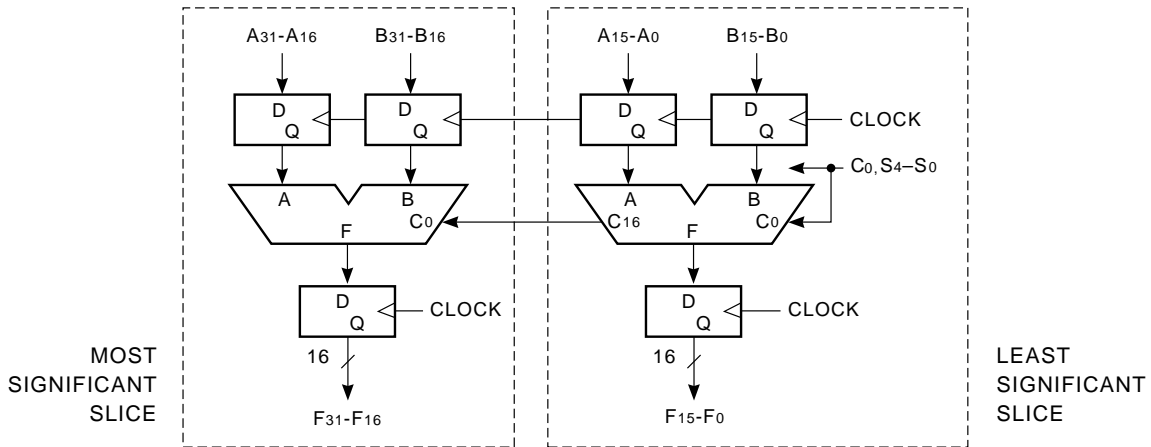
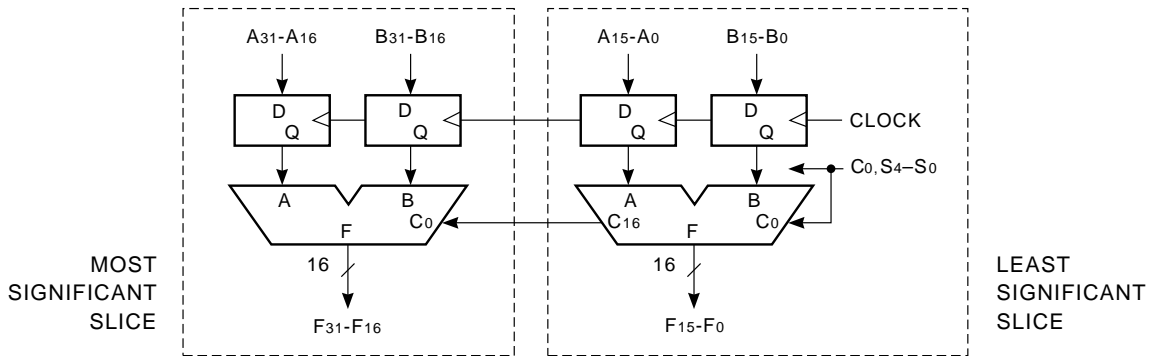


FIGURE 4B. FTAB = 0, FTF = 1

From	To	Calculated Specification Limit
Clock	→ F	= (Clock → C16) + (C0 → F)
Clock	→ Other	= (Clock → C16) + (C0 → Out)
C0	→ F	= (C0 → C16) + (C0 → F)
C0	→ Other	= (C0 → C16) + (C0 → Out)
S4-S0	→ F	= (S4-S0 → C16) + (C0 → F)
S4-S0	→ Other	= (S4-S0 → C16) + (C0 → Out)
A, B	Setup time	= Same as 16-bit case
C0	Setup time	= (C0 → C16) + (C0 Setup time)
S4-S0	Setup time	= (S4-S0 → C16) + (C0 Setup time)
ENA, ENB, ENF	Setup time	= Same as 16-bit case
Minimum cycle time		= (Clock → C16) + (C0 Setup time)



16-bit Cascadable ALU (Extended Set)

FIGURE 4C. FTAB = 1, FTF = 0

From	To	Calculated Specification Limit
Clock	→ F	= Same as 16-bit case
A, B	→ Other	= (A, B → C16) + (C0 → Out)
C0	→ Other	= (C0 → C16) + (C0 → Out)
S4-S0	→ Other	= (S4-S0 → C16) + (C0 → Out)
A, B	Setup time	= (A, B → C16) + (C0 Setup time)
C0	Setup time	= (C0 → C16) + (C0 Setup time)
S4-S0	Setup time	= (S4-S0 → C16) + (C0 Setup time)
\overline{ENA} , \overline{ENB} , \overline{ENF}	Setup time	= Same as 16-bit case
Minimum cycle time (F register accumulate loop)		= (Clock → C16) + (C0 Setup time)

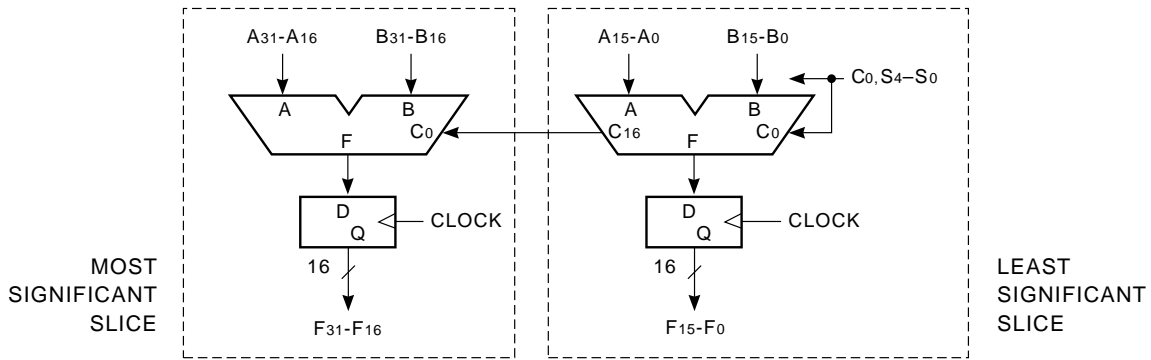
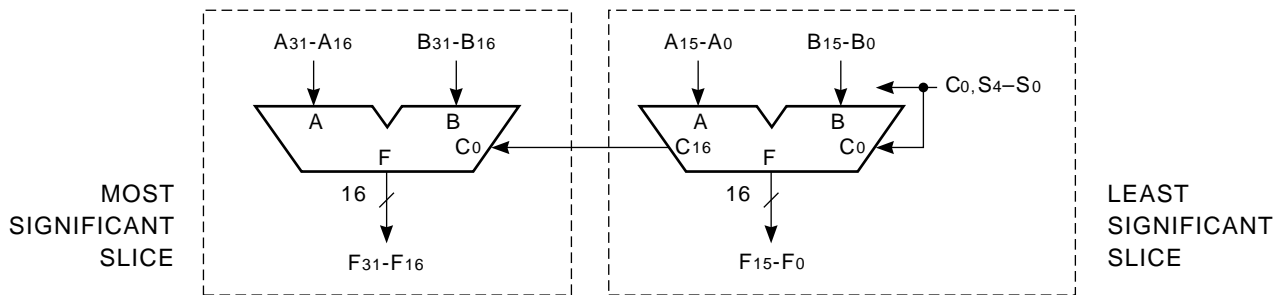


FIGURE 4D. FTAB = 1, FTF = 1

From	To	Calculated Specification Limit
A, B	→ F	= (A, B → C16) + (C0 → F)
A, B	→ Other	= (A, B → C16) + (C0 → Out)
C0	→ F	= (C0 → C16) + (C0 → F)
C0	→ Other	= (C0 → C16) + (C0 → Out)
S4-S0	→ F	= (S4-S0 → C16) + (C0 → F)
S4-S0	→ Other	= (S4-S0 → C16) + (C0 → Out)
A, B	Setup time	= (A, B → C16) + (C0 Setup time)
C0	Setup time	= (C0 → C16) + (C0 Setup time)
S4-S0	Setup time	= (S4-S0 → C16) + (C0 Setup time)
\overline{ENA} , \overline{ENB} , \overline{ENF}	Setup time	= Same as 16-bit case
Minimum cycle time (F register accumulate loop)		= (Clock → C16) + (C0 Setup time)



16-bit Cascadable ALU (Extended Set)

MAXIMUM RATINGS <i>Above which useful life may be impaired (Notes 1, 2, 3, 8)</i>	
Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
V _{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS <i>To meet specified electrical and switching characteristics</i>		
Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS <i>Over Operating Conditions (Note 4)</i>						
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4			V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{Ix}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ V _{CC} (Note 12)			±20	μA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)			1.5	mA

16-bit Cascadable ALU (Extended Set)
SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS Notes 9, 10 (ns)													
To Output From Input		L4C383-55*				L4C383-40*				L4C383-26			
		F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16
FTAB = 0, FTF = 0													
Clock		32	38	53	36	26	30	44	32	22	22	26	22
C0		—	—	34	22	—	—	28	20	—	—	18	18
S4-S0		—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1													
Clock		56	38	53	36	46	30	44	32	28	22	26	22
C0		37	—	34	22	30	—	28	20	22	—	18	18
S4-S0		55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0													
A15-A0, B15-B0		—	36	46	37	—	30	40	32	—	22	22	22
Clock		32	—	—	—	26	—	—	—	22	—	—	—
C0		—	—	34	22	—	—	28	20	—	—	18	18
S4-S0		—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1													
A15-A0, B15-B0		55	36	46	37	40	30	40	32	26	22	22	22
Clock		56	38	53	36	46	30	44	32	28	22	26	22
C0		37	—	34	22	30	—	28	20	22	—	18	18
S4-S0		55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE Notes 9, 10 (ns)												
Input	L4C383-55*				L4C383-40*				L4C383-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A0, B15-B0	8	2	35	2	8	2	28	2	8	2	16	2
C0	21	0	21	0	16	0	16	0	8	0	8	0
S4-S0	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{\text{ENA}}, \overline{\text{ENB}}, \overline{\text{ENF}}$	10	2	10	2	10	2	10	2	8	2	8	2

TRI-STATE ENABLE/DISABLE TIMES Notes 9, 10, 11 (ns)			
	L4C383-55*	L4C383-40*	L4C383-26
t _{ENA}	20	18	16
t _{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH Notes 9, 10 (ns)			
	L4C383-55*	L4C383-40*	L4C383-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

*DISCONTINUED SPEED GRADE

Arithmetic Logic Units

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS Notes 9, 10 (ns)										
To Output From Input		L4C383-20				L4C383-15*				
		F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16	
FTAB = 0, FTF = 0										
Clock		11	20	20	20	11	15	15	15	
C0		—	—	14	14	—	—	13	13	
S4-S0		—	18	20	18	—	14	15	14	
FTAB = 0, FTF = 1										
Clock		20	20	20	20	15	15	15	15	
C0		18	—	14	14	14	—	13	13	
S4-S0		20	18	20	18	15	14	15	14	
FTAB = 1, FTF = 0										
A15-A0, B15-B0		—	16	20	17	—	14	15	14	
Clock		11	—	—	—	11	—	—	—	
C0		—	—	14	14	—	—	13	13	
S4-S0		—	18	20	18	—	14	15	14	
FTAB = 1, FTF = 1										
A15-A0, B15-B0		20	16	20	17	15	14	15	14	
Clock		20	20	20	20	15	15	15	15	
C0		18	—	14	14	14	—	13	13	
S4-S0		20	18	20	18	15	14	15	14	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE Notes 9, 10 (ns)										
Input		L4C383-20				L4C383-15*				
		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		
		Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	
A15-A0, B15-B0		5	0	14	0	5	0	12	0	
C0		12	0	12	0	10	0	10	0	
S4-S0		15	0	15	0	12	0	12	0	
EN \bar{A} , EN \bar{B} , EN \bar{F}		5	0	5	0	5	0	5	0	

TRI-STATE ENABLE/DISABLE TIMES Notes 9, 10, 11 (ns)			
	L4C383-20	L4C383-15*	
t _{ENA}	8	6	
t _{DIS}	8	6	

CLOCK CYCLE TIME AND PULSE WIDTH Notes 9, 10 (ns)			
	L4C383-20	L4C383-15*	
Minimum Cycle Time	18	14	
Highgoing Pulse	5	4	
Lowgoing Pulse	5	4	

*DISCONTINUED SPEED GRADE

16-bit Cascadable ALU (Extended Set)
SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)
GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output From Input	L4C383-65*				L4C383-45*				L4C383-30*			
	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C0	—	—	42	25	—	—	32	23	—	—	22	22
S4-S0	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S4-S0	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A15-A0, B15-B0	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C0	—	—	42	25	—	—	32	23	—	—	22	22
S4-S0	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A15-A0, B15-B0	65	44	56	44	45	32	46	36	30	28	28	28
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C0	42	—	42	25	32	—	32	23	26	—	22	22
S4-S0	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C383-65*				L4C383-45*				L4C383-30*			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A0, B15-B0	10	3	43	3	8	3	33	3	8	3	20	3
C0	25	0	25	0	20	0	20	0	12	0	12	0
S4-S0	50	0	50	0	36	0	36	0	20	0	20	0
EN \bar{A} , EN \bar{B} , EN \bar{F}	12	2	12	2	10	2	10	2	10	2	10	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C383-65*	L4C383-45*	L4C383-30*
t _{ENA}	22	20	18
t _{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C383-65*	L4C383-45*	L4C383-30*
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

*DISCONTINUED SPEED GRADE

Arithmetic Logic Units

16-bit Cascadable ALU (Extended Set)

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS Notes 9, 10 (ns)										
To Output From Input		L4C383-25*				L4C383-20*				
		F15-F0	N	OVF, Z	C16	F15-F0	N	OVF, Z	C16	
FTAB = 0, FTF = 0										
Clock		14	24	24	24	14	20	20	20	
C0		—	—	18	18	—	—	16	16	
S4-S0		—	22	24	22	—	18	20	18	
FTAB = 0, FTF = 1										
Clock		25	24	24	24	20	20	20	20	
C0		21	—	18	18	17	—	16	16	
S4-S0		25	22	24	22	20	18	20	18	
FTAB = 1, FTF = 0										
A15-A0, B15-B0		—	20	25	22	—	17	20	17	
Clock		14	—	—	—	14	—	—	—	
C0		—	—	18	18	—	—	16	16	
S4-S0		—	22	24	22	—	18	20	18	
FTAB = 1, FTF = 1										
A15-A0, B15-B0		25	20	25	22	20	17	20	17	
Clock		25	24	24	24	20	20	20	20	
C0		21	—	18	18	17	—	16	16	
S4-S0		25	22	24	22	20	18	20	18	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE Notes 9, 10 (ns)									
Input	L4C383-25*				L4C383-20*				
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	
A15-A0, B15-B0	7	2	14	2	6	2	12	2	
C0	14	0	14	0	12	0	12	0	
S4-S0	19	0	19	0	16	0	16	0	
EN \bar{A} , EN \bar{B} , EN \bar{F}	7	0	7	0	6	0	6	0	

TRI-STATE ENABLE/DISABLE TIMES Notes 9, 10, 11 (ns)			
	L4C383-25*	L4C383-20*	
t _{ENA}	14	10	
t _{DIS}	14	10	

CLOCK CYCLE TIME AND PULSE WIDTH Notes 9, 10 (ns)			
	L4C383-25*	L4C383-20*	
Minimum Cycle Time	20	18	
Highgoing Pulse	8	6	
Lowgoing Pulse	8	6	

*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

4

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

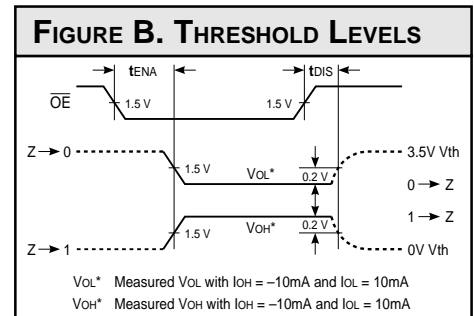
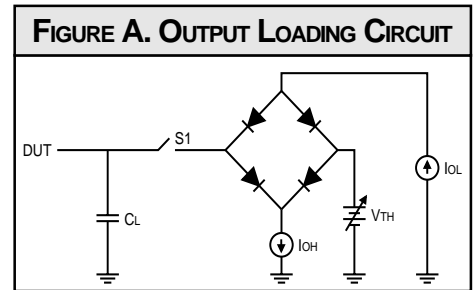
This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

- a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.
- b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.
- c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

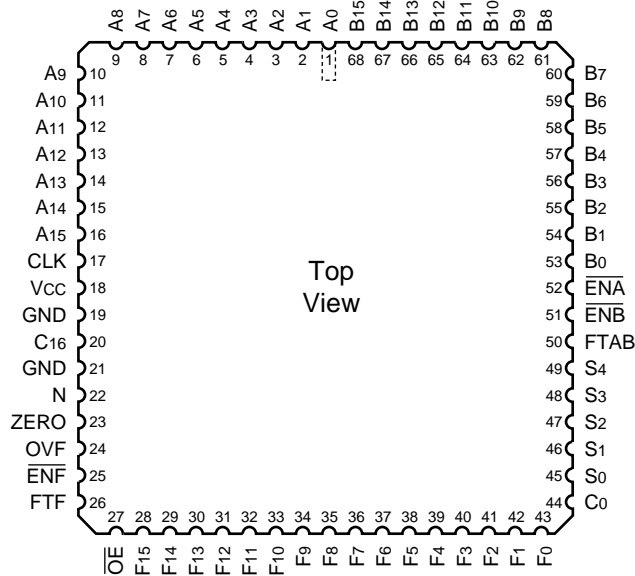
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.



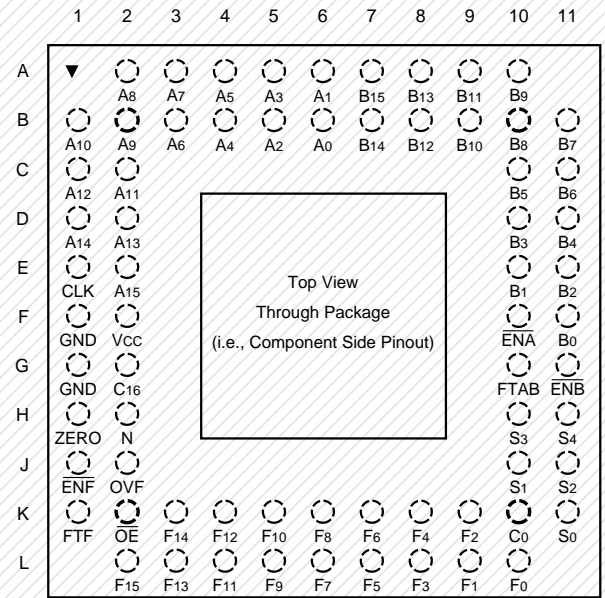
16-bit Cascadable ALU (Extended Set)

ORDERING INFORMATION

68-pin



68-pin



Discontinued Package

Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — COMMERCIAL SCREENING	
26 ns 20 ns	L4C383JC26 L4C383JC20	
	-55°C to +125°C — COMMERCIAL SCREENING	
	-55°C to +125°C — MIL-STD-883 COMPLIANT	