AMERICAN MICROSYSTEMS, INC.

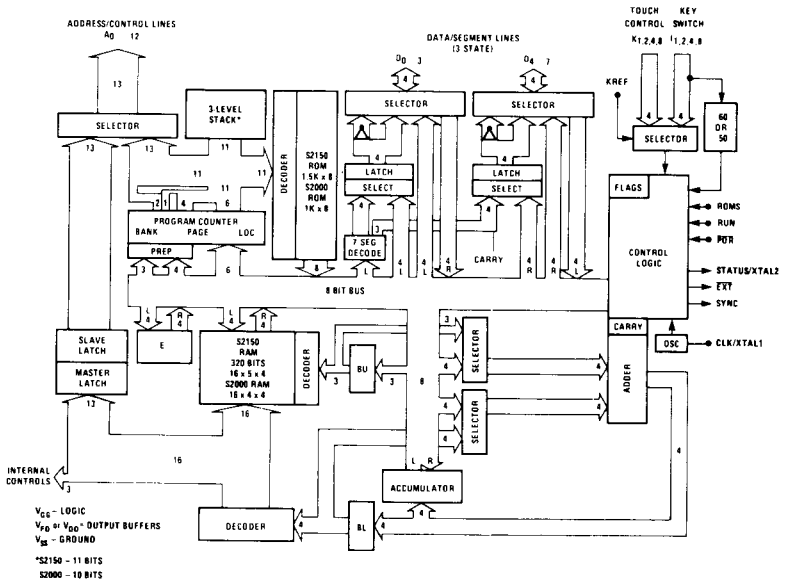
S2000/S2150/A/S2152

SINGLE-CHIP MICROCOMPUTERS

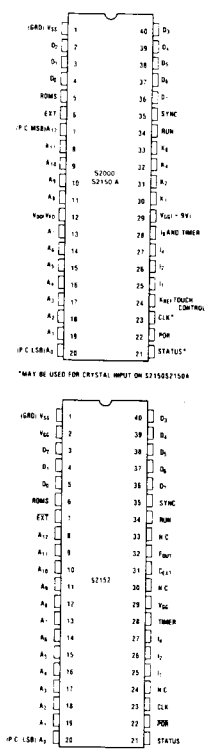
Features

- ☐ 1024×8 Program ROM On-Chip; Externally Expandable to 8192×8—S2000
- ☐ 1536×8 Program ROM On-Chip; Externally Expandable to 8192×8—S2150
- ☐ 64×4 Scratchpad RAM On-Chip—S2000
- ☐ 80×4 Scratchpad RAM On-Chip—S2150
- ☐ 14 Outputs, 8 Inputs, Plus 8 Bi-Directional Three-State Lines
- ☐ TouchControl Capacitive Touchplate Interface
- ☐ Seconds Timer for Both 60Hz and 50Hz Lines
- ☐ 7-Segment Decoder
- ☐ LED Display Drivers—S2000/S2150
- ☐ Vacuum Fluorescent Display Drivers—S2000/S2150A
- ☐ Single +9V Supply
- ☐ Fast 4.5μs Execution Cycle
- ☐ Three-Level Subrouting Stack
- ☐ TTL-Compatible Outputs
- ☐ Reset, Test, and Single Step Modes
- ☐ Crystal Input for Accurate Clocking—S2150
- ☐ S2152:D-To-F Converter Programmable Divide-by-N Counter/Timer

Block Diagram



Pin Configuration



Functional Description

The S2000/S2150 are ideal for a wide range of appliance and process control designs. Versatile input/output and an instruction set optimized for its intended applications make the S2000 preferable to expensive multiple-chip solutions with dramatic cost reductions during product design, manufacture, testing, and maintenance.

The S2000/S2150 have an on-chip 1024/1536 instruction ROM. If necessary, additional program memory can be added externally up to a maximum of 8192 instructions. The Program Counter is a pointer to the next instruction to be executed. The Subroutine Stack holds return addresses during execution of subroutines.

The scratchpad RAM holds the temporary values of 64/80 4-bit data words, typically numeric quantities. The BU and BL registers are used to access RAM words. The E Register can be used as a general purpose register or as an index limit register for controlling RAM accesses.

The ALU—Arithmetic Logic Unit—performs data operations, using the Accumulator and the Carry Register. Software can set and test two Flags as temporary indicators.

The Control Logic includes three inputs and three outputs for interfacing external devices. The Oscillator generates all clocking signals and needs only an external RC circuit to set its rate. The KREF Input is the analog reference for TouchControl and similar interfaces. Software decision-making instructions sample the four K Inputs and the four I Inputs, one of which can be used as a line-frequency counter.

The eight bi-directional three-state D Lines are general-purpose data signals. The thirteen A Lines are outputs for displays, keyboard strobes, control signals, or address lines for external ROM.

General Description for S2152

The S2152 is an extension of the S2000/S2150 and is software compatible with them. It has the following enhanced features:

- ☐ Digital-To-Frequency Converter (4-Bit)
- ☐ Programmable Divide-by-N Counter/Timer
- ☐ 15 Outputs, 4 Inputs, and 8 Bi-Directional Three-State Lines
- ☐ One Open Drain Output, and
- ☐ High Current Outputs

S2000/S2150/A/S2152 Instruction Set Summary

ADCS	ACC+RAM+CARRY, Skip if Sum≤15
ADD	ACC+RAM
ADIS X	ACC+X, Skip if Sum≤15
AND	ACC "AND" RAM
CMA	Complement ACC
DISB	Display Number in Binary Format
DISN	Display Number in Seven Segment Format
EUR	(European) SET 50/60Hz and Display Latch Polarity
INP	Input 8 Bits from D Lines
JMP X	Jump
JMS X	Jump to Subroutine
LAB	Load ACC with BL
LAE	Load ACC with E
LAI X	LOAD ACC with X
LAM Y	LOAD ACC with RAM then BU "XOR"Y
LBE Y	Load BL with E and BU with Y
LBF Y	Load BL with 15 and BU with Y
LBEP Y	Load BL with E+1 and BU with Y
LBZ Y	Load BL with 0 and BU with Y
MVS	Move Master Latch to Slave Latch
NOP	No Operation
OUT	Output 8 Bits to D Lines
PP X	Prepare Page (or Bank)
PSH	Preset Master Strobe High
PSL	Preset Master Strobe Low
RF1	Reset Flag 1
RF2	Reset Flag 2
RSC	Reset Carry
RSM Z	Reset RAM Bit Z
RT	Return from Subroutine
RTS	Return from Subroutine and Skip
SAM	Skip if ACC=RAM
SBE	Skip if BL=E
SF1	Set Flag1
SF2	Set Flag2
SOS	Skip if Seconds Flag Set
STC	Set Carry
STM Z	Set RAM Bit Z
SZC	Skip if Carry=0
SZI	Skip if I=0
SZK	Skip if K=0
SZM Z	Skip if RAM Bit Z=0
TF1	Skip if Flag1=1
TF2	Skip if Flag2=1
XAB	Exchange ACC with BL
XABU	Exchange ACC with BU
XAE	Exchange ACC with E
XC Y	Exchange ACC with RAM then BU "XOR"Y
XCD Y	Exchange ACC and RAM, BU "XOR"Y, Decrement BL, and Skip if BL=0 Before Decrementing
XCI Y	Exchange ACC and RAM, BU "XOR"Y, Increment BL, and Skip if BL=0 After Incrementing
XOR	ACC "Exclusive-OR" RAM