AK4366

Low Power 24-Bit 2ch DAC with HP-AMP

GENERAL DESCRIPTION

The AK4366 is 24bit DAC with built-in Headphone Amplifier. The integrated headphone amplifier features "pop-free" power-on/off, a mute control and delivers 50mW of power at 16Ω. The AK4366 is housed in a 16pin TSSOP package, making it suitable for portable applications.

FEATURE

- ☐ **Multi-bit ΔΣ DAC**
- ☐ **Sampling Rate: 8kHz~48kHz**
- ☐ **64x Oversampling**
- ☐ **On chip perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 54dB**
- ☐ **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- ☐ **System Clock: 256fs/384fs/512fs**
  - **AC Couple Input Available**
- ☐ **Audio I/F Format: MSB First, 2's Compliment**
  - **I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified**
- ☐ **μP Interface: 3-wire**
- ☐ **Bass Boost Function**
- ☐ **Headphone Amplifier**
  - **Output Power: 50mW x 2ch @16Ω, 3.3V**
  - **S/N: 92dB@2.4V**
  - **Pop noise Free at Power-ON/OFF and Mute**
- ☐ **Power Supply: 2.2V ~ 3.6V**
- ☐ **Power Supply Current: 2.6mA@2.4V (@HP-AMP no-output)**
- ☐ **Ta: –40 ~ 85°C**
- ☐ **Small Package: 16pin TSSOP**

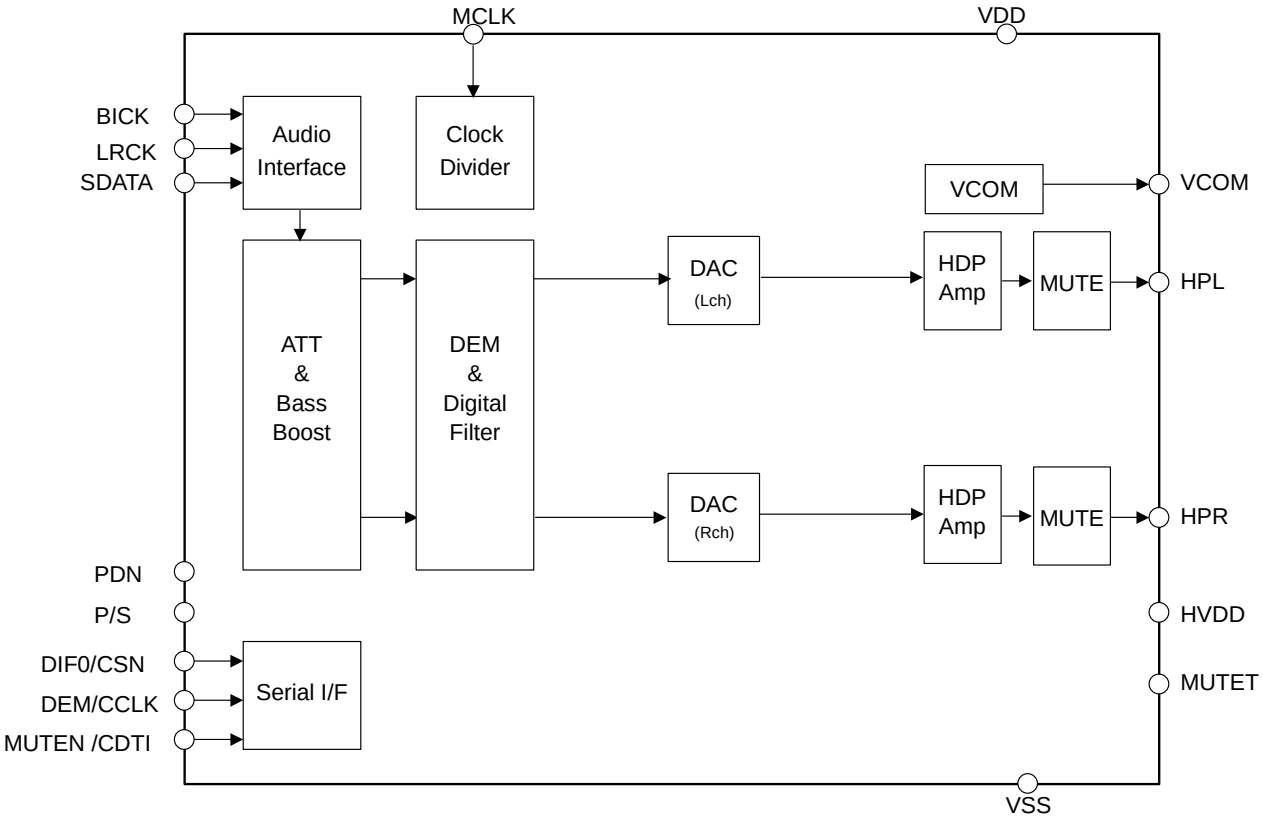
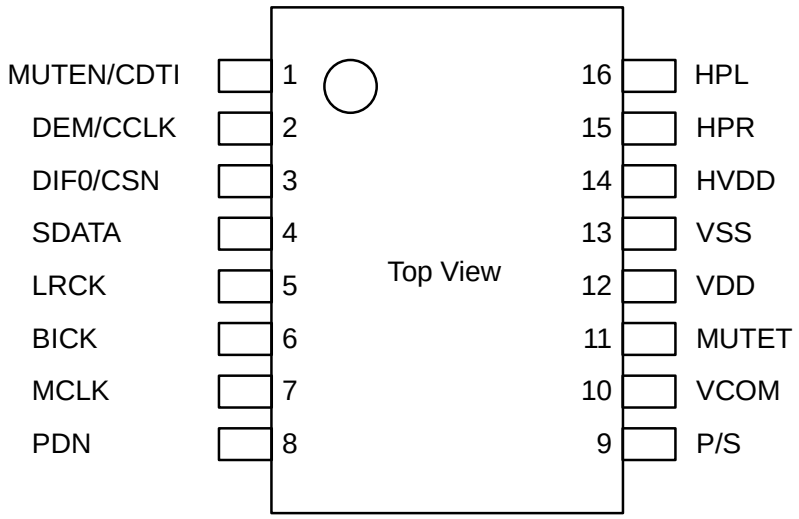


Figure 1. AK4366 Block Diagram

■ Ordering Guide

AK4366VT	–40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4366	Evaluation board for AK4366	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MUTEN	I	Headphone Amp Mute Pin (P/S pin = "H") "H": Normal operation, "L": Mute
	CDTI	I	Control Data Input Pin (P/S pin = "L")
2	DEM	I	De-emphasis Pin (P/S pin = "H") "H": ON(44.1kHz), "L": OFF
	CCLK	I	Control Data Clock Pin (P/S pin = "L")
3	DIF0	I	Audio Interface Format Pin (P/S pin = "H") "H": I^2S, "L": 24bit MSB justified
	CSN	I	Control Data Chip Select Pin (P/S pin = "L")
4	SDATA	I	Audio Serial Data Input Pin
5	LRCK	I	L/R Clock Pin This clock determines which audio channel is currently being input on SDATA pin.
6	BICK	I	Serial Bit Clock Pin This clock is used to latch audio data.
7	MCLK	I	Master Clock Input Pin
8	PDN	I	Power-down & Reset Pin When at "L", the AK4366 is in power-down mode and is held in reset. The AK4366 should always be reset upon power-up.
9	P/S	I	Control Mode Select Pin (Internal Pull-down Pin) "H": Parallel, "L": 3-wire Serial
10	VCOM	O	Common Voltage Output Pin Normally connected to VSS pin with 0.1μF ceramic capacitor in parallel with a 2.2μF electrolytic capacitor.
11	MUTET	O	Mute Time Constant Control Pin Connected to VSS pin with a capacitor for mute time constant.
12	VDD	-	Power Supply Pin
13	VSS	-	Ground Pin
14	HVDD	-	Power Supply Pin for Headphone Amp
15	HPR	O	Rch Headphone Amp Output Pin
16	HPL	O	Lch Headphone Amp Output Pin

Note: All digital input pins except internal pull-down pin must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MUTET, HPR, HPL	These pins should be open.
Digital	DEM, DIF0	These pins should be connected to VSS.

ABSOLUATE MAXIMUM RATING

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog, Digital	VDD	–0.3	4.6	V
	HP-AMP	HVDD	–0.3	4.6	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Input Voltage		VIN	–0.3	VDD+0.3 or 4.6	V
Ambient Temperature		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog, Digital	VDD	2.2	2.4	3.6	V
(Note 2)	HP-AMP	HVDD	2.2	2.4	3.6	V

Note 1. All voltages with respect to ground.
Note 2. VDD should be same voltage as HVDD.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=HVDD=2.4V, VSS=0V; fs=44.1kHz; BOOST OFF; Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Load impedance is a serial connection with R_L=16Ω and C_L=220μF. (Refer to Figure 19); unless otherwise specified)

Parameter			min	typ	max	Units
DAC Resolution			-	-	24	bit
Headphone-Amp: (HPL/HPR pins) (Note 3)						
Analog Output Characteristics						
THD+N	(–4.8dBFS Output, Po=10mW@16Ω, 2.4V)		-	–55	–45	dB
	(–3dBFS Output, Po=28mW@16Ω, 3.3V)		-	–55	-	dB
	(–3dBFS Output, Po=14mW@32Ω, 3.3V)		-	–57	-	dB
D-Range	(–60dBFS Output, A-weighted, 2.4V)		84	92	-	dB
	(–60dBFS Output, A-weighted, 3.3V)		-	94	-	dB
S/N	(A-weighted, 2.4V)		84	92	-	dB
	(A-weighted, 3.3V)		-	94	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.2	-	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance		(Note 4)	16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage	(–4.8dBFS Output)	(Note 5)	1.02	1.13	1.24	Vpp
Max Output Power	(R_L=16Ω, 2.4V)		-	26	-	mW
	(R_L=16Ω, 3.3V)		-	50	-	mW
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")		(Note 6)				
VDD			-	1.6	2.8	mA
HVDD			-	1.0	2.0	mA
Power-Down Mode (PDN pin = "L")		(Note 7)	-	1	100	μA

Note 3. DACL=DACR= "1", ATTL=ATTR=0dB.

Note 4. AC Load

Note 5. Output voltage is proportional to VDD voltage. Vout = 0.47 x VDD(typ)@–4.8dBFS.

Note 6. PMDAC=PMHPL=PMHPR= "1", MUTEN= "1" and HP-Amp output is off.

Note 7. All digital input pins including clock pins (MCLK, BICK and LRCK) are held at VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 8)							
Passband	–0.05dB	(Note 9)	PB	0	-	20.0	kHz
	–6.0dB			-	22.05	-	kHz
Stopband		(Note 9)	SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay		(Note 10)	GD	-	20.8	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 8) (Note 11)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
BOOST Filter:	(Note 11) (Note 12)						
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 8. BOOST OFF (BST1-0 bit = "00")

Note 9. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.05dB), SB=0.546*fs(@–54dB).

Note 10. This is the calculated delay time caused by digital filtering. This time is measured from the setting of the 24bit data of both channels to the input registers to the output of the analog signal.

Note 11. DAC → HPL, HPR

Note 12. These frequency responses scale with fs. If high-level signal is input, the AK4366 clips at low frequency.

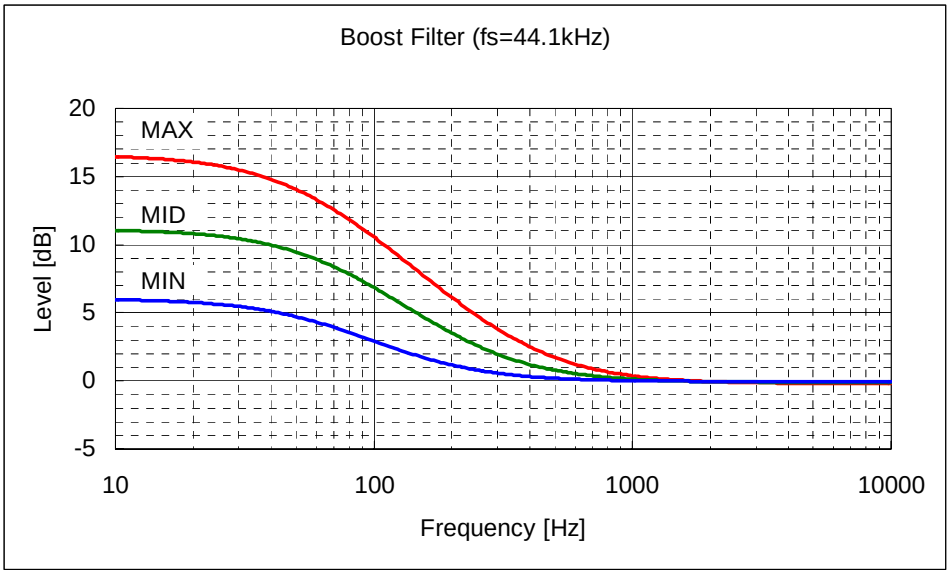


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling	(Note 13)	VAC	1.0	-	-	Vpp
Input Leakage Current	(Note 14)	Iin	-	-	±10	μA

Note 13. Only MCLK pin. (Figure 19)

Note 14. P/S pin has internal pull-down device, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	2.048	-	24.576	MHz
Pulse Width Low	(Note 15)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	(Note 15)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width	(Note 18)	tACW	20	-	-	ns
LRCK Timing						
Frequency		fs	8	44.1	48	kHz
Duty Cycle:		Duty	45	-	55	%
Serial Interface Timing (Note 16)						
BICK Period		tBCK	1/(64fs)	-	-	ns
BICK Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	50	-	-	ns
SDATA Hold Time		tSDH	50	-	-	ns
SDATA Setup Time		tSDS	50	-	-	ns
Control Interface Timing						
CCLK Period		tCCK	200	-	-	ns
CCLK Pulse Width Low		tCCKL	80	-	-	ns
Pulse Width High		tCCKH	80	-	-	ns
CDTI Setup Time		tCDS	40	-	-	ns
CDTI Hold Time		tCDH	40	-	-	ns
CSN "H" Time		tCSW	150	-	-	ns
CSN "↑" to CCLK "↑"		tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"		tCSH	50	-	-	ns

Note 15. Except AC coupling.

Note 16. Refer to "Serial Data Interface".

Note 17. BICK rising edge must not occur at the same time as LRCK edge.

Note 18. Pulse width to ground level when MCLK is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)

■ Timing Diagram

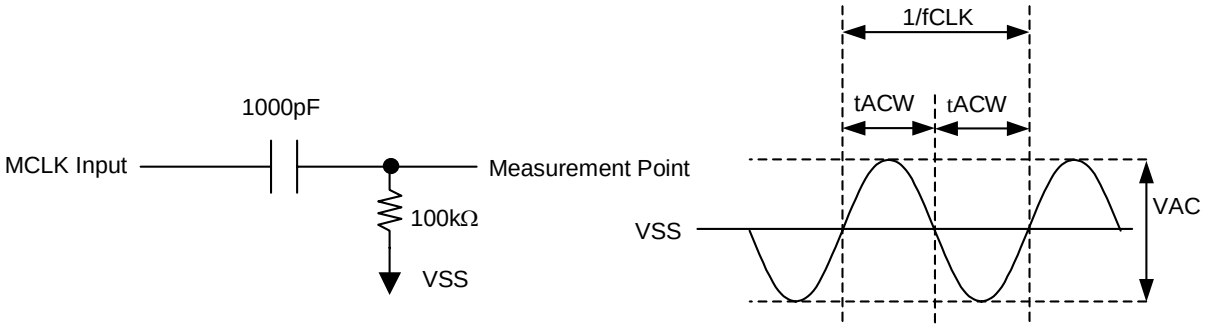


Figure 3. MCLK AC Coupling Timing

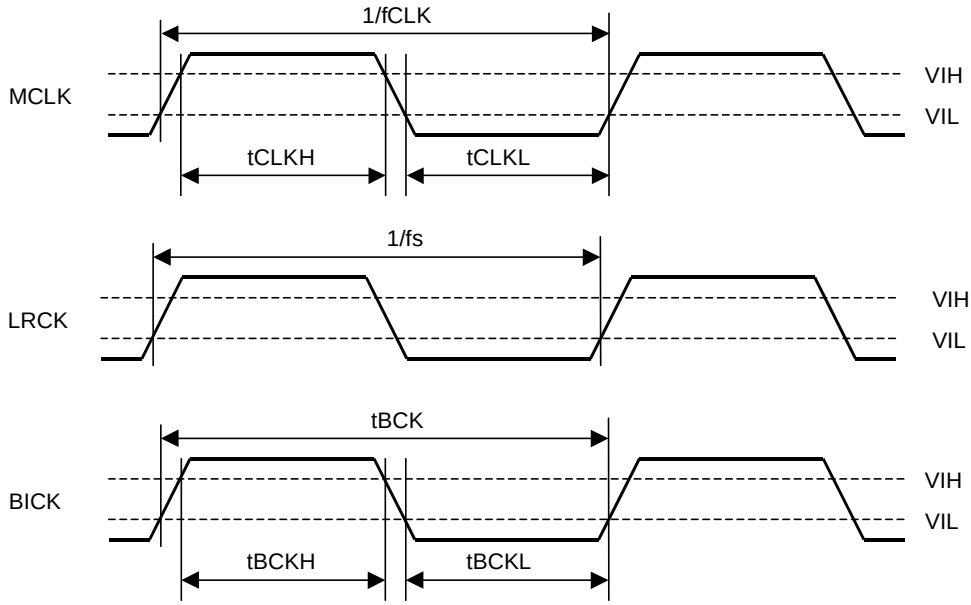


Figure 4. Clock Timing

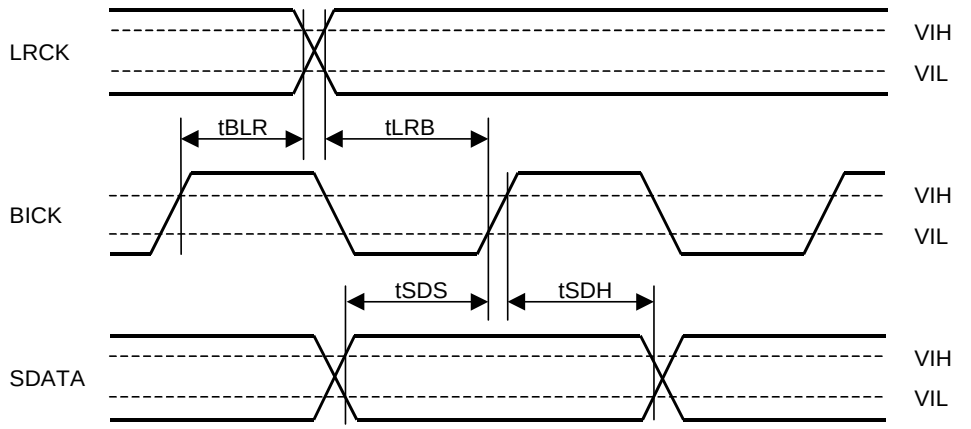


Figure 5. Serial Interface Timing

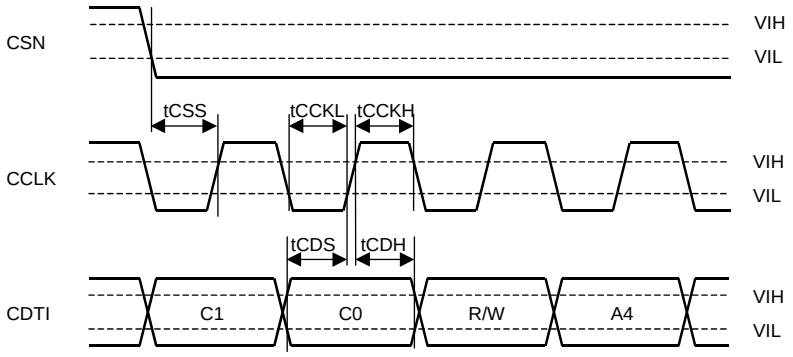


Figure 6. WRITE Command Input Timing

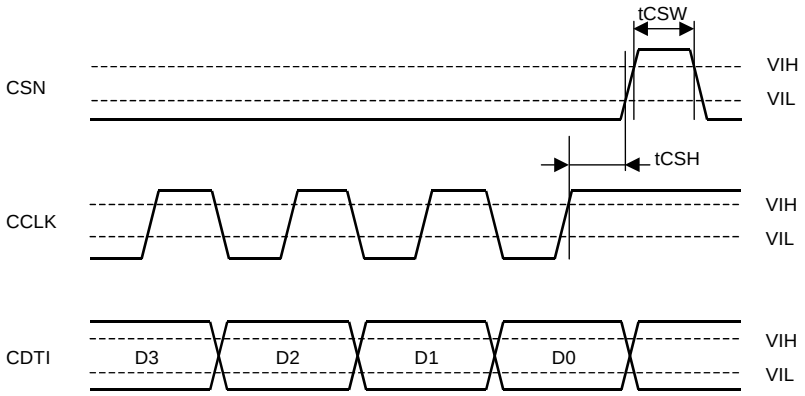


Figure 7. WRITE Data Input Timing

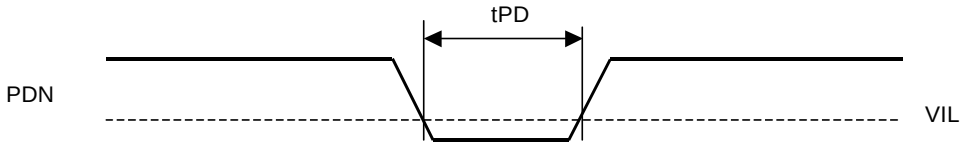


Figure 8. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4366 are MCLK(256fs/384fs/512fs), LRCK(fs) and BICK. The master clock (MCLK) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. The frequency of MCLK is detected automatically, and the internal master clock becomes the appropriate frequency. Table 1 shows system clock example.

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
8kHz	2.048	3.072	4.096	0.512
11.025kHz	2.8224	4.2336	5.6448	0.7056
12kHz	3.072	4.608	6.144	0.768
16kHz	4.096	6.144	8.192	1.024
22.05kHz	5.6448	8.4672	11.2896	1.4112
24kHz	6.144	9.216	12.288	1.536
32kHz	8.192	12.288	16.384	2.048
44.1kHz	11.2896	16.9344	22.5792	2.8224
48kHz	12.288	18.432	24.576	3.072

Table 1. System Clock Example

In serial mode (P/S pin = “L”), all external clocks (MCLK, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = “1”). If these clocks are not provided, the AK4366 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = “0”). When MCLK is input with AC coupling, the MCKAC bit should be set to “1”.

In parallel mode (P/S pin = “H”), all external clocks (MCLK, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PDN pin = “H”). If these clocks are not provided, the AK4366 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PDN pin = “L”).

For low sampling rates, DR and S/N degrade because of the outband noise. In serial mode (P/S pin = “L”), DR and S/N are improved by setting DFS1 bit to “1”. Table 2 shows S/N of HP-amp output. When the DFS1 bit is “1”, MCLK needs 512fs.

DFS1	DFS0	Over Sample Rate	fs	MCLK	S/N (fs=8kHz, A-weighted) HP-amp	
0	0	64fs	8kHz~48kHz	256fs/384fs/512fs	56dB	Default
0	1	128fs	8kHz~24kHz	256fs/384fs/512fs	75dB	
1	x	256fs	8kHz~12kHz	512fs	92dB	

Table 2. Relationship among fs, MCLK frequency and S/N of HP-amp

■ Serial Data Interface

The AK4366 interfaces with external system via the SDATA, BICK and LRCK pins. In serial mode (P/S pin = "L"), five data formats are available and are selected by setting DIF2, DIF1 and DIF0 bits (Table 3). In parallel mode (P/S pin = "H"), two data formats are available and are selected by setting DIF0 pin (Table 3). Mode 0 is compatible with existing 16bit DACs and digital filters. Mode 1 is a 20bit version of Mode 0. Mode 4 is a 24bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format.

DIF2 bit	DIF1 bit	DIF0 bit	MODE	BICK	Figure
0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 64fs	Figure 9
0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 64fs	Figure 10
0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 11
0	1	1	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 12
1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 64fs	Figure 10

Table 3. Audio Data Format (Serial Mode)

DIF0 pin	MODE	BICK	Figure
L	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 11
H	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 12

Table 4. Audio Data Format (Parallel Mode)

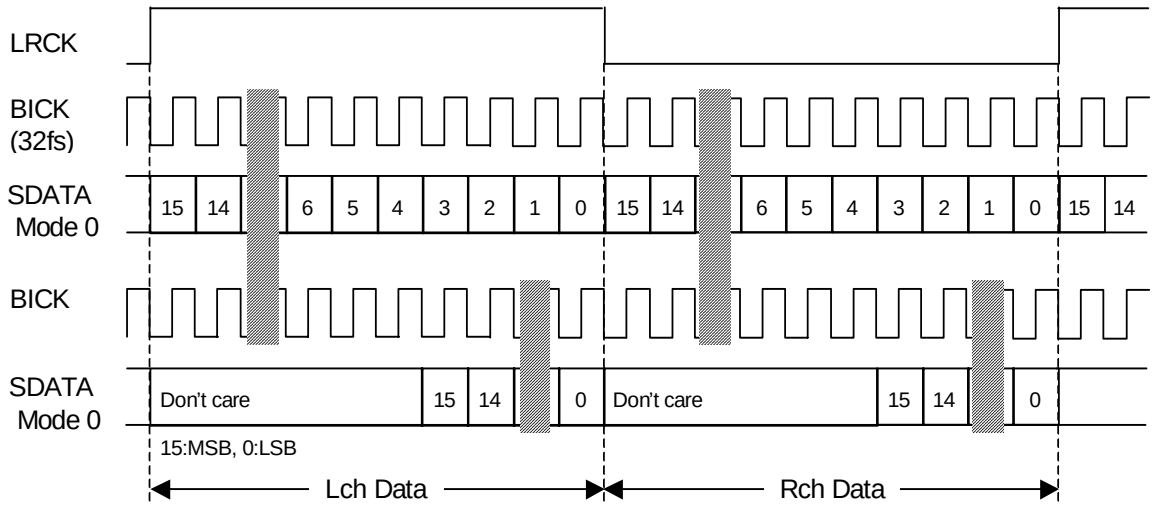


Figure 9. Mode 0 Timing

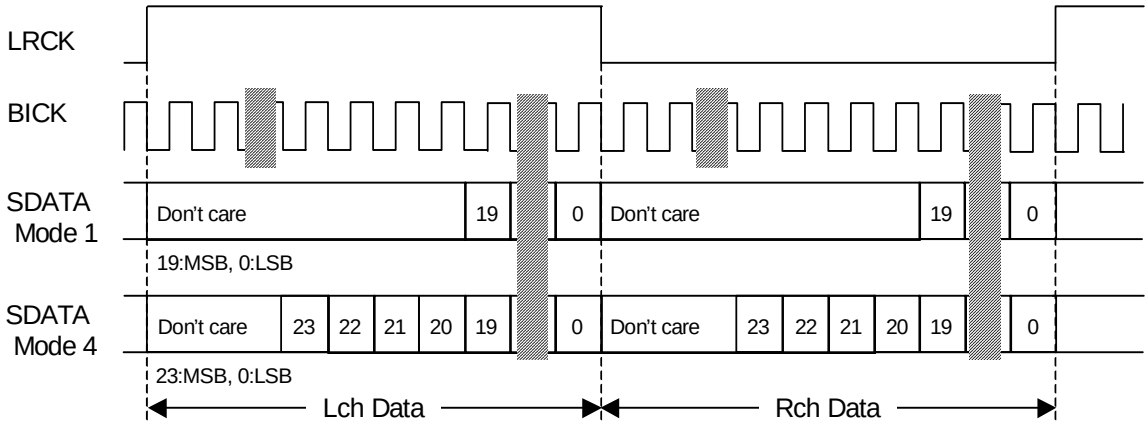


Figure 10. Mode 1, 4 Timing

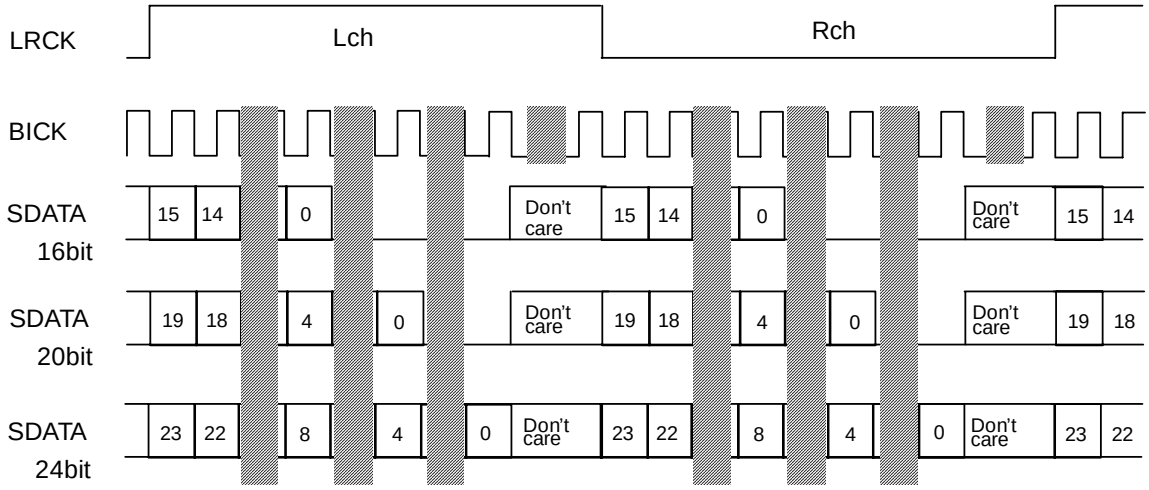


Figure 11. Mode 2 Timing

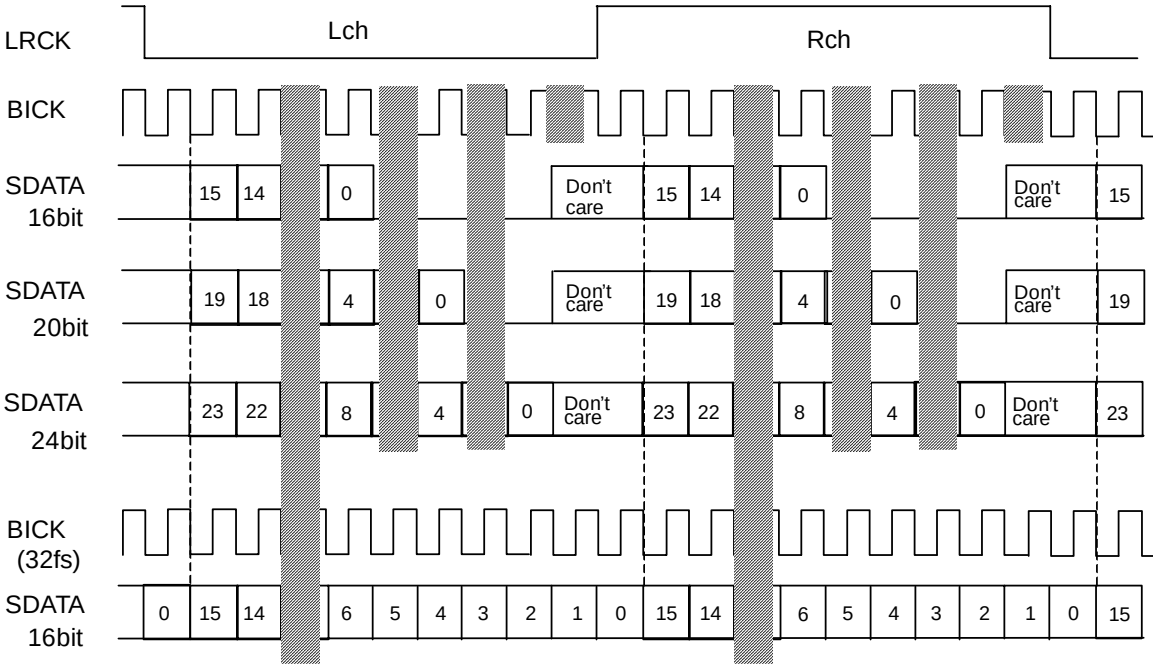


Figure 12. Mode 3 Timing

■ Digital Attenuator

The AK4366 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to −127dB or MUTE) for each channel (Table 5). At DATTC bit = "1", ATTL7-0 bits control both Lch and Rch attenuation levels. At DATTC bit = "0", ATTL7-0 bits control the Lch level and ATTR7-0 bits control the Rch level. In parallel mode (P/S pin = "H"), digital attenuator is fixed to 0dB. When HPM bit = "1", (L+R)/2 summation is done after volume control.

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 5. Digital Volume ATT values

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 6). When ATS bit = "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. Digital attenuator is independent of the soft mute function.

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 6. Transition time between set values of ATT7-0 bits

■ Soft Mute

Soft mute operation is performed at digital domain. In serial mode (P/S pin = "L"), when the SMUTE bit goes to "1", the output signal is attenuated by –∞ during ATT_DATA×ATT transition time (Table 6) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission. In parallel mode (P/S pin = "H"), soft mute is not available.

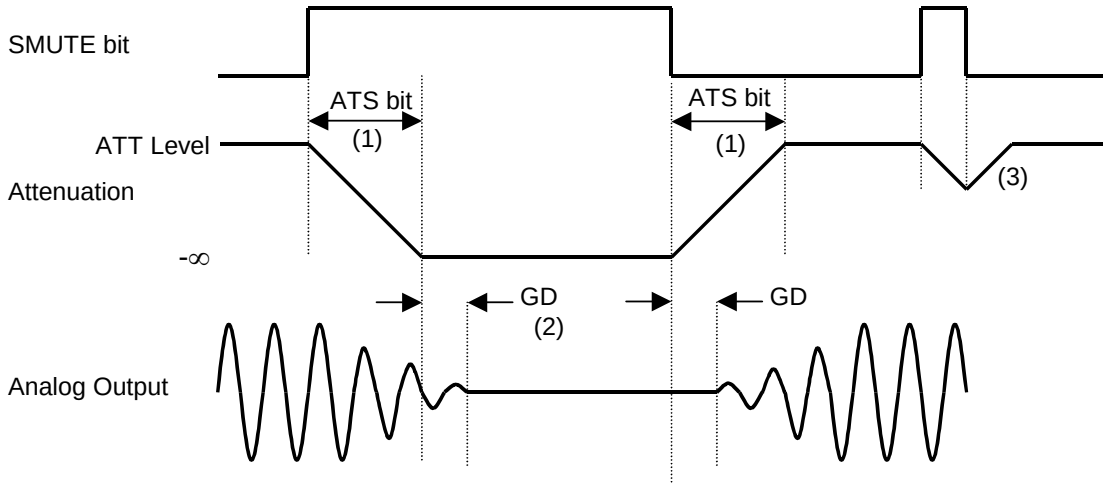


Figure 13. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time (Table 6). For example, this time is 3712LRCK cycles (3712/fs) at ATS bit = "1" and ATT_DATA = "128".
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

■ De-emphasis Filter

The AK4366 includes a digital de-emphasis filter (tc = 50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). In serial mode (P/S pin = "L"), the de-emphasis filter is enabled by setting DEM1-0 bits (Table 7).

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 7. De-emphasis Filter Frequency Select (Serial Mode)

In parallel mode (P/S pin = "H"), the de-emphasis filter corresponding to 44.1kHz is enabled by setting DEM pin "H" (Table 8).

DEM pin	De-emphasis
L	OFF
H	44.1kHz

Table 8. De-emphasis Filter Frequency Select (Parallel Mode)

■ Bass Boost Function

In serial mode (P/S pin = "L"), the low frequency boost signal can be output from DAC by controlling BST1-0 bits (Table 9). The setting value is common in Lch and Rch.

BST1 bit	BST0 bit	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 9. Low Frequency Boost Select

■ System Reset

The AK4366 should be reset once by bringing PDN "L" upon power-up.

In serial mode (P/S pin = "L"), after exiting reset, VCOM, DAC, HPL and HPR switch to the power-down state. The contents of the control register are maintained until the reset is done. DAC exits reset and power down state by MCLK after PMDAC bit is changed to "1", and then DAC is powered up and the internal timing starts clocking by LRCK "↑". DAC is in power-down mode until MCLK and LRCK are input.

In parallel mode (P/S pin = "H"), VCOM and DAC are powered up by PDN pin "H". Headphone amp is powered up by MUTEN pin "H". DAC exits reset and power down state by MCLK after PDN pin goes to "H", and then DAC is powered up and the internal timing starts clocking by LRCK "↑". DAC is in power-down mode until MCLK and LRCK are input.

■ Headphone Output

Power supply voltage for the Headphone-amp is supplied from the HVDD pin and centered on the 0.45 x VDD voltage. The Headphone-amp output load resistance is min.16Ω.

1) Parallel mode (P/S pin = "H")

When MUTEN pin is set to "H" at PDN pin = "H", common voltage goes to 0.45 x VDD. When MUTEN pin is set to "L", common voltage goes to VSS, and the outputs (HPL and HPR pins) are VSS. When PDN pin is "L", headphone amplifiers are powered-down perfectly, and the outputs (HPL and HPR pins) are VSS.

2) Serial mode (P/S pin = "L")

When the MUTEN bit is "1" at PMHPL=PMHPR= "1", the common voltage rises to 0.45 x VDD. When the MUTEN bit is "0", the common voltage of Headphone-amp falls and the outputs (HPL and HPR pins) go to VSS. When PMHPL and PMHPR bits are "0", the Headphone-amps are powered-down perfectly, and the outputs (HPL and HPR pins) are VSS.

A capacitor between the MUTET pin and ground reduces pop noise at power-up/down. It is recommended that the capacitor with small variation of capacitance and low ESR (Equivalent Series Resistance) over all temperature range, since the rise and fall time in Table 10 depend on the capacitance and ESR of the external capacitor at MUTET pin.

t_r: Rise Time up to VCOM/2	100k x C (typ)
t_f: Fall Time down to 0V	200k x C (typ)

Table 10. Headphone-Amp Rise/Fall Time

[Example] : A capacitor between the MUTET pin and ground = 1.0μF:
Time constant of rise time: t_r = 100kΩ x 1μF = 100ms(typ)
Time constant of fall time: t_f = 200kΩ x 1μF = 200ms(typ)

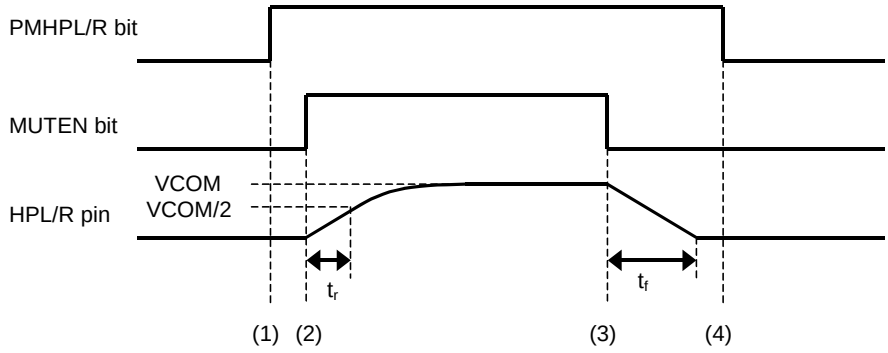


Figure 14. Power-up/Power-down Timing for Headphone-amp

(1) Headphone-amp power-up (PMHPL and PMHPR bits = "1"). The outputs are still VSS.
(2) Headphone-amp common voltage rise up (MUTEN bit = "1"). Common voltage of Headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The rise time up to VCOM/2 is t_r = 100k x C(typ) when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage fall down (MUTEN bit = "0"). Common voltage of Headphone-amp is falling to VSS. This fall time depends on the capacitor value connected with the MUTET pin. The fall time down to 0V is t_f = 200k x C(typ) when the capacitor value on MUTET pin is "C".
(4) Headphone-amp power-down (PMHPL, PMHPR bits = "0"). The outputs are VSS. If the power supply is switched off or Headphone-amp is powered-down before the common voltage goes to VSS, some pop noise occurs.

The cut-off frequency of Headphone-amp output depends on the external resistor and capacitor used. Table 11 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 2.4, 3.0 and 3.3V. The output voltage of headphone is 0.47 x VDD (Vpp) @−4.8dBFS.

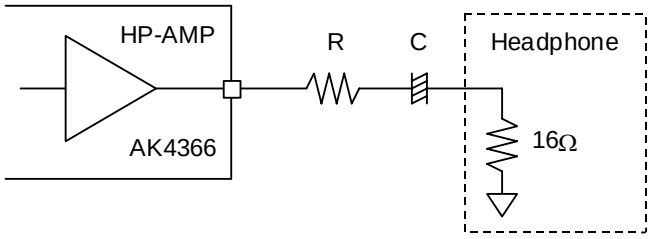


Figure 15. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]		
				2.4V	3.0V	3.3V
0	220	45	17	15	24	28
	100	100	43			
6.8	100	70	28	7	12	14
	47	149	78			
16	100	50	19	4	6	7
	47	106	47			

Table 11. Relationship of external circuit, output power and frequency response

■ Power-Up/Down Sequence

1) Parallel mode (P/S pin = “H”)

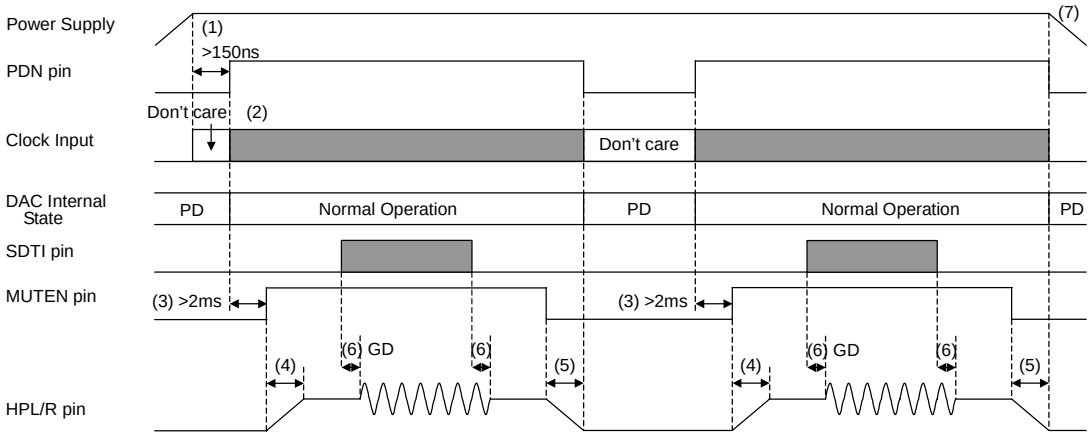


Figure 16. Power-up/down sequence of DAC and HP-amp

(1) PDN pin should be set to “H” at least 150ns after the power is supplied.
(2) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PDN pin = “L”, these clocks can be stopped. Headphone amp can operate without these clocks.
(3) MUTEN pin should be set to “H” at least 2ms after PDN pin goes to “H”.
(4) Rise time of headphone amp is determined by external capacitor (C) of MUTET pin. The rise time up to VCOM/2 is t_r = 100k x C(typ). When C=1µF, time constant is 100ms(typ).
(5) Fall time of headphone amp is determined by external capacitor (C) of MUTET pin. The fall time down to 0V is t_f = 200k x C(typ). When C=1µF, time constant is 200ms(typ).
PDN pin should be set to “L” after HPL and HPR pins go to VSS.
(6) Analog output corresponding to digital input has the group delay (GD) of 20.8/fs (=472µs@fs=44.1kHz).
(7) Power supply should be switched off after headphone amp is powered down (HPL/R pins become “L”).

2) Serial mode (P/S pin = "L")

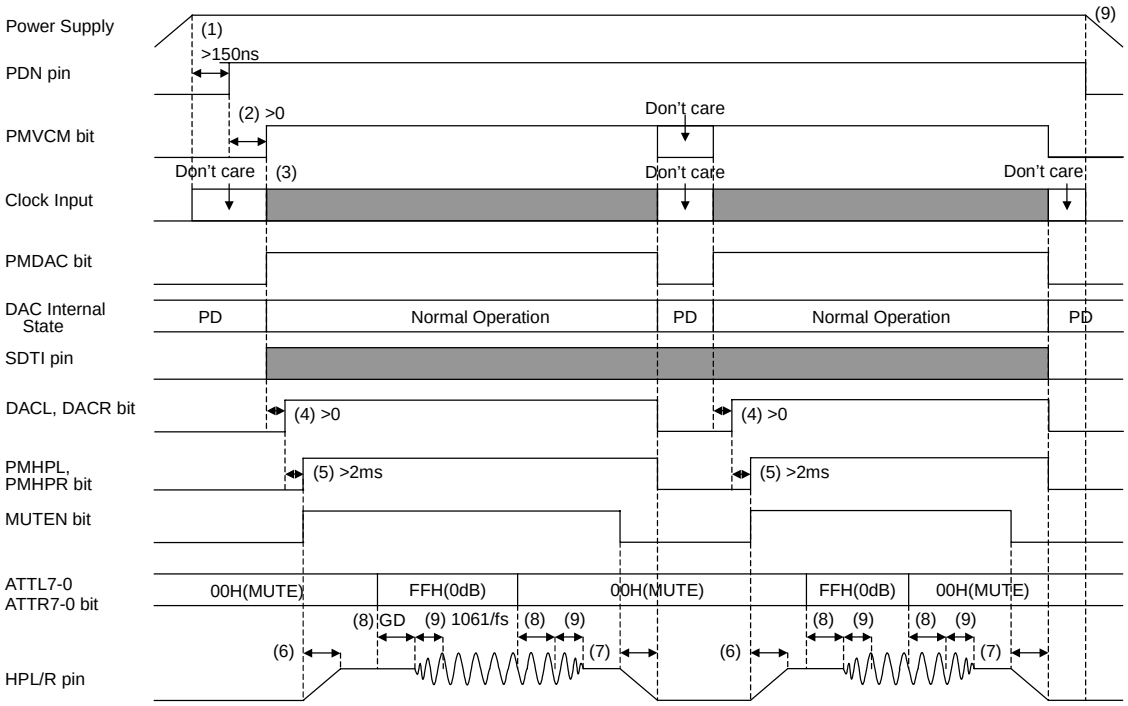


Figure 17. Power-up/down sequence of DAC and HP-amp

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) PMVCM and PMDAC bits should be changed to "1" after PDN pin goes to "H".
(3) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PMDAC bit = "0", these clocks can be stopped. Headphone amp can operate without these clocks.
(4) DACL and DACR bits should be changed to "1" after PMDAC bit is changed to "1".
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms (in case external capacitance at VCOM pin is 2.2μF) after DACL and DACR bits are changed to "1".
(6) Rise time of headphone amp is determined by external capacitor (C) of MUTET pin. The rise time up to VCOM/2 is t_r = 100k x C(typ). When C=1μF, time constant is 100ms(typ).
(7) Fall time of headphone amp is determined by external capacitor (C) of MUTET pin. The fall time down to 0V is t_f = 200k x C(typ). When C=1μF, time constant is 200ms(typ).
PMHPL, PMHPR, DACL and DACR bits should be changed to "0" after HPL and HPR pins go to VSS.
(8) Analog output corresponding to digital input has the group delay (GD) of 20.8/fs(=472μs@fs=44.1kHz).
(9) ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(10) Power supply should be switched off after headphone amp is powered down (HPL/R pins become "L").

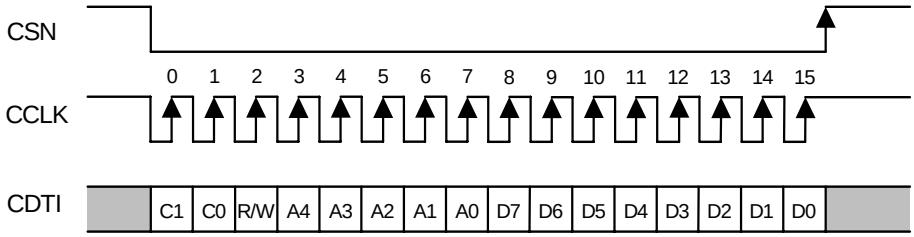
■ Mode Control Interface

Some function of AK4366 can be controlled by both pins (parallel control mode) and register (serial control mode) shown in Table 12. The serial control interface is enabled by the P/S pin = "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). AK4366 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by 16th CCLK "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel mode	Serial mode
De-emphasis	44.1kHz	32kHz/44.1kHz/48kHz
SMUTE	Not Available	Available
Audio I/F Format	I2S, Left justified	I2S, Left Justified, Right justified
Digital Attenuator	Not Available	Available
Bass Boost	Not Available	Available
Power Management	Not Available	Available
Default State at PDN pin = "L" → "H"	Power up	Power down

Table 12. Function List

PDN pin = "L" resets the registers to their default values. When the state of P/S pin is changed, AK4366 should be reset by PDN pin = "L".



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 18. 3-wire Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	Mode Control 0	0	MCKAC	HPM	DIF2	DIF1	DIF0	DFS1	DFS0
02H	Mode Control 1	0	0	0	SMUTE	BST1	BST0	DEM1	DEM0
03H	Mode Control 2	0	0	0	0	ATS	DATTC	BCKP	LRP
04H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
06H	Output Select	0	0	0	0	0	0	DACR	DACL

All registers inhibit writing at PDN pin = "L".
PDN pin = "L" resets the registers to their default values.
For addresses from 07H to 1FH, data must not be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON
In parallel mode (P/S pin = "H"), PMVCM bit is fixed to "1".

PMDAC: Power Management for DAC Blocks
0: Power OFF (Default)
1: Power ON
When PMDAC bit is changed from "0" to "1", DAC is powered-up to the current register values (ATT value, sampling rate, etc). In parallel mode (P/S pin = "H"), PMDAC bit is fixed to "1".

PMHPL: Power Management for Lch of Headphone Amp
0: Power OFF (Default). HPL pin becomes VSS (0V).
1: Power ON

PMHPR: Power Management for Rch of Headphone Amp
0: Power OFF (Default). HPR pin becomes VSS (0V).
1: Power ON

MUTEN: Headphone Amp Mute Control
0: Mute (Default). HPL and HPR pins go to VSS(0V).
1: Normal operation. HPL and HPR pins go to 0.45 x VDD.

All blocks can be powered-down by setting the PDN pin to "L" regardless of register values setup. All blocks can be also powered-down by setting all bits of this address to "0". In this case, control register values are maintained.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Mode Control 0	0	MCKAC	HPM	DIF2	DIF1	DIF0	DFS1	DFS0
Default		0	0	0	0	1	0	0	0

DFS1-0: Oversampling Speed Select (Table 2)
Default: “00” (64fs)

DIF2-0: Audio Data Interface Format Select (Table 3)
Default: “010” (Mode 2)

HPM: Mono Output Select of Headphone
0: Normal Operation (Default)
1: Mono. (L+R)/2 signals from the DAC are output to both Lch and Rch of headphone.

MCKAC: MCLK Input Mode Select
0: CMOS input (Default)
1: AC coupling input

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 1	0	0	0	SMUTE	BST1	BST0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (Table 7)
Default: “01” (OFF)

BST1-0: Low Frequency Boost Function Select (Table 9)
Default: “00” (OFF)

SMUTE: Soft Mute Control
0: Normal operation (Default)
1: DAC outputs soft-muted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 2	0	0	0	0	ATS	DATTC	BCKP	LRP
Default		0	0	0	0	0	0	0	0

LRP: LRCK Polarity Select
0: Normal (Default)
1: Invert

BCKP: BICK Polarity Select
0: Normal (Default)
1: Invert

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (Default)
1: Dependent
At DATTC bit = "1", ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. At DATTC bit = "0", ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

ATS: Digital attenuator transition time setting (Table 6)
0: 1061/fs (Default)
1: 7424/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL (Table 5)
ATTR7-0: Setting of the attenuation value of output signal from DACR (Table 5)
Default: "00H" (MUTE)

The AK4366 has channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to –127dB or MUTE) of each channel. Digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Output Select	0	0	0	0	0	0	DACR	DACL
Default		0	0	0	0	0	0	0	0

DACL: DAC Lch output signal is output to Lch of headphone amp.
0: OFF (Default)
1: ON

DACR: DAC Rch output signal is output to Rch of headphone amp.
0: OFF (Default)
1: ON

SYSTEM DESIGN

Figure 19 and Figure 20 shows the system connection diagram. An evaluation board [AKD4366] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

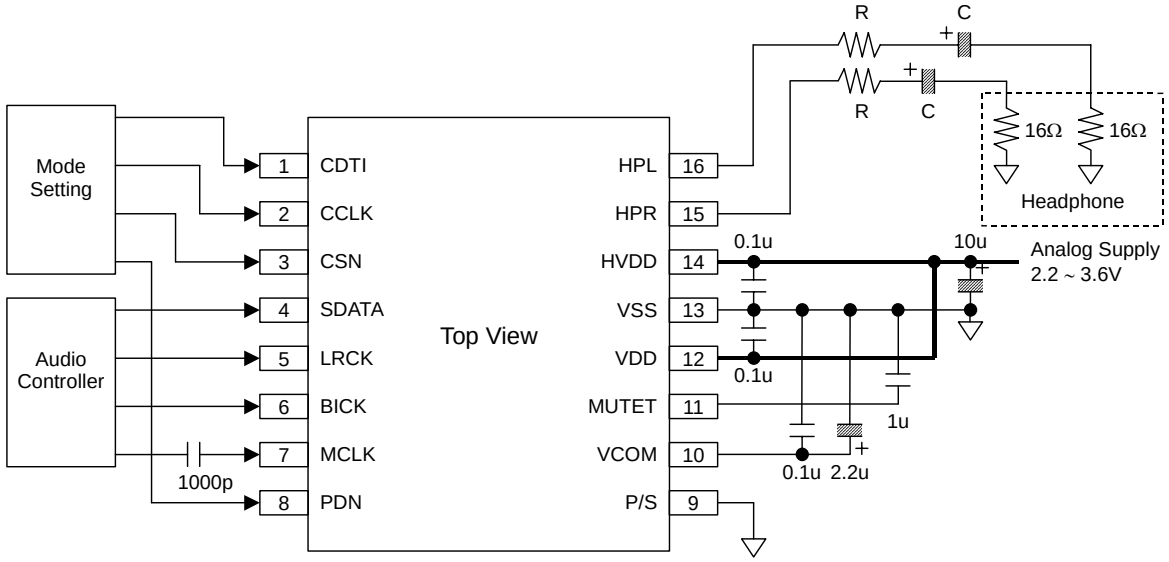


Figure 19. Typical Connection Diagram (In case of AC coupling to MCLK)
(P/S pin = "L": Serial mode)

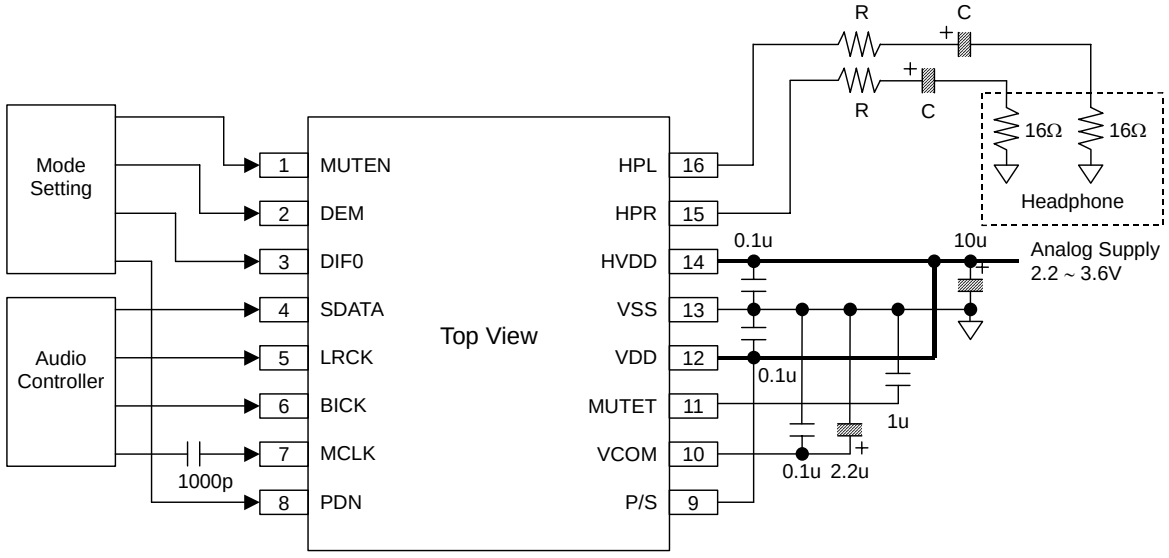


Figure 20. Typical Connection Diagram (In case of AC coupling to MCLK)
(P/S pin = "H": Parallel mode)

1. Grounding and Power Supply Decoupling

The AK4366 requires careful attention to power supply and grounding arrangements. VDD and HVDD are usually supplied from the analog power supply in the system. When VDD and HVDD are supplied separately, VDD must be powered-up at the same time or earlier than HVDD. When the AK4366 is powered-down, HVDD must be powered-down at the same time or later than VDD. VSS must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4366 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference

The input voltage to VDD sets the analog output range. A 0.1μF ceramic capacitor and a 10μF electrolytic capacitor is connected between VDD and VSS, normally. VCOM is a signal ground of this chip (0.45 x VDD). An electrolytic 2.2μF in parallel with a 0.1μF ceramic capacitor attached between VCOM and VSS eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from VDD and VCOM in order to avoid unwanted coupling into the AK4366.

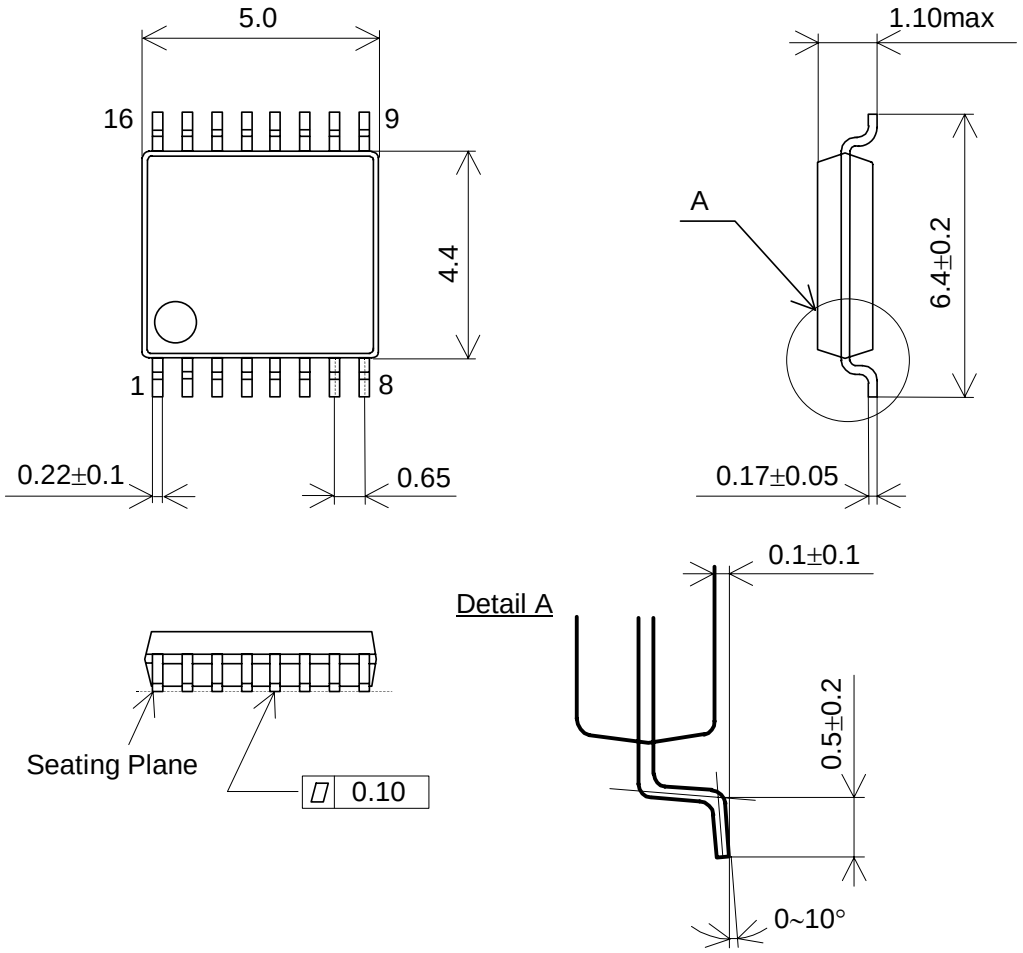
3. Analog Outputs

The analog outputs are single-ended outputs and 0.47xVDD Vpp(typ)@−4.8dBFS centered on the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFFH(@24bit) and negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit).

DC offsets on the analog outputs is eliminated by AC coupling since the analog outputs have a DC offset equal to VCOM plus a few mV.

PACKAGE

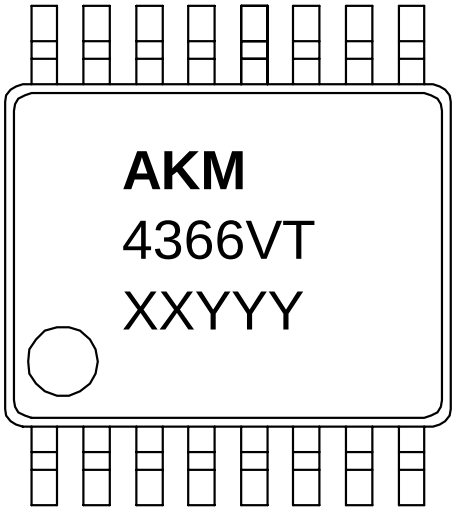
16pin TSSOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4366VT

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
03/11/28	00	First Edition		
04/03/23	01	Spec Change	6	Analog Characteristics Interchannel Gain Mismatch (max): 0.5dB → Removed.

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