

#### General Description

All-CMOS Monitor circuits in a 3-lead SOT-23 package offer the best performance in power consumption and accuracy.

The ILC5061 comes in a series of  $\pm 1\%$  accurate trip voltages to fit most microprocessor applications. Even though its output can sink 2mA, the device draws only 1 $\mu$ A in normal operation.

Additionally, a built-in hysteresis of 5% of detect voltage simplifies system design.

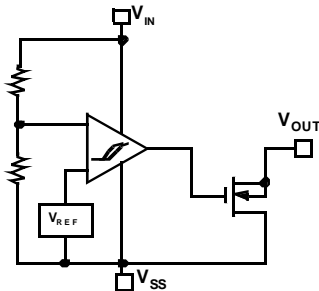
#### Features

- All-CMOS design in SOT-23 and SOT-89 package
- $\pm 1\%$  precision in Reset Detection
- Only 1 $\mu$ A of Iq
- 2mA of sink current capability
- Built-in hysteresis of 5% of detection voltage
- Voltage options of 2.6, 2.9, 3.1, 4.4, and 4.6V fit most supervisory applications

#### Applications

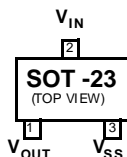
- Microprocessor reset circuits
- Memory battery back-up circuitry
- Power-on reset circuits
- Portable and battery powered electronics

#### Block Diagram



N-Channel Open Drain Output

#### Pin Package Configurations



#### Ordering Information\*

ILC5061AM-26	2.6V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-27	2.7V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-28	2.8V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-29	2.9V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-31	3.1V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-44	4.4V $\pm 1\%$ Monitor in SOT-23
ILC5061AM-46	4.6V $\pm 1\%$ Monitor in SOT-23
ILC5061M-26	2.6V $\pm 2\%$ Monitor in SOT-23
ILC5061M-27	2.7V $\pm 2\%$ Monitor in SOT-23
ILC5061M-28	2.8V $\pm 2\%$ Monitor in SOT-23
ILC5061M-29	2.9V $\pm 2\%$ Monitor in SOT-23
ILC5061M-31	3.1V $\pm 2\%$ Monitor in SOT-23
ILC5061M-44	4.4V $\pm 2\%$ Monitor in SOT-23
ILC5061M-46	4.6V $\pm 2\%$ Monitor in SOT-23

\* Standard product offering comes in tape and reel, quantity 3000 per reel orientation right

**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter		Symbol	Ratings	Units
Input Voltages		V <sub>IN</sub>	12	V
Output Current		I <sub>OUT</sub>	50	mA
Output Voltages		V <sub>OUT</sub>	V <sub>SS</sub> -0.3~+V <sub>IN</sub> +0.3	V
Continuous Total Power Dissipation	SOT-23	P <sub>d</sub>	150	mW
Operation Ambient temperature		T <sub>opr</sub>	-30~+80	°C
Storage Temperature		T <sub>stg</sub>	-40~+125	°C

**Electrical Characteristics (T<sub>A</sub>=25°C)**

Parameter	Symbol	Conditions	Min	Type	Max	Units
Detect Fail Voltage	V <sub>DF</sub>	A grade	V <sub>DF</sub> X 0.99	V <sub>DF</sub>	V <sub>DF</sub> X 1.01	V
Detect Fail Voltage	V <sub>DF</sub>	Standard grade	V <sub>DF</sub> X 0.99	V <sub>DF</sub>	V <sub>DF</sub> X 1.02	V
Hysteresis Range	V <sub>HYS</sub>		V <sub>DF</sub> X 0.02	V <sub>DF</sub> X 0.05	V <sub>DF</sub> X 0.08	V
Supply Current	I <sub>SS</sub>	V <sub>IN</sub> = 1.5V V <sub>IN</sub> = 2.0V V <sub>IN</sub> = 3.0V V <sub>IN</sub> = 4.0V V <sub>IN</sub> = 5.0V		0.9 1.0 1.3 1.6 2.0	2.6 3.0 3.4 3.8 4.2	μA
Operating Voltage	V <sub>IN</sub>	V <sub>DF</sub> = 2.1~ 6.0V	1.5		10.0	V
Output Current	I <sub>OUT</sub>	N-ch V <sub>DS</sub> = 0.5V V <sub>IN</sub> = 1.0V V <sub>IN</sub> = 2.0V V <sub>IN</sub> = 3.0V V <sub>IN</sub> = 4.0V V <sub>IN</sub> = 5.0V  P-ch V <sub>DS</sub> = 2.1V V <sub>IN</sub> = 8V		2.2 7.7 10.1 11.5 13.0  -10		mA
Temperature Characteristics	$\Delta V_{DF}/(\Delta T_{opr} \bullet V_{DF})$	30°C ≤ T <sub>opr</sub> ≤ 80°C		±100		Ppm/°C
Delay Time Release Voltage → Output Inversion)	T <sub>DLY</sub> (V <sub>DR</sub> → V <sub>OUT</sub> inversion)				0.2	ms
Note: 1. An additional resistor between the V <sub>IN</sub> pin and supply voltage may cause deterioration of the characteristics due to increasing V <sub>DR</sub> .						

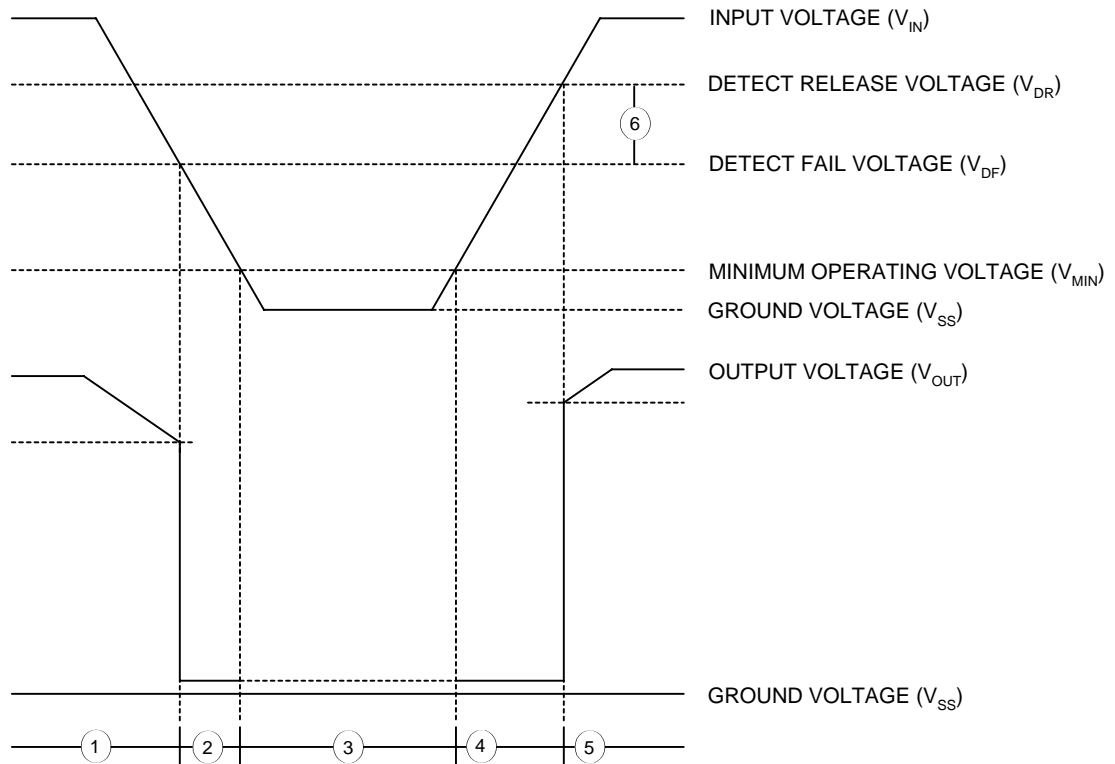
## Functional Description

The following designators 1~6 refer to the timing diagram below.

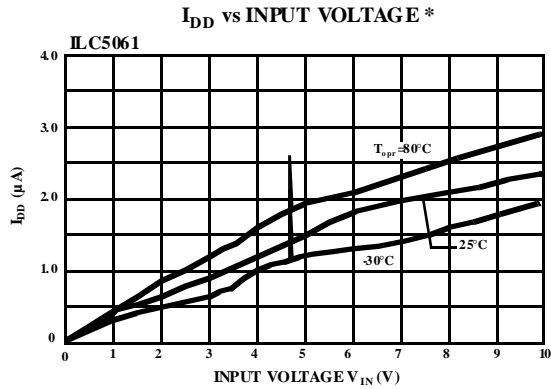
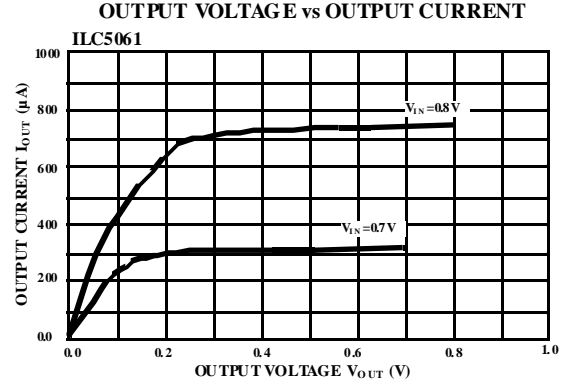
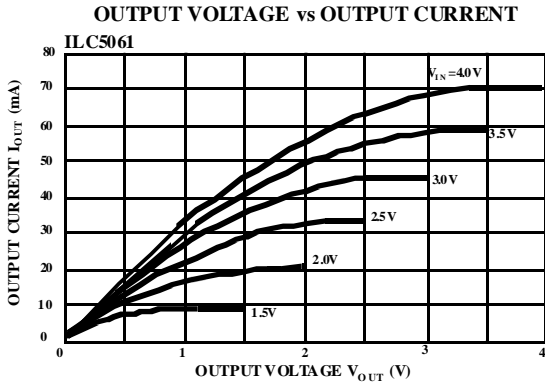
1. While the input voltage ( $V_{IN}$ ) is higher than the detect voltage ( $V_{DF}$ ), the  $V_{OUT}$  output pin is at high impedance state.
2. When the input  $V_{IN}$  voltage falls lower than  $V_{DF}$ ,  $V_{OUT}$  drops near to ground voltage
3. If the input voltage further decreases below the minimum operating voltage ( $V_{MIN}$ ), the  $V_{OUT}$  output becomes unstable. In this condition, if the  $V_{OUT}$  pin is pulled up,  $V_{OUT}$  indicates the  $V_{IN}$  voltage.

4. During an increase of the input voltage from the  $V_{SS}$  voltage,  $V_{OUT}$  is not stable in the voltage below the  $V_{MIN}$ . Exceeding that level, the output stays at the ground level ( $V_{SS}$ ) between the minimum operating voltage ( $V_{MIN}$ ) and the detect release voltage ( $V_{DR}$ ).
5. If the input voltage increases more than  $V_{DR}$ , then the  $V_{OUT}$  output pin is at high impedance state.
6. The difference between  $V_{DR}$  and  $V_{DF}$  is the hysteresis in the system.

## Timing Diagram



Typical Performance Characteristics - general conditions for all curves



\* A spike of 1/2 to 1  $\mu A$  may appear as  $V_{in}$  crosses  $V_{DR}$  or  $V_{DF}$

