

## High-Voltage Ring Generator

### Ordering Information

Operating Voltage	Package Options
$V_{NN1}$	SOW-16
-220V	HV450WG

### Features

- Integrated high voltage transistors
- 67V<sub>RMS</sub> ring signal
- Output over current protection
- Can drive external MOSFETs for larger loads

### Applications

- High voltage ring generator
- Set-top/Street box ring generator
- Pair gain ring generator

### Absolute Maximum Ratings\*

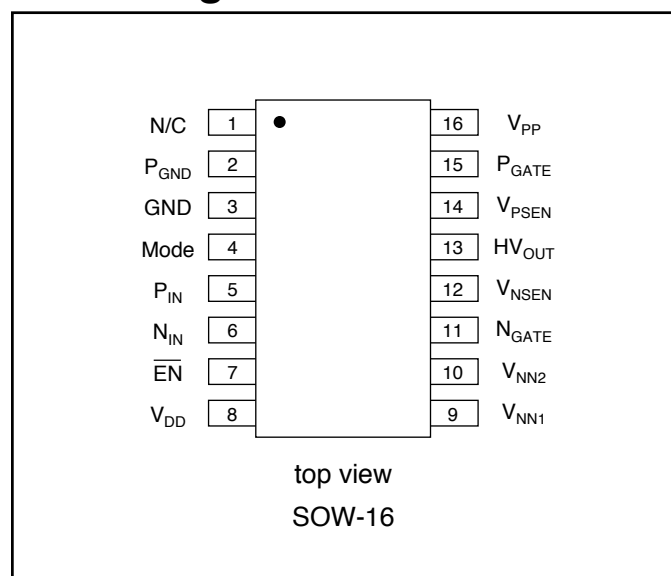
$V_{NN1}$ , power supply voltage	-240V
$V_{PP}$ , P-channel gate voltage supply	-20V
$V_{NN2}$ , N-channel gate voltage supply	$V_{NN1} + 20V$
$V_{DD}$ , logic supply	+7.5V
Storage temperature	-65°C to +150°C
Power dissipation	600mW

\* All voltages referenced to ground

### General Description

The Supertex HV450 is a PWM high voltage ring generator. The high voltage output P- and N-channel transistors are controlled independently by the logic inputs  $P_{IN}$  and  $N_{IN}$ . For application where a single control pin ( $N_{IN}$ ) is desired, the mode pin should be connected to Gnd. This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on  $N_{IN}$  will turn the high voltage P-Channel on and the N-Channel off. The outputs can drive up to 5 RENS. The HV450 can drive external MOSFETs for applications requiring larger loads. The IC can be powered down by connecting the enable pin to  $V_{DD}$ . The high voltage outputs have pulse by pulse over current protection.

### Pin Configuration



## Electrical Characteristics

(Over operating supply voltages unless otherwise specified,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
$V_{PP}$	P-channel linear regulator output voltage	-10		-18	V	
$V_{NN1}$	High voltage negative supply	- 220		-110	V	
$V_{NN2}$	Negative linear regulator output voltage	$V_{NN1} + 6.0$		$V_{NN1} + 10.0$	V	
$V_{DD}$	Logic supply voltage	4.5		5.5	V	
$I_{NN1Q}$	$V_{NN1}$ quiescent current		300	500	$\mu\text{A}$	$P_{IN} = N_{IN} = \overline{EN} = L$
				25		$P_{IN} = N_{IN} = L, \overline{EN} = H$
$I_{DDQ}$	$V_{DD1}$ quiescent current		90	200	$\mu\text{A}$	$P_{IN} = N_{IN} = \overline{EN} = L$
			35	100		$P_{IN} = N_{IN} = L, \overline{EN} = H$
$I_{NN1}$	$V_{NN1}$ operating current		1.4		mA	No load, $V_{OUTP}$ and $V_{OUTN}$ switching at 100KHz
$I_{DD}$	$V_{DD}$ operating current			1.0	mA	
$I_{IL}$	Mode logic input low current		25		$\mu\text{A}$	Mode = 0V
$V_{IL}$	Logic input low voltage	0		1.0	V	$V_{DD} = 5.0\text{V}$
$V_{IH}$	Logic input high voltage	4.0		5.0	V	$V_{DD} = 5.0\text{V}$

## High Voltage Output

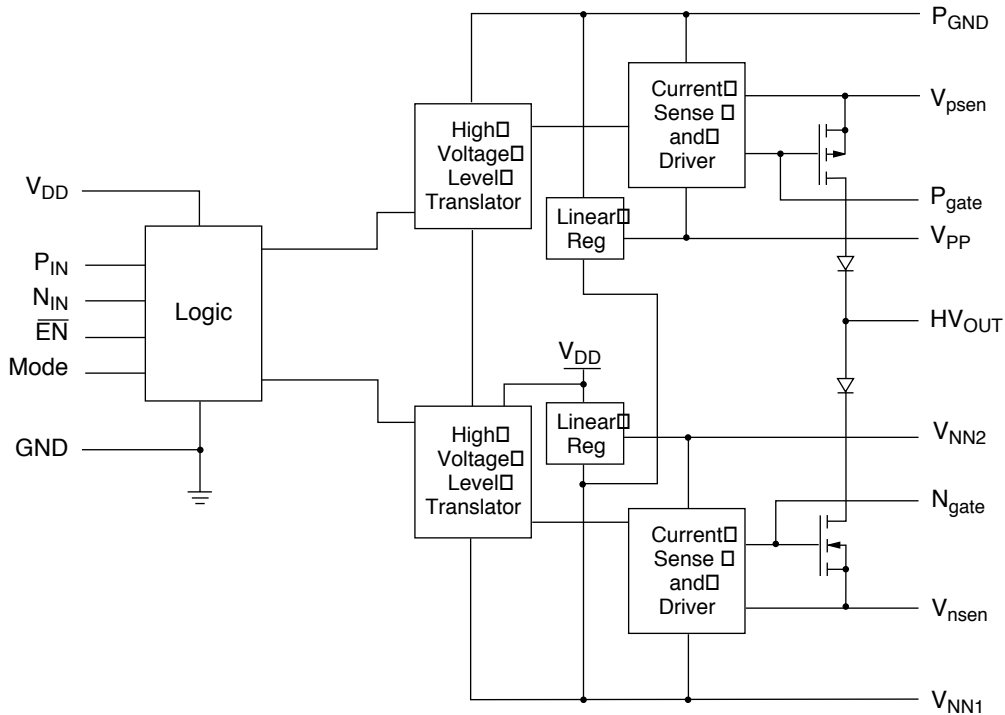
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
$R_{SOURCE}$	$V_{OUTP}$ source resistance		65		$\Omega$	$I_{OUT} = 100\text{mA}$
$R_{SINK}$	$V_{OUTP}$ sink resistance		65		$\Omega$	$I_{OUT} = -100\text{mA}$
$t_{d(ON)}$	$HV_{OUT}$ delay time		150		ns	$P_{IN} = \text{high to low}$ , Mode = high
$t_{rise}$	$HV_{OUT}$ rise time		50		ns	$P_{IN} = \text{high to low}$
$t_{d(OFF)}$	$HV_{OUT}$ delay time		200		ns	$N_{IN} = \text{low to high}$ , Mode = high
$t_{fall}$	$HV_{OUT}$ fall time		50		ns	$N_{IN} = \text{low to high}$
$t_{db}$	Logic deadband time		250		ns	Mode = low
$V_{psen}$	$HV_{OUT}$ current source sense voltage	-1.2		-0.8	V	
$V_{nsen}$	$HV_{OUT}$ current sink sense voltage	$V_{NN1} + 0.8$		$V_{NN1} + 1.2$	V	
$t_{shortP}$	$HV_{OUT}$ off delay time when current source sense is activated		70	150	ns	
$t_{shortN}$	$HV_{OUT}$ off delay time when current sink sense is activated		70	150	ns	
$t_{whout}$	Minimum pulse width for $HV_{OUT}$ at $P_{GND}$			500	ns	
$t_{wlout}$	Minimum pulse width for $HV_{OUT}$ at $V_{NN1}$			500	ns	

## Truth Table

$N_{IN}$	$P_{IN}$	Mode	$\overline{EN}$	$HV_{OUT}$
L	L	H	L	Pgnd
L	H	H	L	High Z
H*	L*	H	L	*
H	H	H	L	$V_{NN1}$
L	X	L	L	$V_{NN1}$
H	X	L	L	Pgnd
X	X	X	H	High Z

\*This state will short  $V_{NN1}$  to Pgnd and should therefore be avoided.

## Block Diagram



## Pin Description

$V_{PP}$	P-channel gate voltage supply. Generated by an internal linear regulator. A 0.1 $\mu$ F capacitor should be connected between $P_{GND}$ and $V_{PP}$ .
$V_{NN1}$	Negative high voltage supply.
$V_{NN2}$	N-channel gate voltage supply. Generated by an internal linear regulator. A 0.1 $\mu$ F capacitor should be connected between $V_{NN2}$ and $V_{NN1}$ .
$V_{DD}$	Logic supply voltage.
GND	Low voltage ground.
$P_{GND}$	High voltage power ground.
$P_{IN}$	Logic control input. When mode is high, logic input high turns OFF output high voltage P-Channel.
$N_{IN}$	Logic control input. When mode is high, logic input high turns ON output high voltage N-Channel.
$\overline{EN}$	Logic enable input. Logic low enables IC.
Mode	Logic mode input. Logic low activates 200nsec deadband. When mode is low, $N_{IN}$ turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to $V_{DD}$ or ground.
$HV_{OUT}$	High voltage output. Voltage swings from $P_{GND}$ to $V_{NN1}$ .
$V_{psen}$	Pulse by pulse over current sensing for P-Channel MOSFET.
$V_{nsen}$	Pulse by pulse over current sensing for N-Channel MOSFET.
$P_{gate}$	Gate drive for external P-channel MOSFET.
$N_{gate}$	Gate drive for external N-channel MOSFET.

# Typical Application Circuit

