512Mb G-die DDR SDRAM Specification

60 FBGA
with Lead-Free & Halogen-Free
(RoHS compliant)

Table of Contents

Revision History

Revision	Month	Year	History
1.0	October	2009	- Initial Release

1.0 Key Features

- V_{DD} : 2.5V ± 0.2V, V_{DDQ} : 2.5V ± 0.2V for DDR333
- V_{DD} : 2.6V ± 0.1V, V_{DDQ} : 2.6V ± 0.1V for DDR400
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQS] (x4,x8) & [L(U)DQS] (x16)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
  - -. Read latency : DDR333(2.5 Clock), DDR400(3 Clock)
  - -. Burst length (2, 4, 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe
- Edge aligned data output, center aligned data input
- LDM,UDM for write masking only (x16)
- DM for write masking only (x4, x8)
- Auto & Self refresh
- 7.8us refresh interval(8K/64ms refresh)
- Maximum burst refresh cycle : 8
- 60Ball FBGA **Lead-Free & Halogen-Free** package
- **RoHS compliant**

2.0 Ordering Information

Part No.	Org.	Max Freq.	Interface	Package
K4H510438G-HC/LCC	128M x 4	CC(DDR400@CL=3)	SSTL2	60ball FBGA Lead-Free & Halogen-Free
K4H510438G-HC/LB3		B3(DDR333@CL=2.5)		
K4H510838G-HC/LCC	64M x 8	CC(DDR400@CL=3)	SSTL2	60ball FBGA Lead-Free & Halogen-Free
K4H510838G-HC/LB3		B3(DDR333@CL=2.5)		
K4H511638G-HC/LCC	32M x 16	CC(DDR400@CL=3)	SSTL2	60ball FBGA Lead-Free & Halogen-Free
K4H511638G-HC/LB3		B3(DDR333@CL=2.5)		

3.0 Operating Frequencies

	CC(DDR400@CL=3)	B3(DDR333@CL=2.5)
Speed @CL2	-	133MHz
Speed @CL2.5	166MHz	166MHz
Speed @CL3	200MHz	-
CL-tRCD-tRP	3-3-3	2.5-3-3

4.0 Ball Description (Top View)

128M x 4

9	V_{DDQ}	NC	NC	NC	NC	NC						
8	NC	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{DD}	$\overline{CAS}$	$\overline{CS}$	BA0	A10/AP	A1	A3
7	V_{DD}	DQ0	NC	DQ1	NC	NC	$\overline{WE}$	$\overline{RAS}$	BA1	A0	A2	V_{DD}
	A	B	C	D	E	F	G	H	J	K	L	M
3	V_{SS}	DQ3	NC	DQ2	DQS	DM	$\overline{CK}$	CKE	A9	A7	A5	V_{SS}
2	NC	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{SS}	CK	A12	A11	A8	A6	A4
1	V_{SSQ}	NC	NC	NC	NC	V_{REF}						

64M x 8

9	V_{DDQ}	NC	NC	NC	NC	NC						
8	DQ0	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{DD}	$\overline{CAS}$	$\overline{CS}$	BA0	A10/AP	A1	A3
7	V_{DD}	DQ1	DQ2	DQ3	NC	NC	$\overline{WE}$	$\overline{RAS}$	BA1	A0	A2	V_{DD}
	A	B	C	D	E	F	G	H	J	K	L	M
3	V_{SS}	DQ6	DQ5	DQ4	DQS	DM	$\overline{CK}$	CKE	A9	A7	A5	V_{SS}
2	DQ7	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{SS}	CK	A12	A11	A8	A6	A4
1	V_{SSQ}	NC	NC	NC	NC	V_{REF}						

32M x 16

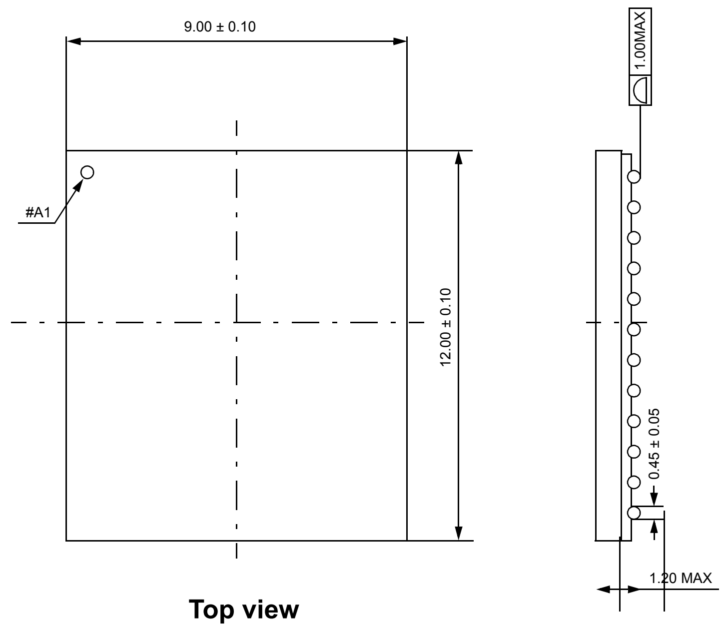
9	V_{DDQ}	DQ1	DQ3	DQ5	DQ7	NC						
8	DQ0	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{DD}	$\overline{CAS}$	$\overline{CS}$	BA0	A10/AP	A1	A3
7	V_{DD}	DQ2	DQ4	DQ6	LDQS	LDM	$\overline{WE}$	$\overline{RAS}$	BA1	A0	A2	V_{DD}
	A	B	C	D	E	F	G	H	J	K	L	M
3	V_{SS}	DQ13	DQ11	DQ9	UDQS	UDM	$\overline{CK}$	CKE	A9	A7	A5	V_{SS}
2	DQ15	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{SSQ}	V_{SS}	CK	A12	A11	A8	A6	A4
1	V_{SSQ}	DQ14	DQ12	DQ10	DQ8	V_{REF}						

Organization	Row Address	Column Address
128Mx4	A0~A12	A0-A9, A11, A12
64Mx8	A0~A12	A0-A9, A11
32Mx16	A0~A12	A0-A9

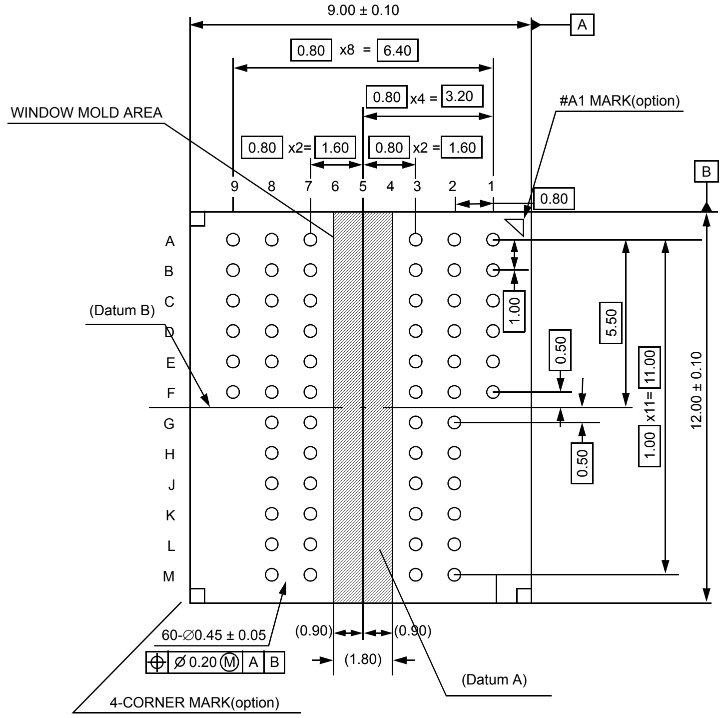
DM is internally loaded to match DQ and DQS identically.

Row & Column address configuration

5.0 Package Physical Dimension



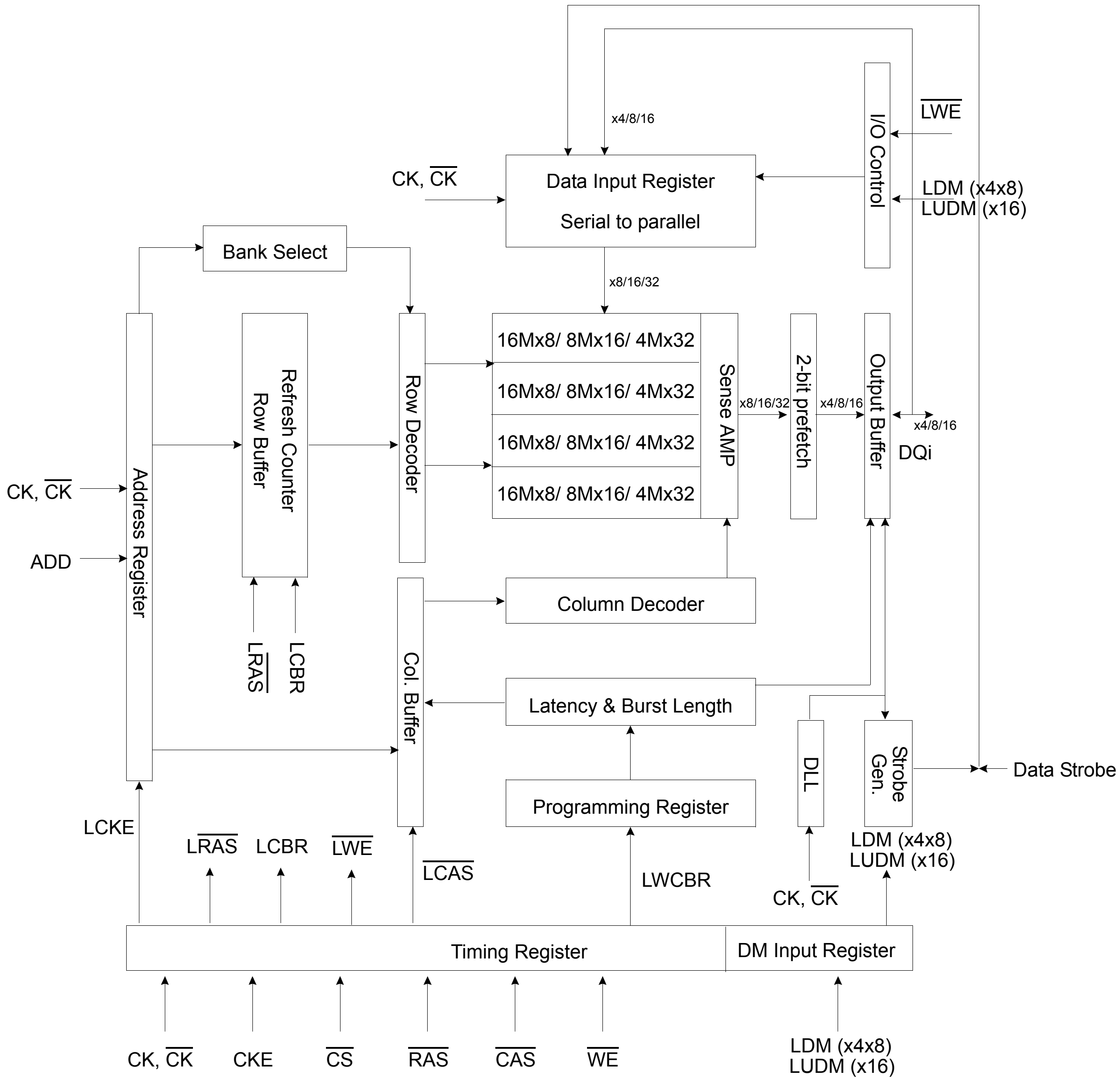
Top view



Bottom view

60Ball FBGA 512Mb Package Dimension

6.0 Block Diagram (32Mb x 4 / 16Mb x 8 / 8Mb x 16 I/O x4 Banks)



7.0 Input/Output Function Description

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE Low provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughput READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS Low level after V_{DD} is applied upon 1st power up, After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH entry and exit, V_{REF} must be maintained to this input.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
LDM,(UDM)	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0~D7 ; UDM corresponds to the data on DQ8~DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Addres Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [0 : 12]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Data Input/Output : Data bus
LDQS,(U)DQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0~D7 ; UDQS corresponds to the data on DQ8~DQ15. LDQS is NC on x4 and x8.
NC	-	No Connect : No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply : +2.5V ± 0.2V. (+2.6V ±0.1V for DDR400)
V_{SSQ}	Supply	DQ Ground.
V_{DD}	Supply	Power Supply : +2.5V ± 0.2V. (+2.6V ±0.1V for DDR400)
V_{SS}	Supply	Ground.
V_{REF}	Input	SSTL_2 reference voltage.

8.0 Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9, A11 ~ A12	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM(UDM/LDM for x16 only)			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note :
1. OP Code : Operand Code. A_0 ~ A_{12}& BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM(x4/8) sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
   UDM/LDM(x16 only) sampled at the rising and falling edges of the UDQS/LDQS and Data-in are masked at the both edges (Write UDM/LDM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

32M x 4Bit x 4 Banks / 16M x 8Bit x 4 Banks / 8M x 16Bit x 4 Banks Double Data Rate SDRAM

9.0 General Description

The K4H510438G / K4H510838G / K4H511638G is 536,870,912 bits of double data rate synchronous DRAM organized as 4x 33,554,432 / 4x 16,777,216 / 4x 8,388,608 words by 4/8/16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 400Mb/s per pin. I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

10.0 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

11.0 DC Operating Conditions

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 2.5V for DDR266/333)	V_{DD}	2.3	2.7	V	
Supply voltage(for device with a nominal VDD of 2.6V for DDR400)	V_{DD}	2.5	2.7	V	
I/O Supply voltage(for device with a nominal VDD of 2.5V for DDR266/333)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage(for device with a nominal VDD of 2.5V for DDR400)	V_{DDQ}	2.5	2.7	V	
I/O Reference voltage	V_{REF}	0.49*V_{DDQ}	0.51*V_{DDQ}	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.36	V_{DDQ}+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	V_I(Ratio)	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Note :
1. V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on V_{REF} may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

12.0 DDR SDRAM IDD Spec Items & Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; tCK=6ns for DDR333, 5ns for DDR400; DQ,DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	**IDD0**
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	**IDD1**
Precharge power-down standby current; All banks idle; power - down mode; CKE = <V_{IL}(max); tCK=6ns for DDR333, 5ns for DDR400; V_{IN} = V_{REF} for DQ,DQS and DM.	**IDD2P**
Precharge Floating standby current; $\overline{CS}$ > =V_{IH}(min);All banks idle; CKE > = V_{IH}(min); tCK=6ns for DDR333, 5ns for DDR400; Address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ,DQS and DM	**IDD2F**
Precharge Quiet standby current; $\overline{CS}$ > = V_{IH}(min); All banks idle; CKE > = V_{IH}(min); tCK=6ns for DDR333, 5ns for DDR400; Address and other control inputs stable at >= V_{IH}(min) or =<V_{IL}(max); Vin = V_{REF} for DQ ,DQS and DM	**IDD2Q**
Active power - down standby current ; one bank active; power-down mode; CKE=< V_{IL} (max); tCK=6ns for DDR333, 5ns for DDR400; V_{IN} = V_{REF} for DQ,DQS and DM	**IDD3P**
Active standby current; $\overline{CS}$ >= V_{IH}(min); CKE>=V_{IH}(min); one bank active; active - precharge; tRC=tRASmax; tCK=6ns for DDR333, 5ns for DDR400; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	**IDD3N**
Operating current - burst read; Burst length = 2; reads; continuous burst; One bank active; address and control inputs changing once per clock cycle; CL=2.5 at CK=6ns for DDR333, CL=3 at tCK=5ns for DDR400; 50% of data changing on every transfer; Iout = 0 m A	**IDD4R**
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2.5 at tCK=6ns for DDR333, 5ns for DDR400; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	**IDD4W**
Auto refresh current; tRC = tRFC(min) which is 12*tCK for DDR333 at tCK=6ns, 14*tCK for DDR400 at tCK=5ns; distributed refresh	**IDD5**
Self refresh current; CKE =< 0.2V; External clock on; tCK=6ns for DDR333, 5ns for DDR400.	**IDD6**
Operating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	**IDD7A**

13.0 Input/Output Capacitance

(T_A= 25°C, f=100MHz)

Parameter	Symbol	Min	Max	DeltaCap(max)	Unit	Note
Input capacitance (A0 ~ A12, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN1}	1.5	2.5	0.5	pF	4
Input capacitance(CK, $\overline{CK}$)	C_{IN2}	1.5	2.5	0.25	pF	4
Data & DQS input/output capacitance	C_{OUT}	3.5	4.5	0.5	pF	1,2,3,4
Input capacitance(DM for x4/8, UDM/LDM for x16)	C_{IN3}	3.5	4.5		pF	1,2,3,4

Note :
1. These values are guaranteed by design and are tested on a sample basis only.
2. Although DM is an input -only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
3. Unused pins are tied to ground.
4. This parameteer is sampled. For DDR333 V_{DDQ} = +2.5V +0.2V, V_{DD} = +3.3V +0.3V or +0.25V+0.2V. For DDR400, V_{DDQ} = +2.6V +0.1V, V_{DD} = +2.6V +0.1V. For all devices, f=100MHz, tA=25°C, Vout(dc) = V_{DDQ}/2, Vout(peak to peak) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

14.0 Detailed Test Condition for DDR SDRAM IDD1 & IDD7A

IDD1 : Operating current: One bank operation

1. Typical Case: For DDR333: V_{DD} = 2.5V, T=25°C; For DDR400: V_{DD}=2.6V,T=25°C
   Worst Case : V_{DD} = 2.7V, T= 10°C

2. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

3. Timing patterns

- B3(166Mhz, CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRCD=3*tCK, tRC = 10*tCK, tRAS=7*tCK
  Read : A0 N N R0 N N P0 N N A0 N - repeat the same timing with random address changing
  *50% of data changing at every burst

- CC(200Mhz,CL = 3) : tCK = 5ns, CL = 3, BL = 4, tRCD = 3*tCK , tRC = 11*tCK, tRAS = 8*tCK
  Read : A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing
  *50% of data changing at every transfer

IDD7A : Operating current: Four bank operation

1. Typical Case: For DDR333: V_{DD} = 2.5V, T=25°C; For DDR400: V_{DD}=2.6V,T=25°C
   Worst Case : V_{DD} = 2.7V, T= 10°C

2. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA

4. Timing patterns

- B3(166Mhz,CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK, Read with autoprecharge
  Read : A0 N A1 R0 A2 R1 A3 R2 N R3 N A0 N A1 R0 - repeat the same timing with random address changing
  *50% of data changing at every burst

- CC(200Mhz,CL = 3) : tCK = 5ns, CL = 3, BL = 4, tRCD = 3*tCK , tRC = 11*tCK, tRAS = 8*tCK
  Read : A0 N A1 R0 A2 R1 A3 R2 N R3 N A0 N A1 R0 - repeat the same timing with random address changing
  *50% of data changing at every transfer

  Legend : A=Activate, R=Read, W=Write, P=Precharge, N=DESELECT

15.0 DDR SDRAM IDD Spec Table

(V_{DD}=2.7V, T = 10°C)

Symbol		128Mx4 (K4H510438G)		Unit	Notes
		CC(DDR400@CL=3)	B3(DDR333@CL=2.5)		
IDD0		70	65	mA	
IDD1		80	75	mA	
IDD2P		5	5	mA	
IDD2F		23	23	mA	
IDD2Q		20	20	mA	
IDD3P		20	15	mA	
IDD3N		40	35	mA	
IDD4R		90	80	mA	
IDD4W		100	95	mA	
IDD5		120	110	mA	
IDD6	Normal	5	5	mA	
	Low power	3	3	mA	
IDD7A		220	210	mA	

Symbol		64Mx8 (K4H510838G)		Unit	Notes
		CC(DDR400@CL=3)	B3(DDR333@CL=2.5)		
IDD0		75	65	mA	
IDD1		90	80	mA	
IDD2P		5	5	mA	
IDD2F		23	23	mA	
IDD2Q		20	20	mA	
IDD3P		20	15	mA	
IDD3N		40	40	mA	
IDD4R		110	95	mA	
IDD4W		110	100	mA	
IDD5		130	110	mA	
IDD6	Normal	5	5	mA	
	Low power	3	3	mA	
IDD7A		240	220	mA	

Symbol		32Mx16 (K4H511638G)		Unit	Notes
		CC(DDR400@CL=3)	B3(DDR333@CL=2.5)		
IDD0		80	70	mA	
IDD1		100	90	mA	
IDD2P		5	5	mA	
IDD2F		23	23	mA	
IDD2Q		20	20	mA	
IDD3P		20	15	mA	
IDD3N		45	40	mA	
IDD4R		140	120	mA	
IDD4W		135	120	mA	
IDD5		135	115	mA	
IDD6	Normal	5	5	mA	
	Low power	3	3	mA	
IDD7A		255	230	mA	

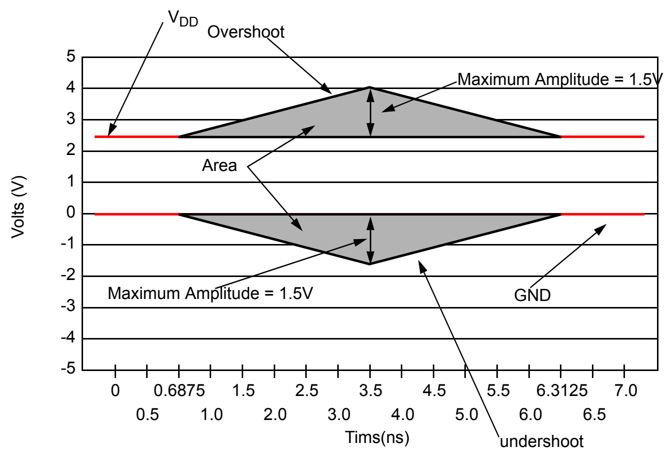
16.0 AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH}(AC)	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V_{IL}(AC)		V_{REF} - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(AC)	0.7	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX}(AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	2

Note :
1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

17.0 AC Overshoot/Undershoot Specification for Address and Control Pins

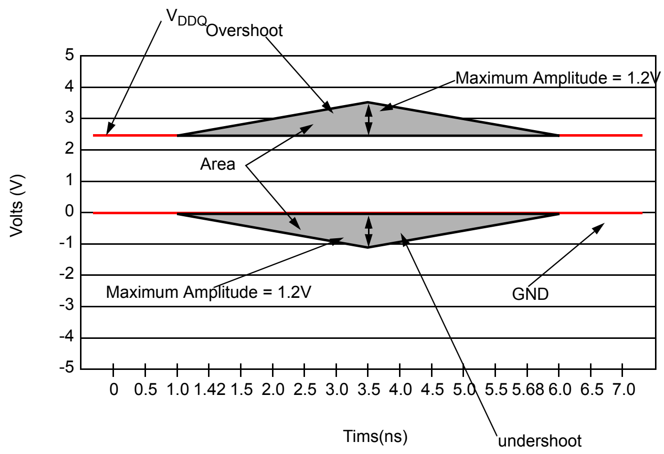
Parameter	Specification	
	DDR400	DDR333
Maximum peak amplitude allowed for overshoot	1.5 V	1.5 V
Maximum peak amplitude allowed for undershoot	1.5 V	1.5 V
The area between the overshoot signal and V_{DD} must be less than or equal to	4.5 V-ns	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5 V-ns	4.5 V-ns



AC overshoot/Undershoot Definition

18.0 Overshoot/Undershoot Specification for Data, Strobe and Mask Pins

Parameter	Specification	
	DDR400	DDR333
Maximum peak amplitude allowed for overshoot	1.2 V	1.2 V
Maximum peak amplitude allowed for undershoot	1.2 V	1.2 V
The area between the overshoot signal and V_{DD} must be less than or equal to	2.4 V-ns	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to	2.4 V-ns	2.4 V-ns



DQ/DM/DQS AC overshoot/Undershoot Definition

19.0 AC Timming Parameters & Specifications

Parameter		Symbol	CC (DDR400@CL=3.0)		B3 (DDR333@CL=2.5)		Unit	Note
			Min	Max	Min	Max		
Row cycle time		tRC	55		60		ns	
Refresh row cycle time		tRFC	70		72		ns	
Row active time		tRAS	40	70K	42	70K	ns	
RAS to CAS delay		tRCD	15		18		ns	
Row precharge time		tRP	15		18		ns	
Row active to Row active delay		tRRD	10		12		ns	
Write recovery time		tWR	15		15		ns	
Last data in to Read command		tWTR	2		1		tCK	
Clock cycle time	CL=2.0	tCK	-	-	7.5	12	ns	
	CL=2.5		6	12	6	12		
	CL=3.0		5	10	-	-		
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/CK		tDQSCK	-0.55	+0.55	-0.6	+0.6	ns	
Output data access time from CK/CK		tAC	-0.65	+0.65	-0.7	+0.7	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.4	-	0.4	ns	22
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.72	1.28	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		ns	13
DQS-in hold time		tWPRE	0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		tCK	
Address and Control Input setup time(fast)		tIS	0.6		0.75		ns	15, 17~19
Address and Control Input hold time(fast)		tIH	0.6		0.75		ns	15, 17~19
Address and Control Input setup time(slow)		tIS	0.7		0.8		ns	16~19
Address and Control Input hold time(slow)		tIH	0.7		0.8		ns	16~19
Data-out high impedence time from CK/CK		tHZ	-0.65	+0.65	-0.7	+0.7	ns	11
Data-out low impedence time from CK/CK		tLZ	-0.65	+0.65	-0.7	+0.7	ns	11
Mode register set cycle time		tMRD	10		12		ns	
DQ & DM setup time to DQS		tDS	0.4		0.45		ns	j, k
DQ & DM hold time to DQS		tDH	0.4		0.45		ns	j, k
Control & Address input pulse width		tIPW	2.2		2.2		ns	18
DQ & DM input pulse width		tDIPW	1.75		1.75		ns	18
Exit self refresh to non-Read command		tXSNR	75		75		ns	
Exit self refresh to read command		tXSRD	200		200		tCK	
Refresh interval time		tREFI		7.8		7.8	us	14
Output DQS valid window		tQH	tHP -tQHS	-	tHP -tQHS	-	ns	21
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	20, 21
Data hold skew factor		tQHS		0.5		0.5	ns	21
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	tCK	12
Active to Read with Auto precharge command		tRAP	15		18			
Autoprecharge write recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	23
Power Down Exit Time		tPDEX	1		1		tCK	

20.0 System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333 and DDR400 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR400		DDR333			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Units	Notes
DQ/DM/DQS input slew rate measured between V_{IH}(DC), V_{IL}(DC) and V_{IL}(DC), V_{IH}(DC)	DCSLEW	0.5	4.0	0.5	4.0	V/ns	a, l

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtIS	ΔtIH	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtDS	ΔtDH	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	ΔtDS	ΔtDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristice (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristice (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR400		DDR333		
PARAMETER	MIN	MAX	MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)	0.67	1.5	0.67	1.5	e, l

21.0 Component Notes

1. All voltages referenced to V_{SS}.

2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

3. Figure 1 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

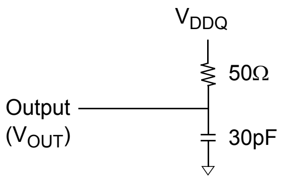


Figure 1 : Timing Reference Load

4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.

6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE $\leq 0.2V_{DDQ}$ is recognized as LOW.

7. Enables on.chip refresh and address counters.

8. IDD specifications are tested after the device is properly initialized.

9. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.

10. The output timing reference voltage level is V_{TT}.

11. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).

12. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.

13. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previ ously in progress on the bus, DQS will be transitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

14. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

15. For command/address input slew rate $\geq$ 1.0 V/ns

16. For command/address input slew rate $\geq$ 0.5 V/ns and $<$ 1.0 V/ns

Component Notes

17. For CK & $\overline{CK}$ slew rate ≥ 1.0 V/ns

18. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

19. Slew Rate is measured between V_{OH}(AC) and V_{OL}(AC).

20. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

21. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

22. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

23. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR400 at CL=3 and tCK=5ns tDAL = (15 ns / 5 ns) + (15 ns/ 5ns) = (3) + (3)
tDAL = 6 clocks

22.0 System Notes

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 2.

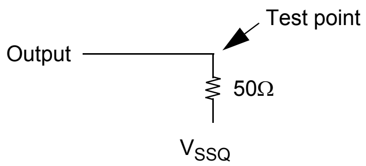


Figure 2 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 3.

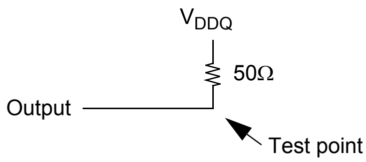


Figure 3 : Pulldown slew rate test load

c. Pullup slew rate is measured between (V_{DDQ}/2 - 320 mV +/- 250 mV)
Pulldown slew rate is measured between (V_{DDQ}/2 + 320 mV +/- 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
Example : For typical slew rate, DQ0 is switching
For minmum slew rate, all DQ bits are switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical : 25 °C (T Ambient), V_{DDQ} = 2.5V(for DDR333) and 2.6V(for DDR400), typical process
Minimum : 70 °C (T Ambient), V_{DDQ} = 2.3V(for DDR333) and 2.5V(for DDR400), slow - slow process
Maximum : 0 °C (T Ambient), V_{DDQ} = 2.7V(for DDR333) and 2.7V(for DDR400), fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package divices only.

h. Only intended for operation up to 400 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates detemined by either V_{IH}(AC) to V_{IL}(AC) or V_{IH}(DC) to V_{IL}(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either V_{IH}(AC) to V_{IL}(AC) or V_{IH}(DC) to V_{IL}(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)} - {1/(Slew Rate2)}

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC - AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either V_{IH}(AC) to V_{IL}(AC) or V_{IH}(DC) to V_{IL}(DC), and similarly for rising transitions.

l. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotonic.

23.0 IBIS : I/V Characteristics for Input and Output Buffers

DDR SDRAM Output Driver V-I Characteristics

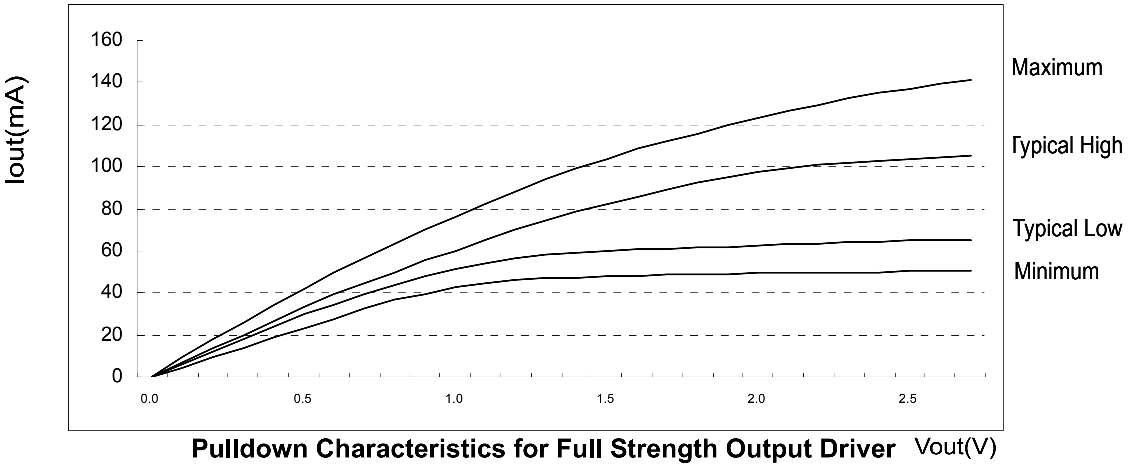
DDR SDRAM Output driver characteristics are defined for full and half strength operation as selected by the EMRS bit A1.

Figures 4 and 5 show the driver characteristics graphically, and tables 8 and 9 show the same data in tabular format suitable for input into simulation tools. The driver characteristcs evaluation conditions are:

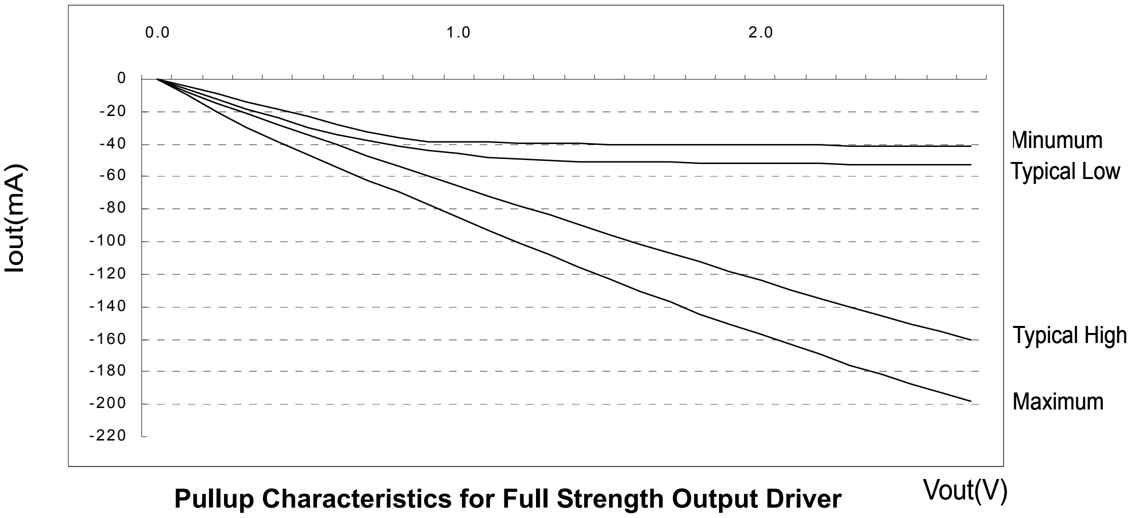
Typical	25×C	V_{DD}/V_{DDQ} = 2.5V, typical process
Minimum	70×C	V_{DD}/V_{DDQ} = 2.3V, slow-slow process
Maximum	0×C	V_{DD}/V_{DDQ} = 2.7V, fast-fast process

Output Driver Characteristic Curves Notes:

1. The full variation in driver current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figures 4 and 5.
2. It is recommended that the "typical" IBIS V-I curve lie within the inner bounding lines of the V-I curves of Figures 4 and 5.
3. The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be unity +/- 10%, for device drain to source voltages from 0.1 to1.0. This specification is a design objective only. It is not guaranteed.



Pulldown Characteristics for Full Strength Output Driver

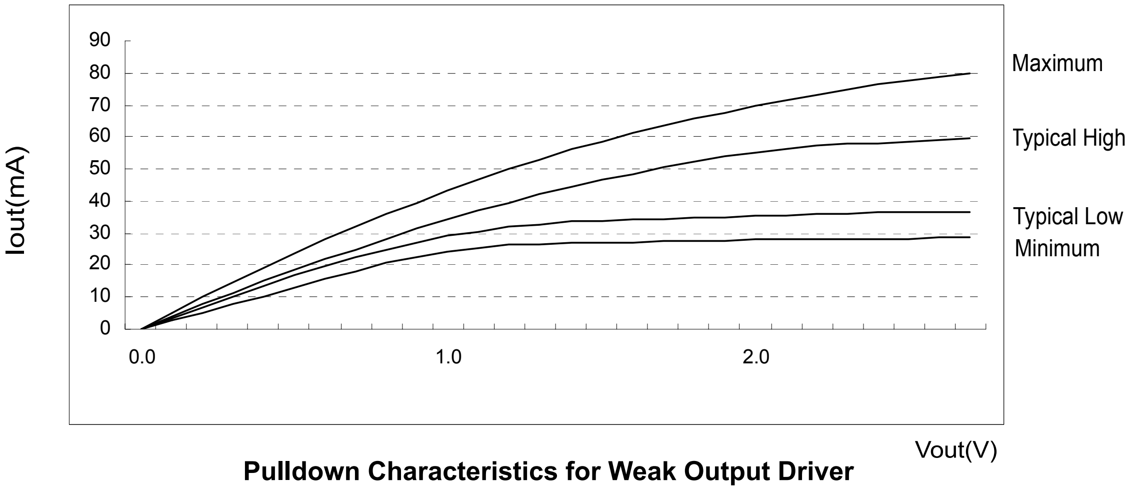


Pullup Characteristics for Full Strength Output Driver

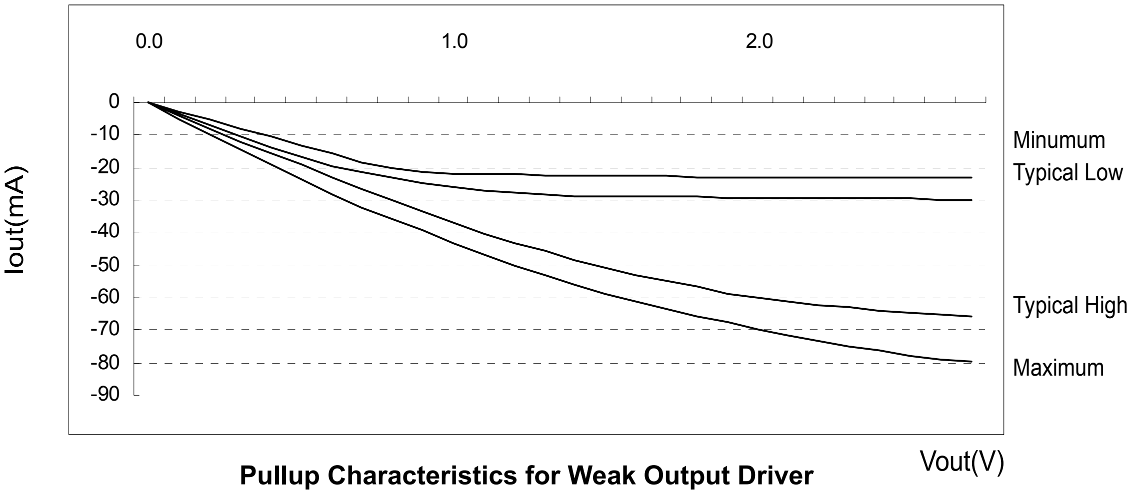
Figure 4. I/V characteristics for input/output buffers:Pulldown(above) and pullup(below)

	Pulldown Current (mA)				pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-41.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Table 8. Full Strength Driver Characteristics



Pulldown Characteristics for Weak Output Driver



Pullup Characteristics for Weak Output Driver

Figure 5. I/V characteristics for input/output buffers:Pulldown(above) and pullup(below)

	Pulldown Current (mA)				pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

Table 9. Weak Driver Characteristics