

Quartz Controlled Pulse Generator

Description

The monolithic integrated bipolar circuit, U2391B, is designed as a quartz controlled pulse generator. The tristate input enables the selection of different pulse period durations. The internal switch-on monitoring

achieves the start up of the IC when the power-on occurs. The output pulse can supply a drive signal upto 150 mA, which is short circuit protected.

Features

- Standard quartz $f_{osc} = 32.768 \text{ kHz}$
- Minimum operating voltage $4.5 \text{ V}/1.5 \text{ mA}$
- Pulse width, $t_p = 31.25 \text{ ms}$
- Power stage with current limitation: typical 150 mA
- Tristate period selection: $1/36/60 \text{ s}$
- Reset and disable possibility
- Operation with $C \geq 33 \text{ pF}$, as operational time counter possible
- Minimum dimensions due to SO-case

Application

Operational time counter

Case: SO8

Block Diagram

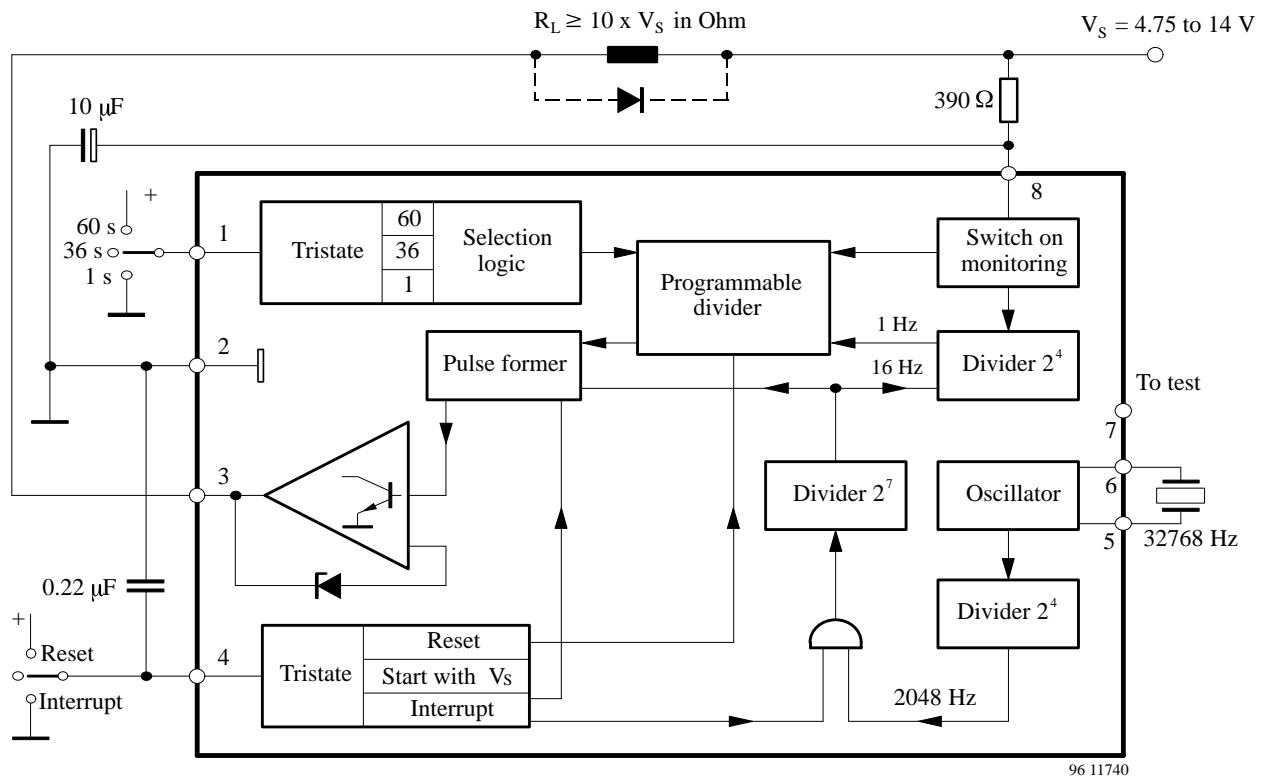


Figure 1. Block diagram with external circuit

Pin Description

Pin	Symbol	Function
1	Period	Period selection input
2	GND	Ground
3	Output	Output control pulse
4	Contr.	Control input
5, 6	Osc.	Quartz-oscillator input
7	Test	Test logic input/output
8	V _S	Supply voltage

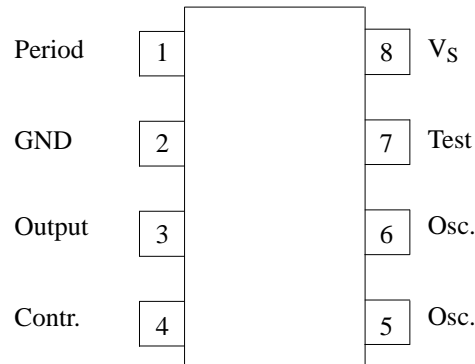


Figure 2. Pinning

Description

Pin 1, Period Selection Logic

Period selection at Pin 1 is as follows:

Pin 1 = open, $\tau = 36$ s

Pin 1 = ground $\tau = 1$ s

Pin 1 = V_S (Pin 8), $\tau = 60$ s

Pin 2, Ground

Pin 3, Output Stage

Output stage, being short circuit protected is limited to a current value of typical 150 mA. Apart from it, there is a voltage limitation which controls the power stage at the rate of $V_3 \geq 28.8$ to 32 V and serves as an active Z-diode. Output pulse width is 31.25 ms when quartz frequency is 32.768 kHz. It is independent of the selected period.

Pin 4, Control Logic

- Counting delay is typ 1.5 s (maximum 8 s) when Pin 4 is open and V_S is switched on.
- Programmable residual divider $\tau \geq 1$ s is reseeded if Pin 4 is connected to Pin 8. This results in an absolute tolerance, at the start across "Reset/End" to be ≤ 1 s.
- Clock input to the 2^7 divider is inhibited, if Pin 4 is connected to the ground (Pin 2). Absolute tolerance for every interruption is ≤ 0.488 ms.

- An interruption is ignored (Pin 4 = \perp) during the output pulse time.
- When Pin 4 is switched to V_S during the output pulse time – this output pulse will be reseeded.

Pin 5, 6 Quartz-Oscillator Input

The propagated period time selection is based on circuit with a low cost clock quartz of 32.768 kHz.

Pin 7, Test Logic, Figure 2, 3

To test the circuit in a reasonable time, it is possible to control the divider ($f_o = 16$ Hz) at Pin 7 as well as to feed in a higher frequency to the programmed residual counter ($f_i \leq 2$ kHz).

Pin 8, Supply Voltage

An operating voltage of 4.5 V is necessary for the functioning of the circuit, although an internal switch-on monitoring allows it to operate with a voltage of 3.6 V. This means that there is sufficient reliability for the performance of the circuit.

The circuit is designed for 12 V $\pm 10\%$ with internal supply voltage limitation of typical 15 V. In case of higher voltages there is a need of a series resistance and buffer capacitance as shown in figure 1.

Absolute Maximum Ratings

Reference point Pin 2, unless otherwise specified

Parameters	Symbol	Value	Unit
Supply current $t \leq 10 \mu\text{s}$	Pin 8 I_S i_s	30 150	mA
Supply voltage without series resistance	Pin 8 V_S	13.2	V
Voltages			
Selection logic	Pin 1 V_1	0 to V_S	V
Control logic	Pin 4 V_4	0 to V_S	V
Output stage, without protection circuit	Pin 3 V_3	28.8	V
Currents			
Test logic	Pin 7 I_7	± 100	μA
Oscillator	Pin 5, 6 I_{osc}	± 100	μA
Output stage $t \leq 1 \text{ ms}$	Pin 3 I_3	300	mA
Power dissipation			
$T_{amb} = 45^\circ\text{C}$ $T_{amb} = 85^\circ\text{C}$	P_{tot}	270 135	mW
Storage temperature range	T_{stg}	-40 to +125	$^\circ\text{C}$
Ambient temperature range	T_{amb}	-20 to +100	$^\circ\text{C}$
Junction temperature	T_j	125	$^\circ\text{C}$

Electrical Characteristics

$V_S = 5 \text{ V}$, $T_{amb} = 25^\circ\text{C}$, figure 1, reference point Pin 2, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC supply currents	$V_8 = 5 \text{ V}$ Pin 8 $V_8 = 12 \text{ V}$	I_S		1.2	1.5 2	mA
Minimum supply voltage	Pin 8	V_S	4.5			V
Supply voltage limitation	$I_8 = 3 \text{ mA}$ Pin 8 $I_8 = 30 \text{ mA}$	V_S	13.2	15	16.3 17.2	V
Voltage monitoring Pin 8						
Turn-on threshold		V_{TON}		3.6		V
Turn-off threshold		V_{TOFF}		2.4		V
Temperature coefficient		-TC		0.33		%/K
Selection logic	Pin 1 = \perp (1 s) Pin 1 = + (60 s)	I_1 $-I_1$		6 6		μA
Control logic	Pin 4 = 0 V (Interrupt) Pin 4 = 5 V (Reset) Reset current	I_4 $-I_4$ $-I_4$	65	45 135	1500	μA
Oscillator $f_{osc} = 32768 \text{ Hz}$, $C_{osc} \geq 33 \text{ pF}$						
Operating current	Pin 5, 6	$-I_{osc}$		20		μA
Build-up time		t_{on}		1.5	8	s

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Output stage Pin 3						
Saturation voltages	$-I_O = 100 \text{ mA}$, $V_S = 12 \text{ V}$ $-I_O = 75 \text{ mA}$, $V_S = 12 \text{ V}$	V_O			0.5 0.5	V
Current limitation	$V_3 = 2 \text{ V}$	$-I_O$	100		220	mA
Output pulse width	$f_{osc} = 32768 \text{ Hz}$	t_p		31.25		ms
Voltage limitation	$-I_O = 1 \text{ mA}$	V_{limit}	28.8		33	V
Reserve current	$V_3 = 12 \text{ V}$	$I_{O(R)}$			10	μA
Drive current (ΔI_8 during t_p)	$V_8 = 5 \text{ V}$ Pin 8 $V_8 = 12 \text{ V}$	ΔI_8		4 10		mA

Test Circuit

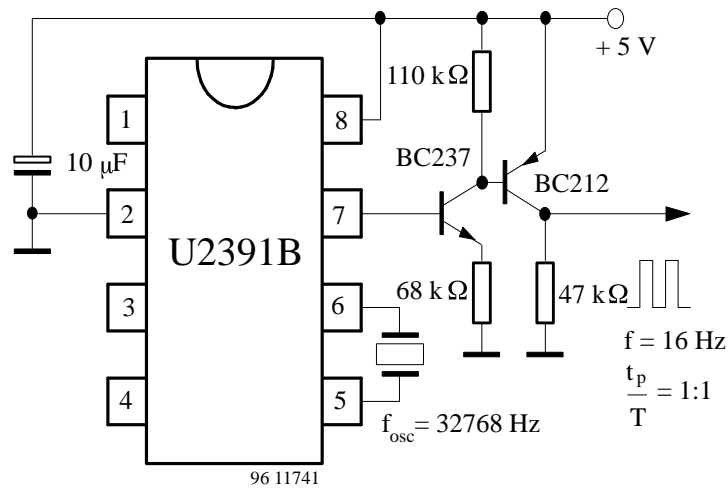


Figure 3. 16 Hz Test

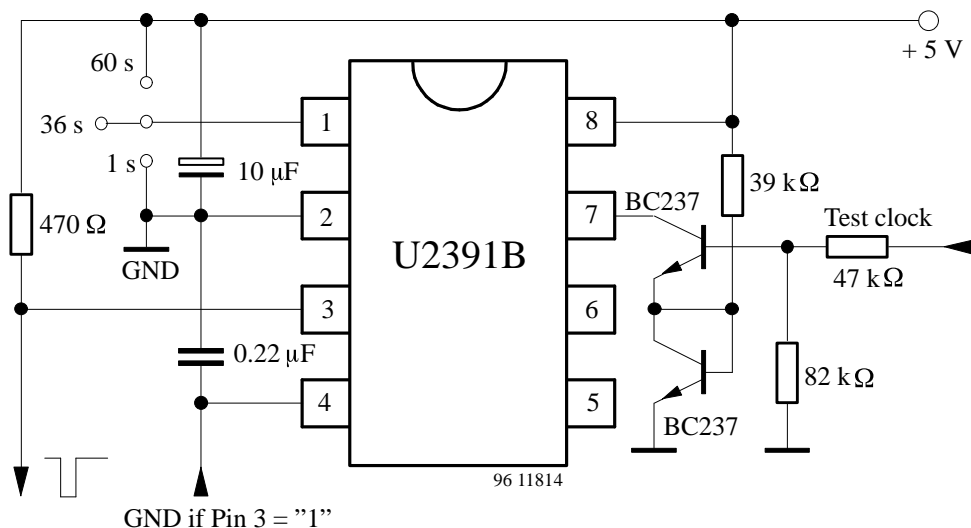


Figure 4. Programmed residual counter $f_i = 2 \text{ kHz}$ (Test clock)

Applications

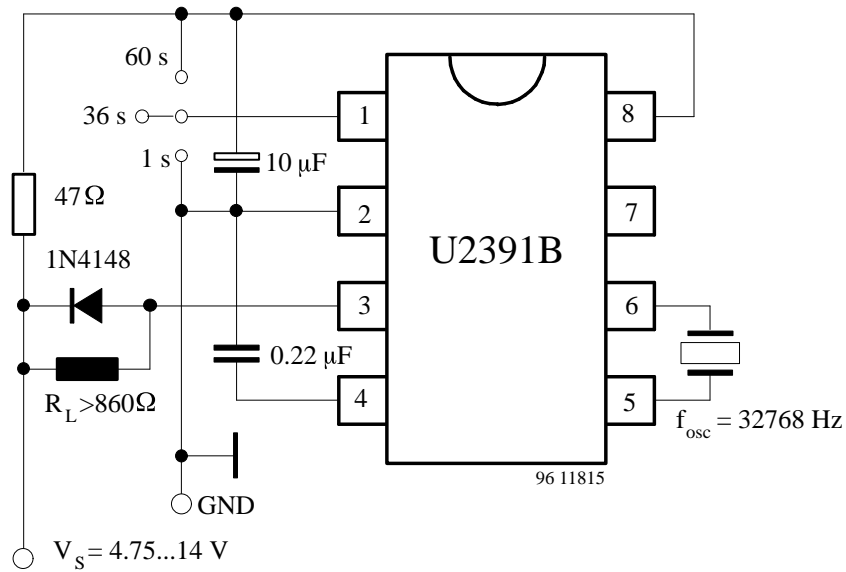


Figure 5. Standard circuit for $V_S = 4.75$ to 14 V, without reset and interruption
Cycle duration selected by Pin 1

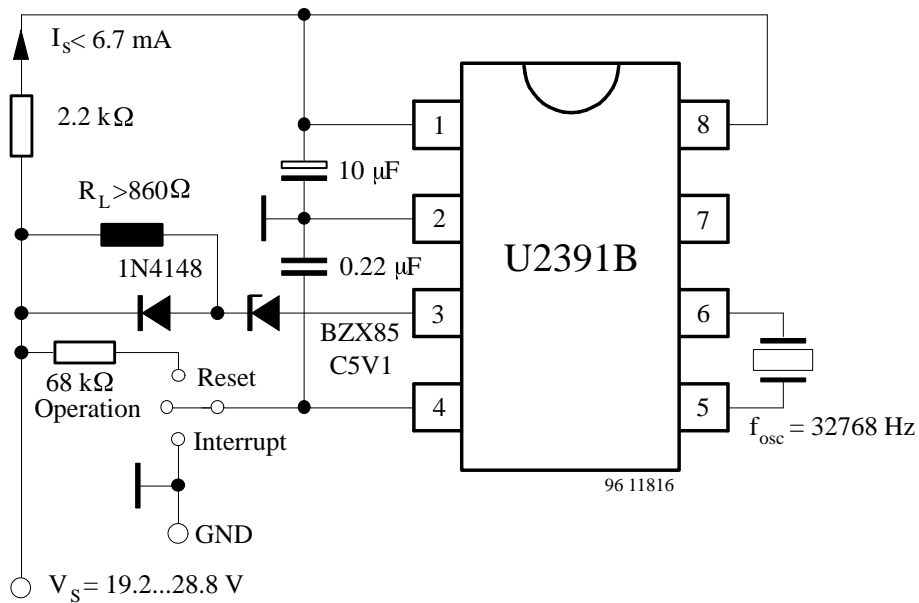
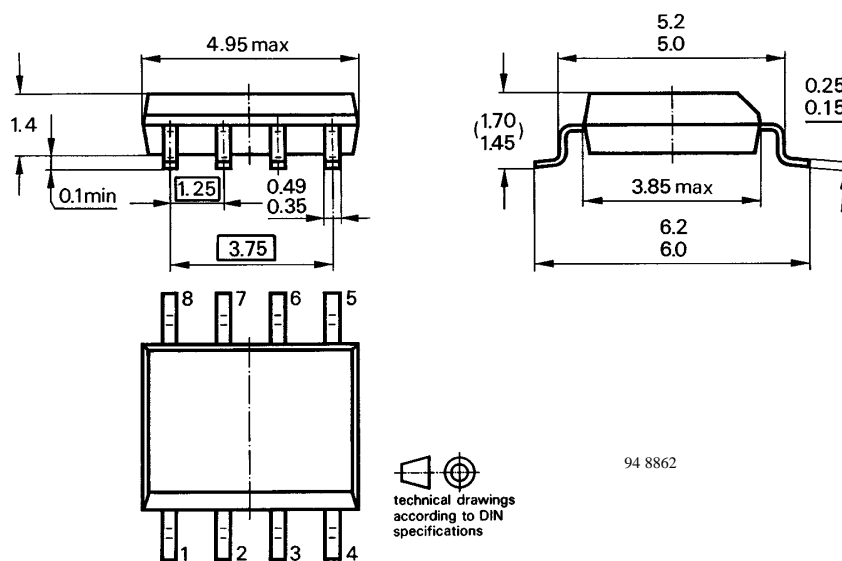


Figure 6. $V_S = 24$ V \pm 20% with reset and interrupt switch,
Cycle time $\tau = 60$ sec.

Dimensions in mm

Package: SO8



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