

PART NUMBERING GUIDE

Environmental/Mechanical Specifications on page F5

Package _____ **OAE 100 27 AA C - 30.000MHz**

OAE = 14 Pin Dip / ±5.2Vdc / ECL
 OAP = 14 Pin Dip / +5.0Vdc / PECL
 OAP3 = 14 Pin Dip / +3.3Vdc / PECL

Inclusive Stability _____
 100= +/-100ppm, 50= +/-50ppm, 25= +/-25ppm,
 10= +/-10ppm @ 25°C / +/-20ppm @ 0-70°C

Operating Temperature Range _____
 Blank = 0°C to 70°C
 27 = -20°C to 70°C (50ppm and 100ppm Only)
 48 = -40°C to 85°C (50ppm and 100ppm Only)

Pin One Connection
 Blank = No Connect
 C = Complimentary Output

Pin Configuration
 See Table Below
 ECL = AA, AB, AC, AB
 PECL = A, B, C, E

ELECTRICAL SPECIFICATIONS

Revision: 1994-B

| | | |
|--|---|---|
| Frequency Range | 20.000MHz to 250.000MHz | |
| Operating Temperature Range | 0°C to 70°C / -20°C to 70°C / -40°C to 85°C | |
| Storage Temperature Range | -55°C to 125°C | |
| Supply Voltage | ECL = ±5.2Vdc ±5% PECL = +5.0Vdc ±5% / +3.3Vdc ±5% | |
| Input Current | 140mA Maximum | |
| Frequency Tolerance / Stability | Inclusive of Operating Temperature Range, Supply Voltage and Load | ±100ppm, ±50ppm, ±25ppm, ±10ppm/±20ppm (0°C to 70°C) |
| Output Voltage Logic High (Voh) | ECL Output | -1.0Vdc Minimum / -0.7Vdc Maximum |
| | PECL Output | 4.0Vdc Minimum / 4.5Vdc Maximum |
| Output Voltage Logic Low (Vol) | ECL Output | -1.95Vdc Minimum / -1.6Vdc Maximum |
| | PECL Output | 3.0Vdc Minimum / 3.42Vdc Maximum |
| Rise Time / Fall Time | 20% to 80% of Waveform | 2nSeconds Maximum |
| Duty Cycle | @ 1.4Vdc w/TTL Load | 50 ±10% (Standard), 50±5% (Optional) |
| Load Drive Capability | ECL Output / AA, AB, AM / AC PECL Output | 50 Ohms into -2.0Vdc / 50 Ohms into +3.0Vdc 50 Ohms into +3.0Vdc |
| Aging (@ 25°C) | ±5ppm / year Maximum | |
| Start Up Time | 20mSeconds Maximum | |

ECL

PIN CONFIGURATIONS

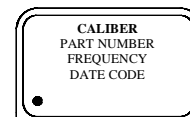
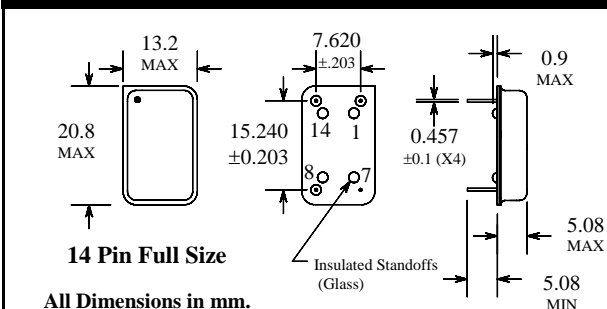
PECL

| | AA | AB | AM |
|---------------|-----------------|----------------------------------|----------------------------------|
| Pin 1 | Ground/ Case | No Connect or Comp. Output | No Connect or Comp. Output |
| Pin 7 | -5.2V | -5.2V | Case Ground |
| Pin 8 | ECL Output | ECL Output | ECL Output |
| Pin 14 | Ground | Case Ground | -5.2Vdc |

| | A | C | D | E |
|---------------|----------------------|----------------------|-------------------|----------------------|
| Pin 1 | No Connect | No Connect | PECL Comp. Out | PECL Comp. Out |
| Pin 7 | Vee (Case Ground) | Vee | Vee | Vee (Case Ground) |
| Pin 8 | PECL Output | PECL Output | PECL Output | PECL Output |
| Pin 14 | Vcc | Vcc (Case Ground) | Vcc | Vcc |

MECHANICAL DIMENSIONS

Marking Guide



Marking Guide
 Line 1: Caliber
 Line 2: Complete Part Number
 Line 3: Frequency in MHz
 Line 4: Date Code (Year/Week)

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|--|--|
| <p>CPO - D P 5 A E T - 125.000MHz</p> | |
| <p>Package Style:</p> <ul style="list-style-type: none"> A = Full Size, 14 Pin Dip B = Half Size, 8 Pin Dip C1 = Ceramic SMD, 5X7X1.6mm (4 pad) C2 = Ceramic SMD, 5X7X1.6mm (6 pad/PECL) P = Plastic SMD, 10X13X5mm <p>Output Type:</p> <ul style="list-style-type: none"> C = HCMOS P = PECL S = HCMOS (with Tristate) <p>Pin One Connection:</p> <ul style="list-style-type: none"> 5 = +5.0V 3 = +3.3V | <p>Pin 1 Connection:</p> <ul style="list-style-type: none"> T = Tristate Enable High P = Power Down <p>Operating Temperature Range:</p> <ul style="list-style-type: none"> Blank = -20°C to 70°C E = -40°C to 85°C (50ppm / 100ppm) <p>Inclusive Stability:</p> <ul style="list-style-type: none"> A = +/-100ppm B = +/-50ppm C = +/-30ppm (0°C-70°C) D = +/-25ppm (0°C-70°C) |

| ELECTRICAL SPECIFICATIONS | | Revision: 2000-B |
|---|--|---|
| Frequency Range | 340.000kHz to 250.000MHz | |
| Operating Temperature Range | -20°C to 70°C / -40°C to 85°C | |
| Storage Temperature Range | -55°C to 125°C | |
| Supply Voltage | 5.0Vdc ±10%, 3.3Vdc ±10% | |
| Input Current | 70mA Maximum | |
| Frequency Tolerance / Stability | Inclusive of Operating Temperature Range, Supply Voltage and Load | ±100ppm, ±50ppm, ±30ppm (-20°C to 70°C), ±25ppm (-20° to 70°C) |
| Output Voltage Logic High (Voh) / PECL Output Voltage Logic High (Voh) / HCMOS | -1.0V Min. Vdd: -0.8V Max. -.04Vdc Min. | |
| Output Voltage Logic Low (Vol) / PECL Output Voltage Logic Low (Vol) / HCMOS | -2.0V Min. Vdd: -1.6V Max. 0.4Vdc Max. | |
| Rise Time / Fall Time | 2nS Max. 20% to 80% / 80% to 20% (PECL) 5nS Max. 10% to 90% / 90% to 10% (HCMOS) | |
| Duty Cycle | PECL HCMOS | 50 ±10% 50 ±5% |
| Load Drive Capability | 5.0V: up to 100.000MHz = 25pF / 100 to 250.000MHz = 10pF 3.3V: up to 100.000MHz = 15pF / 100 to 250.000MHz = 10pF | |
| Pin 1 Tristate Input Voltage | No Connection VIH VIL | Enables Output +2.2Vdc Minimum to Enable Output +0.8Vdc Maximum to Disable Output |
| Disable Current (TS Option) | 30mA Max. (pin 1 ground) | |
| Standby Current (PD Option) | 50uA Max. (pin 1 ground) | |
| Aging (@ 25°C) | ±5ppm / year Maximum | |
| Start Up Time | 10mSeconds Maximum | |
| Absolute Clock Jitter | ±175pSeconds Maximum | |
| One Sigma Clock Jitter | ±50pSeconds Maximum | |