REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added case outline letter U to the drawing. Removed ESDS requirements from drawing. Editorial changes throughout.	90-01-26	M. A. Frye
B	Changes in accordance with NOR 5962-R117-92	92-01-27	M. A. Frye
C	Redrawn with changes. Add device type 05. Add software data protect. Added vendor CAGE 60395 and 61394 as approved sources. Editorial changes throughout.	92-12-18	M.A. Frye
D	Changes in accordance with NOR 5962-R216-93	93-08-20	M.A. Frye
E	Updated boilerplate. Removed data retention and endurance tests from drawing. Removed programming specifics from drawing. - glg	00-08-07	Raymond Monnin
F	Boilerplate update and part of five year review. tcr	07-03-29	Robert M. Heber

REV																				
SHEET																				
REV	F	F	F	F	F															
SHEET	15	16	17	18	19															

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Kenneth Rice	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 32K x 8 EEPROM, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 89-02-13	
	REVISION LEVEL F	SIZE: A; CAGE CODE: **67264**; **5962-88634**
		SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88634	01	U	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	End of write indicator	Endurance
01	See 6.6	32K x 8 EEPROM	120 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling/toggle bit	10,000 cycles
02	See 6.6	32K x 8 EEPROM	120 ns	3 ms	byte/page	$\overline{\text{DATA}}$ polling/toggle bit	10,000 cycles
03	See 6.6	32K x 8 EEPROM	90 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling/toggle bit	10,000 cycles
04	See 6.6	32K x 8 EEPROM	90 ns	3 ms	byte/page	$\overline{\text{DATA}}$ polling/toggle bit	10,000 cycles
05	See 6.6	32K x 8 EEPROM	70 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling/toggle bit	10,000 cycles

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	28	Pin grid array
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP4-F28	28	Flat pack

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.3 V dc to +6.25 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.0 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) 2/ ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Input voltage range (V_{IL}, V_{IH}) ..... -0.3 V dc to +6.25 V dc
Data retention ..... 20 years (minimum)
Endurance ..... 10,000 cycles (minimum)
Chip clear voltage (V_h) ..... 13.0 V dc

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Input voltage, low range (V_{IL}) ..... -0.1 V dc to +0.8 V dc
Input voltage, high range (V_{IH}) ..... +2.0 V dc to V_{CC} + 0.3 V dc

1/ All voltages are referenced to V_{SS} (ground).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table(s). The truth table(s) for unprogrammed devices shall be as specified on figure 3.

3.2.2.1 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with figure 1 and 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current (operating)	I_{CC1}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all I/O's = 0.0 mA, inputs = V_{CC} = 5.5 V, t_{AVAV} = t_{AVAV}(min)	1, 2, 3	All		80	mA
Supply current (TTL standby)	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, all I/O's = 0.0 mA, inputs = V_{CC} - 0.3 V, f = 0.0 MHz	1, 2, 3	01, 02		3	mA
				03, 04, 05		60	
Supply current (CMOS standby)	I_{CC3}	$\overline{CE}$ = V_{CC} - 0.3 V, all I/O's = 0.0 mA, inputs = V_{IL} or V_{CC} - 0.3 V, f = 0.0 MHz	1, 2, 3	01, 02		350	µA
				03, 04, 05		60	mA
Input leakage (high)	I_{IH}	V_{IN} = 5.5 V	1, 2, 3	All		10	µA
Input leakage (low)	I_{IL}	V_{IN} = 0.1 V	1, 2, 3	All	-10		µA
Output leakage (high)	I_{OHZ}	V_{OUT} = 5.5 V, $\overline{CE}$ = V_{IH} 2/	1, 2, 3	All		10	µA
Output leakage (low)	I_{OLZ}	V_{OUT} = 0.1 V, $\overline{CE}$ = V_{IH} 2/	1, 2, 3	All	-10		µA
Input voltage low	V_{IL}		1, 2, 3	All	-0.1	0.8	V
Input voltage high	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.3 V	V
Output voltage low	V_{OL}	I_{OL} = 6.0 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Output voltage high	V_{OH}	I_{OH} = -4.0 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{OE}$ high leakage (chip erase)	I_{OE}	V_H = 13 V	1, 2, 3	All	-10	100	µA
Input capacitance	C_I	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, see 4.3.1c 3/ 4/	4	All		10	pF
Output capacitance	C_O	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, see 4.3.1c 3/ 4/	4	All		10	pF
Read cycle time	t_{AVAV}	See figure 4 5/	9, 10, 11	01, 02	120		ns
				03, 04	90		
				05	70		
Address access time	t_{AVQV}		9, 10, 11	01, 02		120	ns
				03, 04		90	
				05		70	
Chip enable access time	t_{ELQV}		9, 10, 11	01, 02		120	ns
				03, 04		90	
				05		70	
Output enable access	t_{OLQV}		9, 10, 11	01, 02		50	ns
				03, 04, 05		40	
Chip enable to output in low Z 4/	t_{ELQX}		9, 10, 11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip disable to output in high Z 4/	t_{EHQZ}	See figure 4 5/	9, 10, 11	01, 02		50	ns
				03, 04, 05		40	
Output enable to output in low Z 4/	t_{OLQX}		9, 10, 11	All	10		ns
Output disable to output in high Z 4/	t_{OHQX}		9, 10, 11	01, 02		50	ns
				03, 04, 05		40	
Output hold from address change	t_{AXQX}		9, 10, 11	All	0		ns
Write cycle time	t_{WHWL1}		9, 10, 11	01, 03, 05		10	ms
	t_{EHEL1}			02, 04		3	
Address setup time	t_{AVEL} t_{AVWL}		9, 10, 11	All	20		ns
Address hold time	t_{ELAX} t_{WLAX}		9, 10, 11	All	50		ns
Write setup time	t_{WLEL} t_{ELWL}		9, 10, 11	All	0		ns
Write hold time	t_{EHWH} t_{WHEH}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{OE}$ setup time	t_{OHEL} t_{OHWL}	See figure 4 5/	9, 10, 11	All	0		ns
$\overline{OE}$ hold time	t_{EHOL} t_{WHOL}		9, 10, 11	All	0		ns
$\overline{WE}$ pulse width	t_{ELEH} t_{WLWH}		9, 10, 11	All	150		ns
Data setup time	t_{DVEH} t_{DVWH}		9, 10, 11	All	50		ns
Data hold time	t_{EHDX} t_{WHDX}		9, 10, 11	All	0		ns
Byte load cycle	t_{WHWL2}		9, 10, 11	All	.20	149	µs
Last byte loaded to data polling 4/	t_{WHEL} t_{EHEL}		9, 10, 11	All		0	ns
$\overline{CE}$ setup time	t_{ELWL1}		9, 10, 11	All	5		µs
Output setup time	t_{OVHWL}		9, 10, 11	All	5		µs
$\overline{CE}$ hold time	t_{WHEH1}		9, 10, 11	All	5		µs
$\overline{OE}$ hold time	t_{WHOH}		9, 10, 11	All	5		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High voltage	V_H	See figure 4 5/	9, 10, 11	All	12	13	V
Chip erase	t_{WLWH2}		9, 10, 11	All		210	ms
$\overline{WE}$ pulse width for chip erase	t_{WLWH1}		9, 10, 11	All	10		ms

1/ DC and read mode.
2/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}.
3/ All pins not being tested are to be open.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ Tested by application of specified timing signals and conditions, including:

Equivalent ac test conditions for all device types:
Output load: 1 TTL gate and C_L = 100 pF (minimum) or equivalent circuit.
Input rise and fall times ≤ 10 ns. Input pulse levels: 0.4 V and 2.4 V.
Timing measurements reference levels:
Inputs 1.0 V and 2.0 V. Outputs 0.8 V and 2.0 V.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

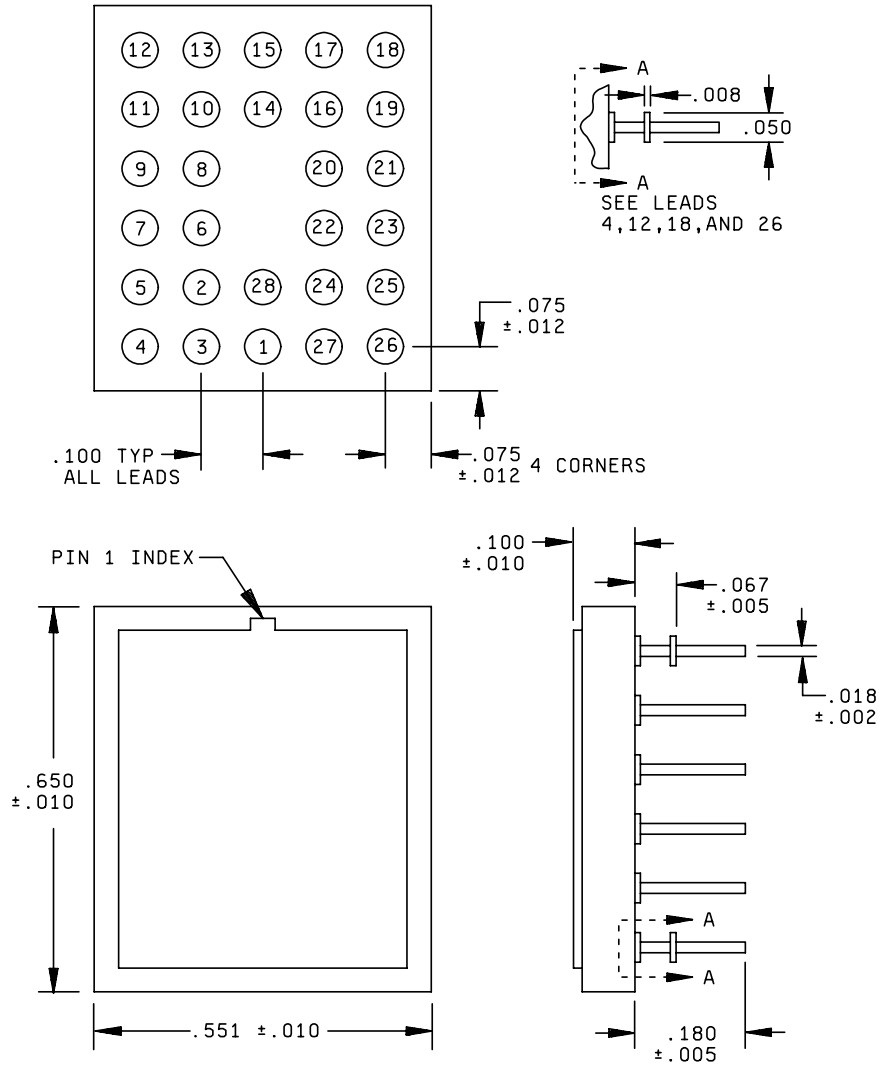
3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified by the manufacturer.

3.10.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified by the manufacturer and shall be made available upon request.

3.10.3 Verification of erasure or programmability of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot or sample.



Inches	mm
.002	0.05
.005	0.13
.008	0.20
.010	0.25
.012	0.30
.018	0.46
.050	1.27
.067	1.70
.075	1.90
.100	2.54
.180	4.57
.551	14.00
.650	16.51

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are for general information only.

FIGURE 1. Case outline U.

Device types	01 through 05	
Case outlines	X, Z, U	Y
Terminal number	Terminal symbol	
1	A14	NC
2	A12	A14
3	A7	A12
4	A6	A7
5	A5	A6
6	A4	A5
7	A3	A4
8	A2	A3
9	A1	A2
10	A0	A1
11	I/O0	A0
12	I/O1	NC
13	I/O2	I/O0
14	VSS	I/O1
15	I/O3	I/O2
16	I/O4	VSS
17	I/O5	NC
18	I/O6	I/O3
19	I/O7	I/O4
20	$\overline{CE}$	I/O5
21	A10	I/O6
22	$\overline{OE}$	I/O7
23	A11	$\overline{CE}$
24	A9	A10
25	A8	$\overline{OE}$
26	A13	NC
27	$\overline{WE}$	A11
28	VCC	A9
29	----	A8
30	----	A13
31	----	$\overline{WE}$
32	----	VCC

FIGURE 2. Terminal connections.

Device types 01 through 05

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Chip clear	V_{IL}	V_H	V_{IL}	X
Byte write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write inhibit	X	V_{IL}	X	High Z/D_{OUT}
Write inhibit	X	X	V_{IH}	High Z/D_{OUT}

V_{IH} = High logic level
V_{IL} = Low logic level
V_H = Chip clear high voltage
X = Don't care
High Z = High impedance state
D_{IN} = Data in
D_{OUT} = Data out

FIGURE 3. Truth table for unprogrammed devices.

Read cycle waveform

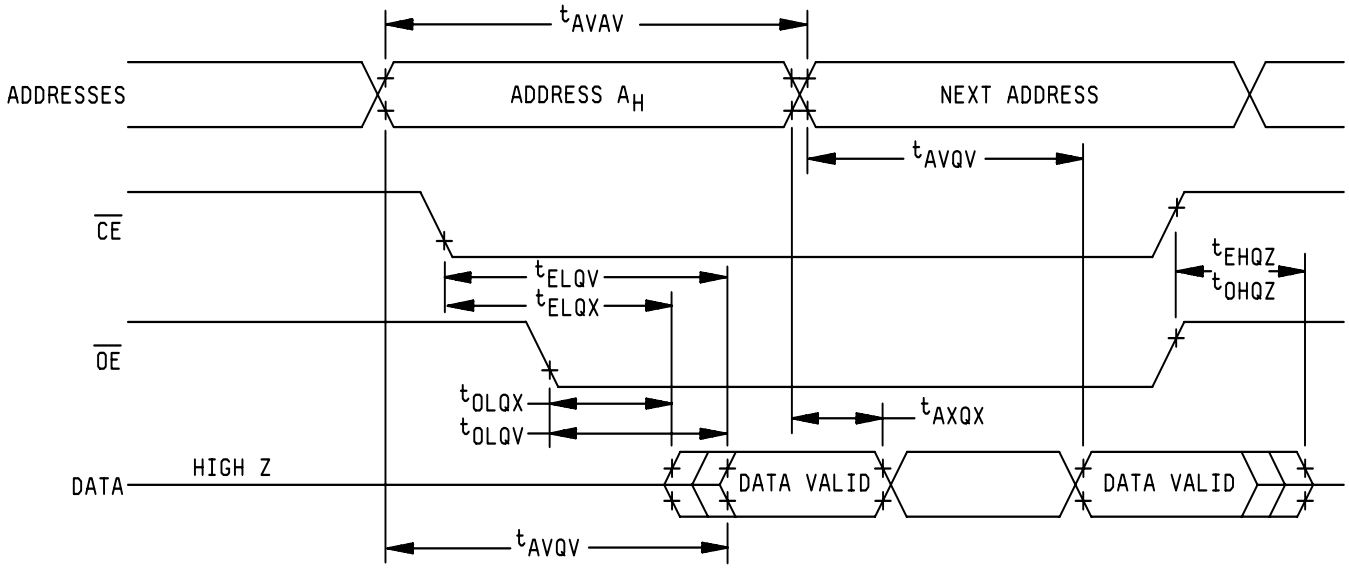


FIGURE 4. AC waveforms.

$\overline{WE}$ controlled byte write programming waveforms

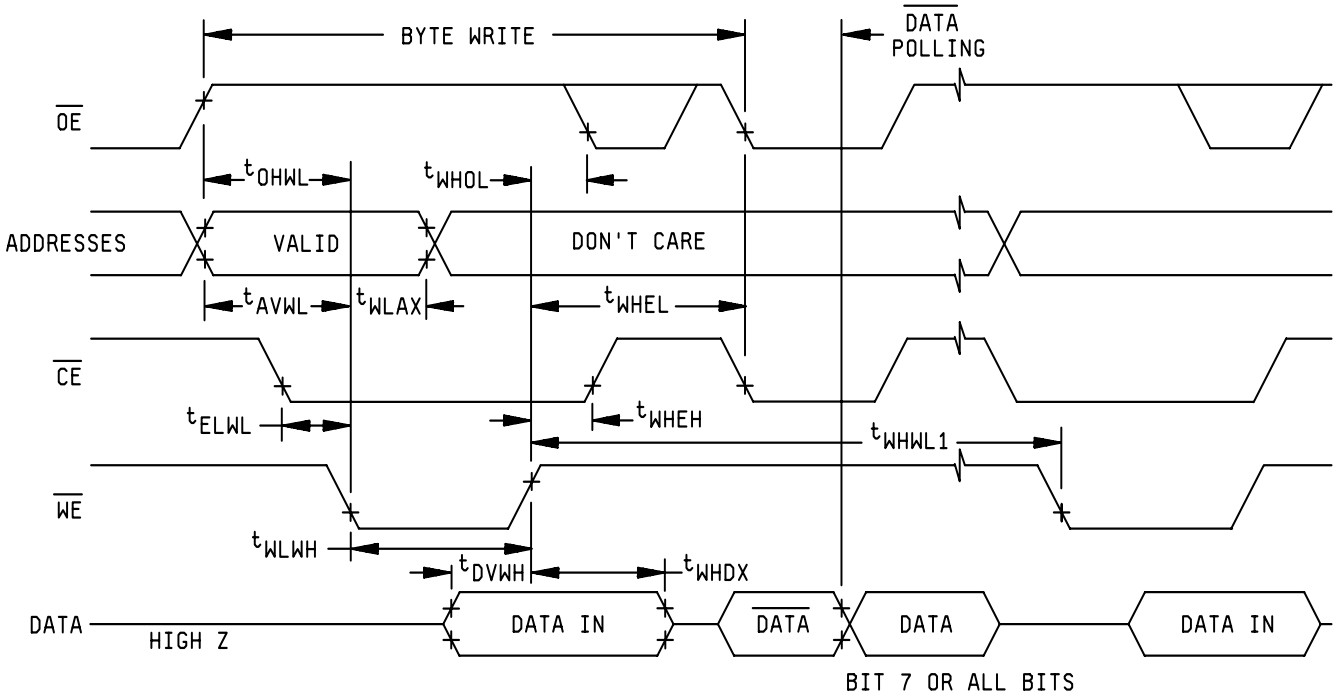


FIGURE 4. AC waveforms - continued.

$\overline{CE}$ controlled byte write programming waveforms

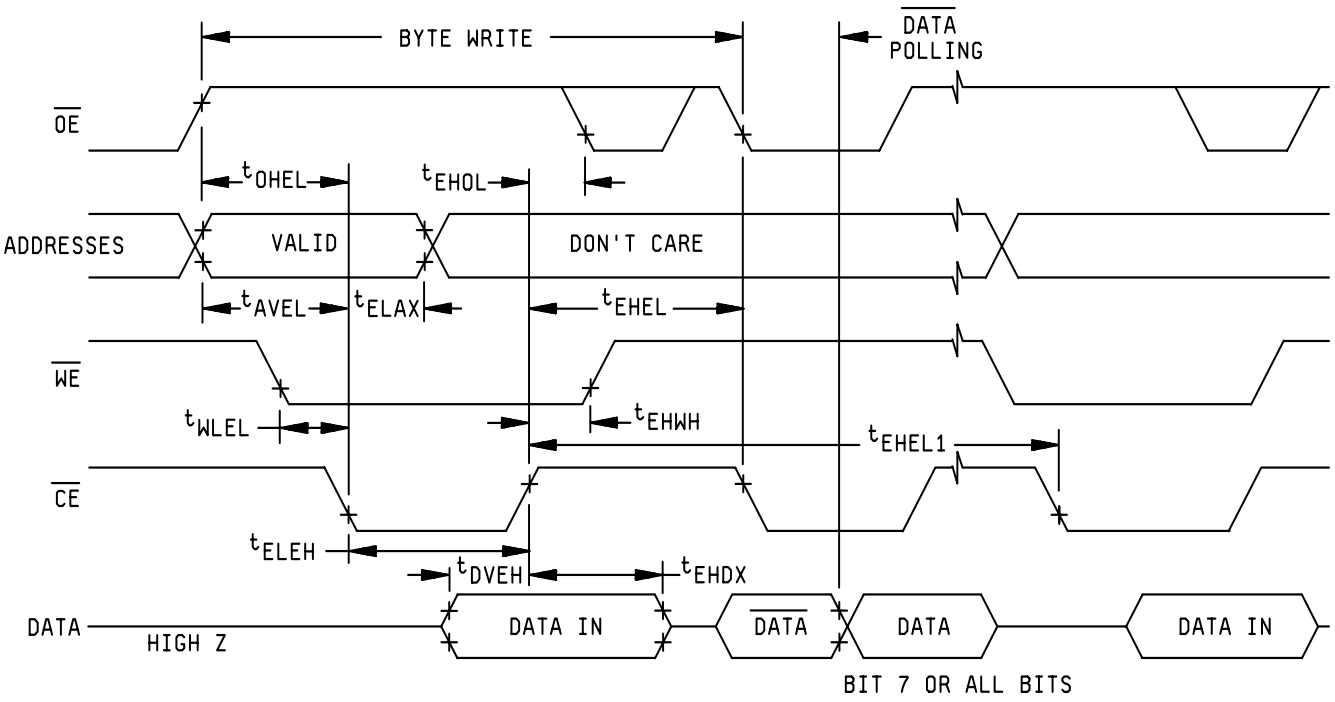


FIGURE 4. AC waveforms - continued.

Page write waveform

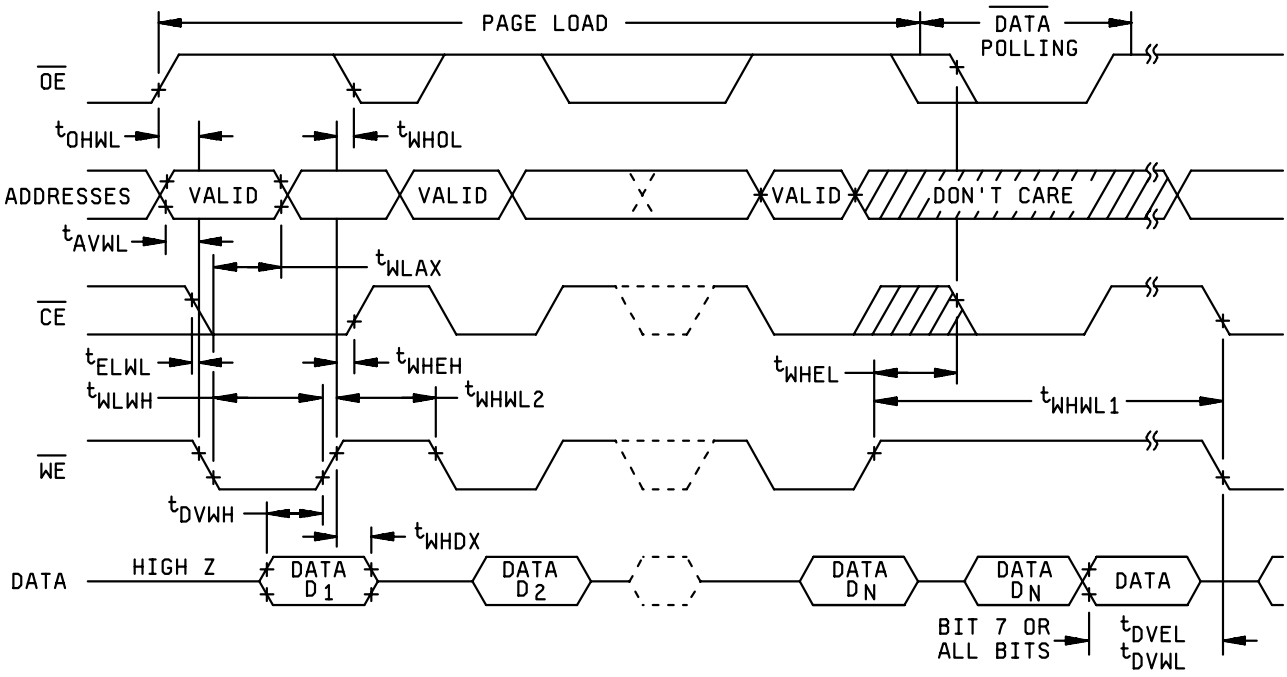


FIGURE 4. AC waveforms - continued.

Chip clear waveform

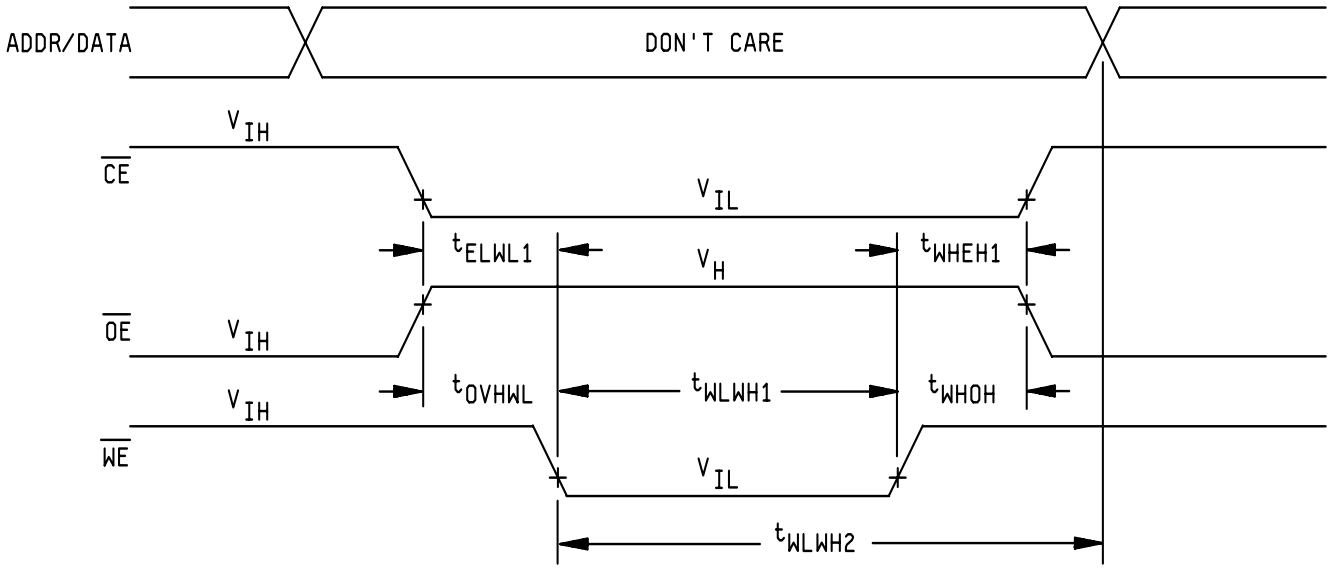


FIGURE 4. AC waveforms - continued.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or F. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a checkerboard pattern or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured for initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices, all input and output terminals tested, and no failures.

d. As a minimum, subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections. Groups C and D inspections shall be in accordance with method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or F. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables of method 5005 of MIL-STD-883 and as follows.

4.4.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.4.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available on request.

4.4.3 Erasing procedure. The erasing procedures shall be as specified by the device manufacturer and shall be made available on request.

4.4.4 Software data protection. The software data protect procedures shall be as specified by the device manufacturer and shall be made available on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9, or 2, 8A, 10
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11

1/ (*) Indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using multifunction testers.
3/ Subgroups 7, 8A, and 8B shall consist of writing and reading the data pattern specified in accordance with the limits of table I, subgroups 9, 10, and 11.
4/ For all electrical tests, the device shall be programmed to the data pattern specified.
5/ (**) Indicates that subgroup 4 will only be performed during initial testing and after design or process changes (see 4.3.1c).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replacability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Approved sources of supply . Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 07-03-29

Approved sources of supply for SMD 5962-88634 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8863401UA	1FN41	AT28HC256-12UM/883
	3/	TM28HC256-120
5962-8863401UC	3/	X28HC256KMB-12
5962-8863401XA	1FN41	AT28HC256-12DM/883
	34371	28HC256
	3/	X28HC256DMB-12
	3/	DM28HC256-120
5962-8863401YA	1FN41	AT28HC256-12LM/883
	3/	X28HC256EMB-12
	3/	LM28HC256-120
5962-8863401ZA	1FN41	AT28HC256-12FM/883
	3/	FM28HC256-120
5962-8863401ZC	34371	28HC256
	3/	X28HC256FMB-12
5962-8863402UA	1FN41	AT28HC256FL-12UM/883
	3/	TM28HC256-120
5962-8863402XA	1FN41	AT28HC256FL-12DM/883
	3/	DM28HC256-120
5962-8863402YA	1FN41	AT28HC256FL-12LM/883
	3/	LM28HC256-120
5962-8863402ZA	1FN41	AT28HC256FL-12FM/883
	3/	FM28HC256-120
5962-8863403UA	1FN41	AT28HC256-90UM/883
	3/	TM28HC256-90
5962-8863403UC	3/	X28HC256KMB-90
5962-8863403XA	1FN41	AT28HC256-90DM/883
	34371	28HC256
	3/	X28HC256DMB-90
	3/	DM28HC256-90
5962-8863403YA	1FN41	AT28HC256-90LM/883
	3/	X28HC256EMB-90
	3/	LM28HC256-90

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8863403ZA	1FN41	AT28HC256-90FM/883
	3/	FM28HC256-90
5962-8863403ZC	34371	28HC256
	3/	X28HC256FMB-90
5962-8863404UA	1FN41	AT28HC256F-90UM/883
	3/	TM28HC256-90
5962-8863404XA	1FN41	AT28HC256F-90DM/883
	3/	DM28HC256-90
5962-8863404YA	1FN41	AT28HC256F-90LM/883
	3/	LM28HC256-90
5962-8863404ZA	1FN41	AT28HC256F-90FM/883
	3/	FM28HC256-90
5962-8863405UA	1FN41	AT28HC256-70UM/883
	3/	TM28HC256-70
5962-8863405XA	1FN41	AT28HC256-70DM/883
	3/	DM28HC256-70
5962-8863405YA	1FN41	AT28HC256-70LM/883
	3/	LM28HC256-70
5962-8863405ZA	1FN41	AT28HC256-70FM/883
	3/	FM28HC256-70

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
1FN41	ATMEL Corporation 2325 Orchard Parkway San Jose, CA 95131 - 1034
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035 - 5680