

Recording Y/C Amplifier

Description

CXA1047M is a bipolar IC developed to process the recording signals (luminance/chroma signals) of 8 mm video's.

Features

- Recording Y(Luminance)/C(Chroma) signals can be processed by 1 chip IC.
- Built-in, DDS (Date Display System) and timing phase detector, circuits.
- Low power consumption 95 mW (Typ.) (during recording)
- Single supply voltage 5 V

Functions

Y clamp circuit, KNEE circuit, camera white clip, Y emphasis circuit, white clip circuit, dark clip circuit, FM modulator, chroma emphasis circuit, chroma AGC, MUTE circuit, DDS circuit. Timing phase detector circuit, 4.2 V regulator.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

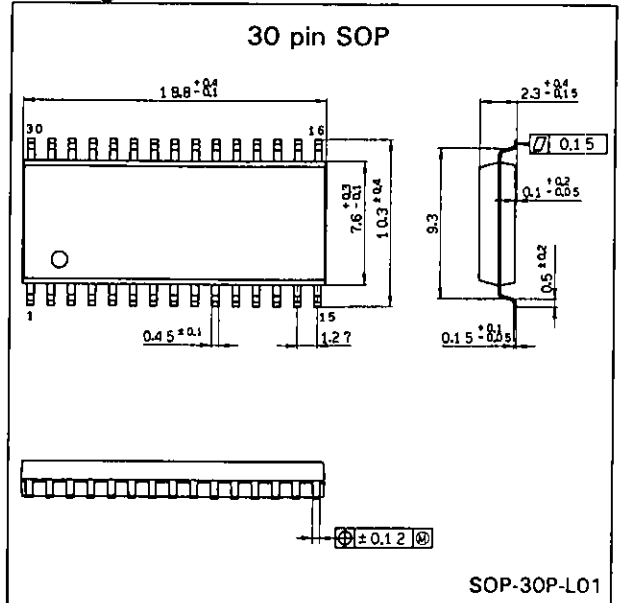
• Supply voltage	VCC	7.0	V
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-55 to +150	°C
• Allowable power dissipation	PD	600	mW

Recommended Operating Condition

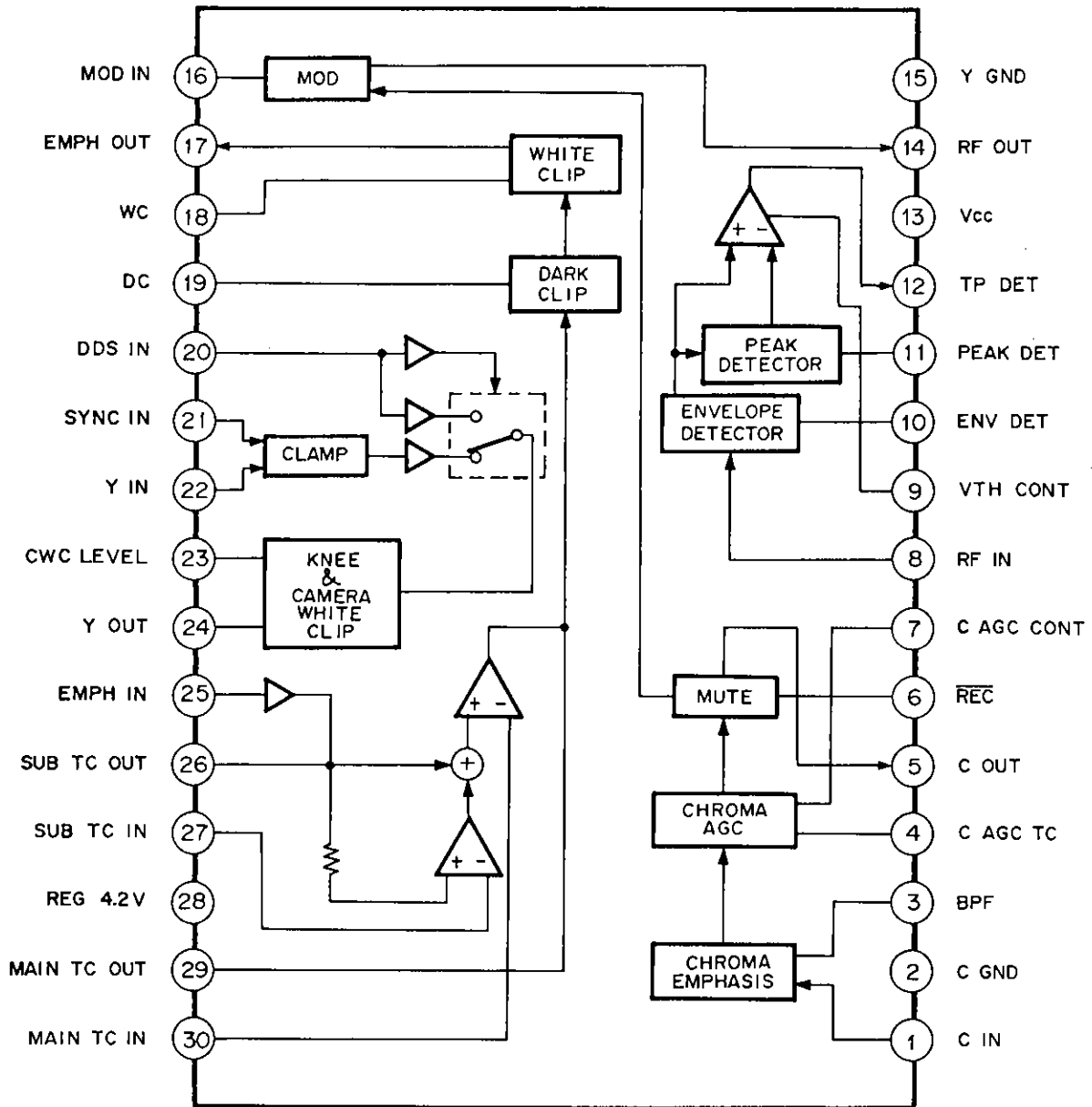
• Supply voltage	VCC	4.5 to 5.5	V
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Package Outline

Unit: mm



Block Diagram



Pin Description and Equivalent Circuit

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
1	C IN		2.8 V	420 mVp-p (Ref. level)	Down converted chroma (743 kHz) signal input pin.
2	C GND	—	—	—	GND for chroma emphasis, chroma AGC and 4.2 V Reg.
3	BPF		2.35 V	—	BPF connecting pin for chroma emphasis.
4	C AGC TC		1.3 V	—	Time constant connecting pin for chroma AGC.
5	C OUT		2.4 V	420 mVp-p	Chroma signal output pin.
6	REC		—	—	Control pin for REC/PB mode Vcc to 3.0 V: PB 1.0 V to GND: REC
7	C AGC CONT		2.3 V	—	Chroma AGC level adjustment pin. By applying an external DC, AGC setting level can be varied.
8	RF IN		3.7 V		Playback RF signal input pin for Timing phase detector. (Track adjustment, f3 detection)

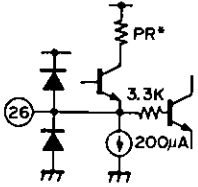
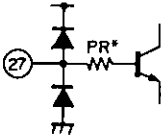
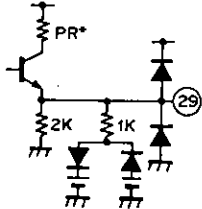
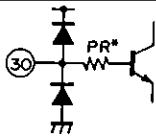
Note) PR indicates Protective Resistance (about 140Ω).

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
9	V _{TH} CONT		1.3 V	—	Sets the peak level (V _{TH}) of the peak detection circuit. By applying an external DC, V _{TH} can be varied.
10	ENV DET		4.4 V	—	Connects the time constant for the detection of the playback RF signal envelope.
11	PEAK DET		3.7 V	—	Connects the time constant for the peak detection of the playback RF signal envelope.
12	TP DET		—	—	Peak detection output pin for the playback RF signal envelope.
13	V _{CC}	—	—	—	Supply pin
14	RF OUT		3.3 V	500 mVp-p	FM MOD output pin
15	Y GN	—	—	—	GND for Y system amplifier, Y emphasis and DDS, timing phase detector circuits.
16	MOD IN		2.1 V	—	FM MOD input pin (Current input). Imaginary-short to 2.1 V (V _{REG} /2)
17	EMPH OUT		2.1 V	250 mVp-p	Output pin of Y signal emphasis circuit.

Note) PR indicates Protective Resistance (about 140Ω).

No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
18	WC		2.7 V	—	Sets the white clip level of Y signal. By applying an external DC, the white clip level can be varied.
19	DC		1.9 V	—	Sets the dark clip level of Y signal. By applying an external DC, the dark clip level can be varied.
20	DDS IN		2.4 V	—	DDS signal input pin. An input level above 40 mV _{o-p} is necessary.
21	SYNC IN		—	—	Composite sync input pin. H level: 3.5 V to V _{cc} L level: GND to 1.0 V
22	Y IN		2.1V		Input pin for Y signal from the camera system.
23	CWC LEVEL		3.3 V	—	Sets the white clip level of the Y signal from the camera system. By applying an external DC, the white clip level can be varied.
24	Y OUT		2.1 V		Output pin of Y signal (including DDS signal).
25	EMPH IN		—		Input pin of the Y signal emphasis circuit.

Note) PR indicates Protective Resistance (about 140Ω).

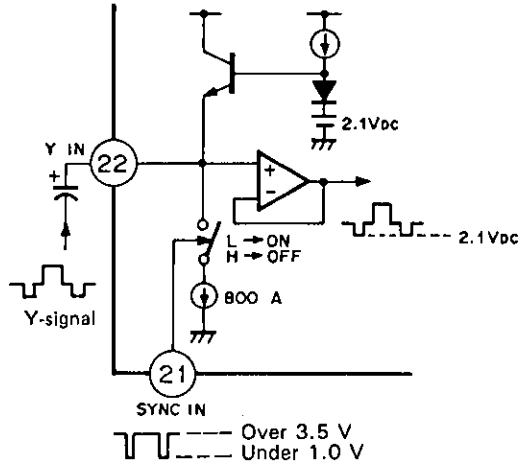
No.	Symbol	Equivalent Circuit	Voltage		Description
			DC	AC	
26	SUB TC OUT		2.1 V	500 mVp-p	The time constant for the sub emphasis circuit of the Y signal emphasis circuit is connected.
27	SUB TC IN		—	—	The time constant for the sub emphasis circuit is connected. It is also the input pin of the sub emphasis limiter.
28	REG 4.2 V	—	4.2 V	—	Regulator (4.2 V) output pin.
29	MAIN TO OUT		2.1 V	250 mVp-p	The time constant for the main emphasis circuit of the Y signal emphasis circuit is connected. It is also the output pin of the Y signal emphasis circuit.
30	MAIN TC IN		—	—	The time constant for the main emphasis circuit is connected. It is also the input pin of the main emphasis amplifier.

Note) PR indicates Protective Resistance (about 140Ω).

Description of Functions

1. Y clamp circuit

The Y signal sync tip level is clamped at 2.1 VDC. At that time it is necessary to input COMP sync to the sync IN of pin 21.



Y clamp circuit

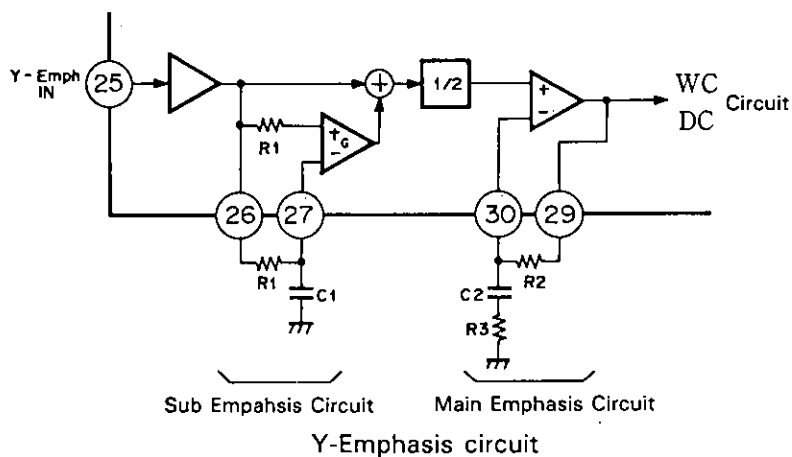
COMP sync L level: 0 V to 1.0 V
 H level: 3.5 V to Vcc

2. KNEE and CWC (Camera White Clip) Circuit

When the reference level (from the Y signal sync tip level to the white peak) is set to 1.0 V (100% white), a signal of 1.3 V maximum (130%) is input. There to prevent over modulation, it is necessary to control the white peak level at the CWC circuit. Also, to preserve the high luminance tone, soft limiter characteristics are maintained at the KNEE circuit.

3. Y Emphasis circuit

Here is shown the structure of Y-Emphasis circuit for CXA1047M.

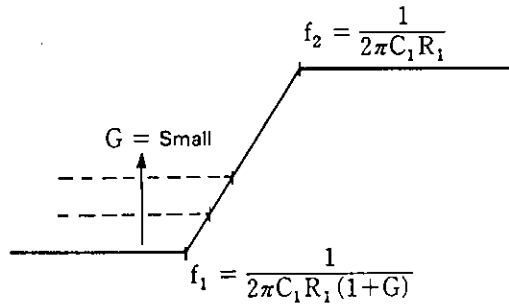


Y-Emphasis circuit

Sub Emphasis Transfer Function $H(S)_{SUB}$ is as follows:

$$H(S)_{SUB} = 1 + \left(1 - \frac{1}{1 + SC_1R_1}\right) G = \frac{1 + SC_1R_1(1 + G)}{1 + SC_1R_1}$$

Here, in amplifier G , by providing non linear characteristics where the gain varies according to the input level, the sub emphasis transfer function $H(S)_{SUB}$ achieves non linear emphasis characteristics. Sub emphasis characteristics are shown in the figure below.



Sub emphasis characteristics

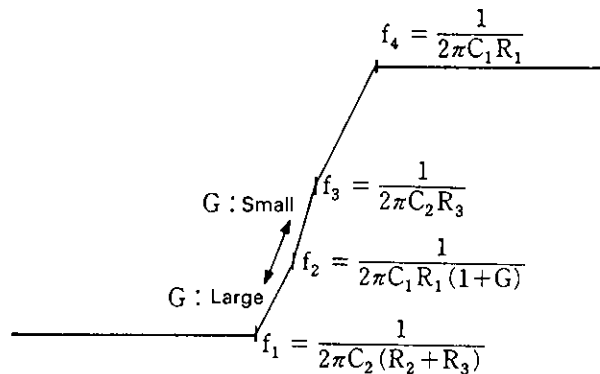
Main emphasis transfer function $H(S)_{MAIN}$ is as follows:

$$H(S)_{MAIN} = \frac{1 + SC_2(R_2 + R_3)}{1 + SC_2R_3}$$

Accordingly the total Y-emphasis characteristics become:

$$H(S)_{EMP} = \frac{\{1 + SC_1R_1(1 + G)\} \{1 + SC_2(R_2 + R_3)\}}{(1 + SC_1R_1)(1 + SC_2R_3)}$$

The frequency response of Y-emphasis is shown in the figure below.



Y-Emphasis characteristics

When $C_2(R_2 + R_3) > C_1R_1(1 + G) > C_2R_3 > C_1R_1$

The Y-emphasis circuit reference input level is set to 500 mVp-p and at that time the output level is 250 mVp-p.

4. White Clip Circuit (WC) and Dark Clip Circuit (DC)

The output signal of the Y-emphasis circuit features a spike wave at the signal's rising or falling edge.

There may generate over modulation.

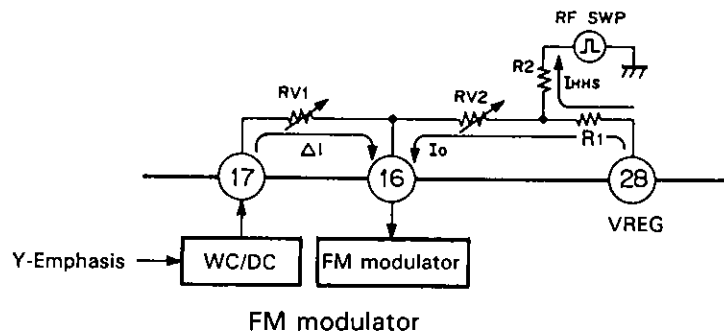
In the WC and DC circuits, a diode limiter is used to determine the DC clip level of the Y-emphasis output signal. Also by applying an external DC, the clip level can be varied.

5. FM Modulator

The CXA1047M FM modulator consists of a current controlled oscillator.

The modulator input (pin 16) is imaginary-short to $V_{REG}/2$ ($\cong 2.1$ V) under a low input impedance.

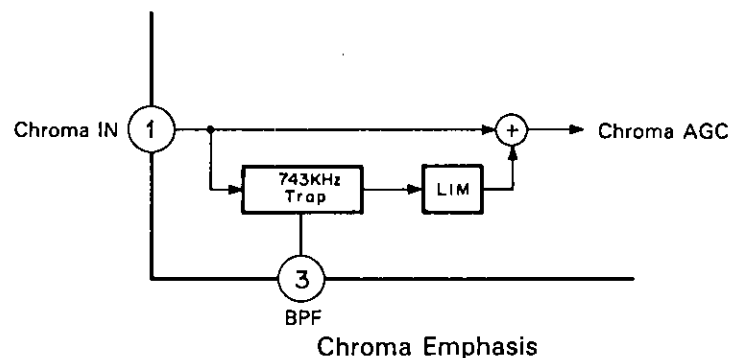
The bias current for carrier (i_0), the modulation signal current and HHS ($1/2$ fh shift) current are added to input.



At the figure, (FM modulator) the carrier bias current I_0 can be adjusted through RV_2 . Also, the level (deviation) of signal current Δi can be set with RV_1 . The HHS current (I_{HHS}) is determined through R_1 , R_2 , and RF SWP level.

The FM modulator control sensitivity of CXA1047M amounts to about $15 \text{ kHz}/\mu\text{A}$.

6. Chroma Emphasis

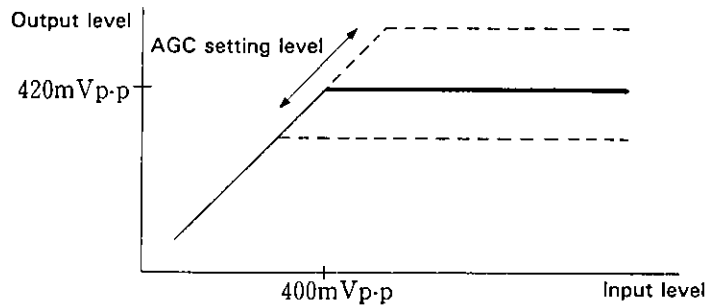


The down converted chroma signal is applied to the chroma Emphasis input, and the amount of emphasis diminishes around f_{sc} (color sub carrier frequency: 743.444 kHz) as it is distanced from f_{sc} , the amount of emphasis grows.

The above figure shows the structure of the chroma emphasis. By using the 743 kHz Trap, the amount of emphasis around f_{sc} is controlled, and LIM (limiter) realizes the non linear characteristics.

7. Chroma AGC

Chroma AGC Input/Output characteristics are shown in the Figure below.



Chroma AGC Characteristics

By applying DC to pin 7, AGC setting level can be varied.

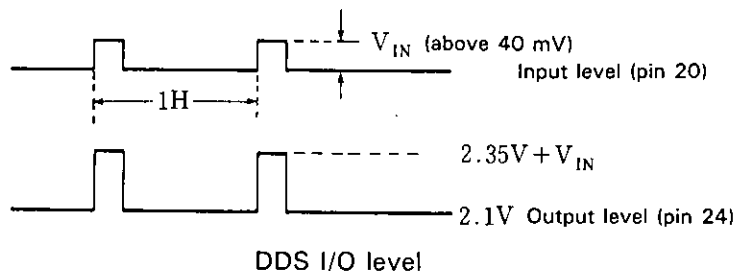
For the AGC setting level, assuming DC of pin 7 is V_7 , the following relation is obtained.

$$\text{AGC setting level (output, p-p)} \approx V_7 \frac{30}{170}$$

8. DDS (Date Display System) Circuit

The DDS circuit serves to input the date and other information.

When DDS signal is input, Y signal and DDS signal are switched and DDS signal is output at Y OUT. The Y/DDS signal switching is executed at the DDS signal itself, and a signal level above 40 mVp-p is necessary. The relation between the DDS input level and output level is shown in the figure below.

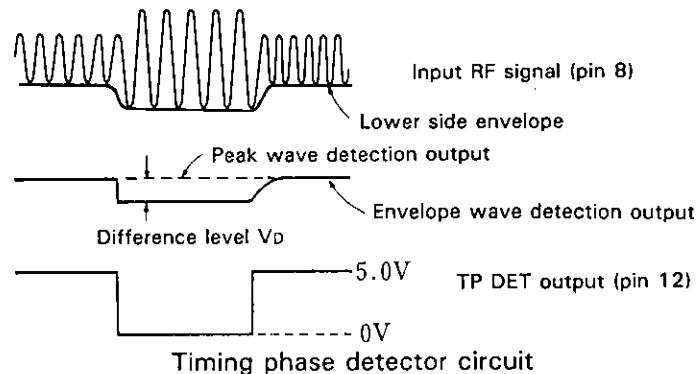


DDS I/O level

9. Timing Phase Detector Circuit

The timing phase detector circuit executes envelope wave detection and peak wave detection for

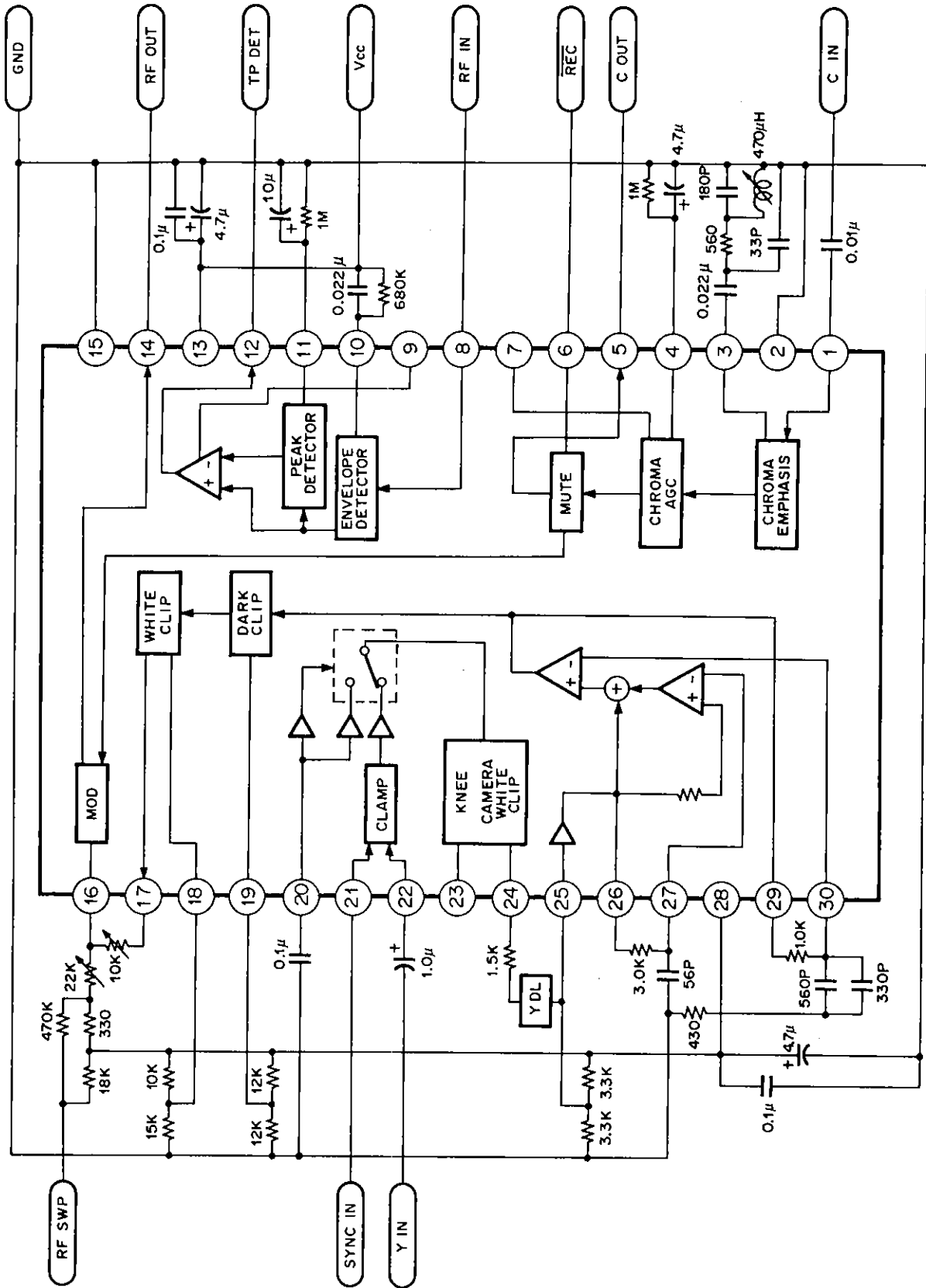
- 1) Timing phase detection for the track adjustment using slow playback.
- 2) Phase adjustment of ATF PILOT signal.



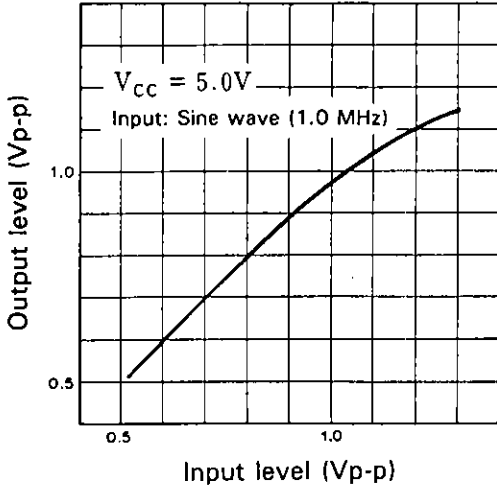
Timing phase detector circuit

The envelope wave detection circuit detects the lower side envelope of input RF signal. The peak detection circuit detects the level difference V_D of the envelope wave detection output. By applying DC to pin 9 the difference detection level (V_{TH}) can be varied. However when pin 9 is open (it is internally biased to 1.3 V), V_{TH} becomes 50 mV, and with a signal where the difference exceeds 50 mV, TP DET output is obtained.

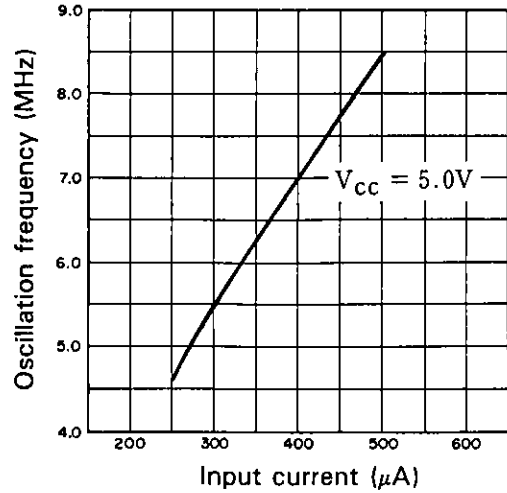
Application Circuit



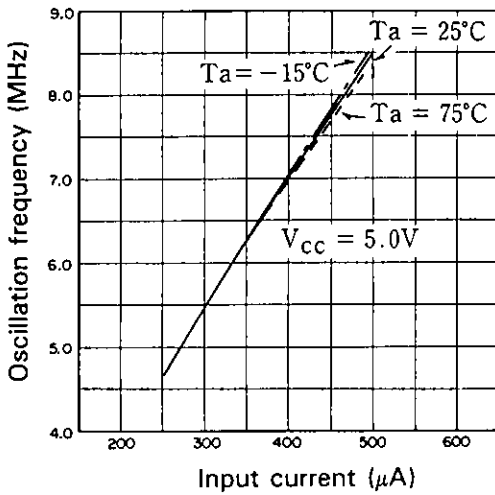
KNEE and CWC characteristics



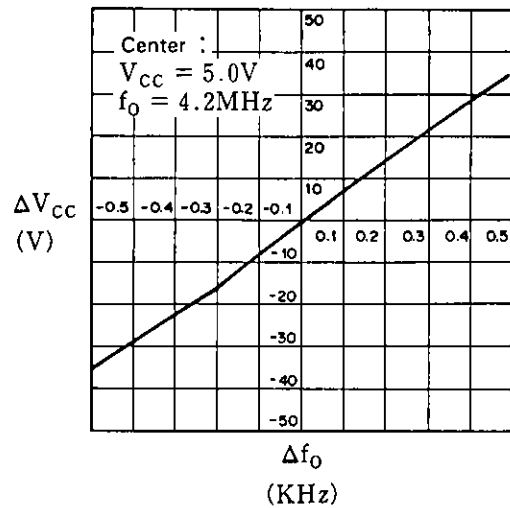
FM MOD Oscillation frequency characteristics



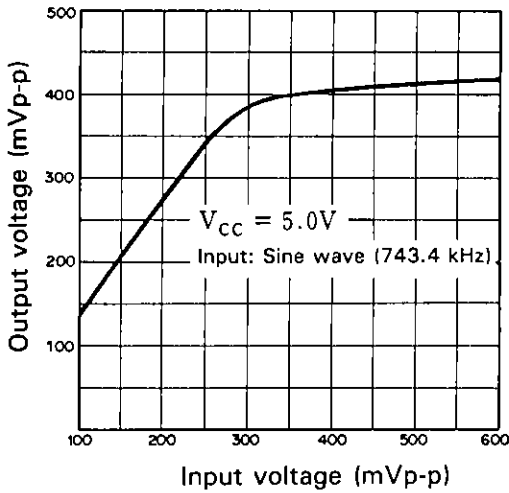
FM MOD Oscillation frequency temperature characteristics



FM MOD Oscillation frequency supply voltage characteristics



Chroma AGC I/O characteristics (Including chroma emphasis)



Y-Emphasis characteristics

