

Single and Dual Retriggerable Monostable Multivibrators with Clear

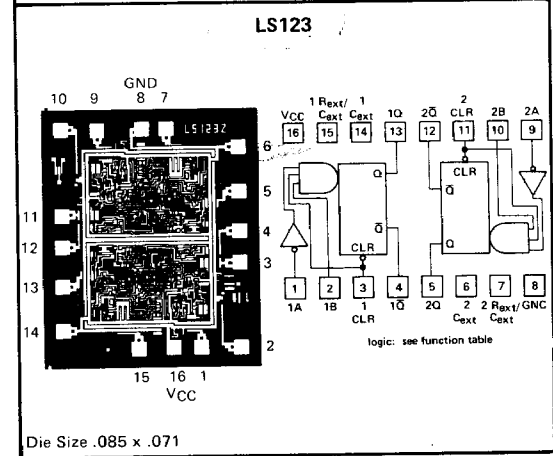
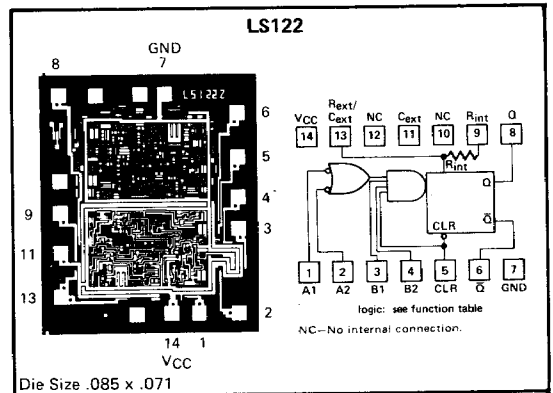
LS122 LS123

FEATURES

- Functionally and Mechanically Identical to 54122 and 54123
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Low Power Dissipation:
 - 'LS122 . . . 30 mW Typical
 - 'LS123 . . . 60 mW Typical
- Compensated for VCC and Temperature Variations
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- 'LS122 Has Internal 10 kΩ Timing Resistor
- Diode-Clamped Inputs
- Compatible for Use with TTL or DTL

DESCRIPTION

The 'LS122 and 'LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.



'LS122 FUNCTION TABLE
(SEE NOTE 1)

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	[Pulse]	[Pulse]
H	L	X	H	↑	[Pulse]	[Pulse]
H	X	L	H	H	[Pulse]	[Pulse]
H	X	L	↑	H	[Pulse]	[Pulse]
H	X	L	H	↑	[Pulse]	[Pulse]
H	H	↓	H	H	[Pulse]	[Pulse]
H	↓	↓	H	H	[Pulse]	[Pulse]
H	↓	H	H	H	[Pulse]	[Pulse]
↑	L	X	H	H	[Pulse]	[Pulse]
↑	X	L	H	H	[Pulse]	[Pulse]

'LS123 FUNCTION TABLE
(SEE NOTE 1)

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	[Pulse]	[Pulse]
H	↓	H	[Pulse]	[Pulse]
↑	L	H	[Pulse]	[Pulse]

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LS122 LS123

- NOTES: 1. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, H = one high-level pulse, L = one low-level pulse, X = irrelevant (any input, including transitions).
 2. To use the internal timing resistor of 'LS122, connect R_{int} to V_{CC} .
 3. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
 4. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
 5. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

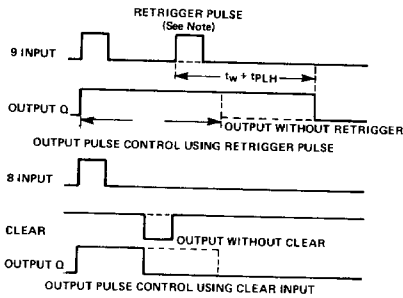


FIGURE 1—Typical Input/Output Pulses

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The 'LS122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external

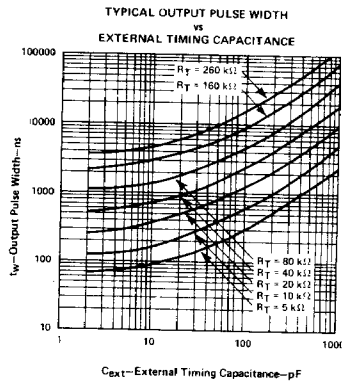


FIGURE 2

†These values of resistance exceed the maximum recommended for use over the full temperature range of the 9LS/54LS' circuits.

capacitor and resistor. For $C_{ext} > 1000\text{ pF}$, the output pulse width (t_w) is defined as:

$$t_w = 0.4 \cdot R_T \cdot C_{ext}$$

where

- R_T is in $\text{k}\Omega$ (either internal or external timing resistor),
- C_{ext} is in pF ,
- t_w is in ns .

For pulse widths when $C_{ext} \leq 1000\text{ pF}$, see Figure 2.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			400			400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	A or B inputs high	40		40			ns
	A or B inputs low	40		40			
	Clear low	40		40			
External timing resistance, R_{ext}	5		225	5		360	$\text{k}\Omega$
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal	50			50			pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	9LS/54LS			9LS/74LS			Unit			
		Min.	Typ.‡	Max.	Min.	Typ.‡	Max.				
V _{IH}	High-level input voltage	2			2			V			
V _{IL}	Low-level input voltage			0.7			0.8	V			
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5		-1.5	V		
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2V, V _{IL} = V _{IL} max, I _{OH} = -400 μA		2.5	3.5		2.7	3.5	V		
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2V, V _{IL} = V _{IL} max							V		
		I _{OL} = 4 mA	0.25	0.4		0.25	0.4				
	I _{OL} = 8 mA					0.35	0.5				
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7V				0.1		0.1	mA		
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20		20	μA		
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4		-0.4	mA		
I _{OS}	Short-circuit output current‡	V _{CC} = MAX		-30		-150	-30	-150	mA		
I _{CC}	Supply current (quiescent or triggered)	V _{CC} = MAX, See Note 2		‘LS122		6	11	6		11	mA
				‘LS123		12	20	12		20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k, C_{ext} = 0pF, R_{ext} = 5.0kΩ (See Fig. 3, page 2-61 and Fig. A, page 2-174)												
t _{PLH}	A	Q	25	37		22	33		25	37	ns	
	B		32	48		29	44		32	48		
t _{PHL}	A	Q̄	33	49		30	45		33	49	ns	
	B		40	61		37	56		40	61		
t _{PHL}	clear	Q	21	31		18	27		21	31	ns	
t _{PLH}		Q̄	33	50		30	45		33	50	ns	
tw _{Q(min)}	A or B	Q	140	250		116	200		140	250	ns	
*tw _Q	A or B	Q	-	-	-	4.0	4.5	5.0	-	-	μs	
Test Conditions: C_L = 50pF, R_L = 2.0k, C_{ext} = 0pF, R_{ext} = 5.0kΩ (See Fig. 3, page 2-61 and Fig. A, page 2-174)												
t _{PLH}	A	Q	30	43		26	38		30	43	ns	
	B		37	54		33	49		37	54		
t _{PHL}	A	Q̄	38	55		34	50		38	55	ns	
	B		45	67		41	62		45	67		
t _{PHL}	clear	Q	26	37		22	32		26	37	ns	
t _{PLH}		Q̄	39	55		35	50		39	55	ns	
tw _{Q(min)}	A or B	Q	155	270		127	240		155	270	ns	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

*For this test R_{ext} = 10kΩ, C_{ext} = 1000pF.

TYPICAL APPLICATION DATA

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF.

When $C_{ext} > 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \cdot R_T \cdot C_{ext}$$

where

R_T is in $k\Omega$ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in nanoseconds

For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.

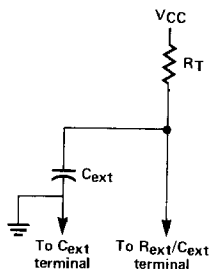


FIGURE 3
TIMING COMPONENT CONNECTIONS