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LXT915

Simple Quad Ethernet Repeater

General Description

The LXT915 is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10BASE-T transceivers. The AUI port allows connection of an external transceiver (10BASE-2, 10BASE-5, 10BASE-T or FOIRL) or a drop cable. The 10BASE-T transceivers are entirely self-contained with internal filters which simplify the design work required for FCC-compliant EMI performance.

An Inter-Repeater Backplane (IRB) interface allows 128 or more 10BASE-T ports to be cascaded, creating a large single-segment multi-port repeater.

The LXT915 requires only a single 5-volt power supply due to its advanced CMOS fabrication process.

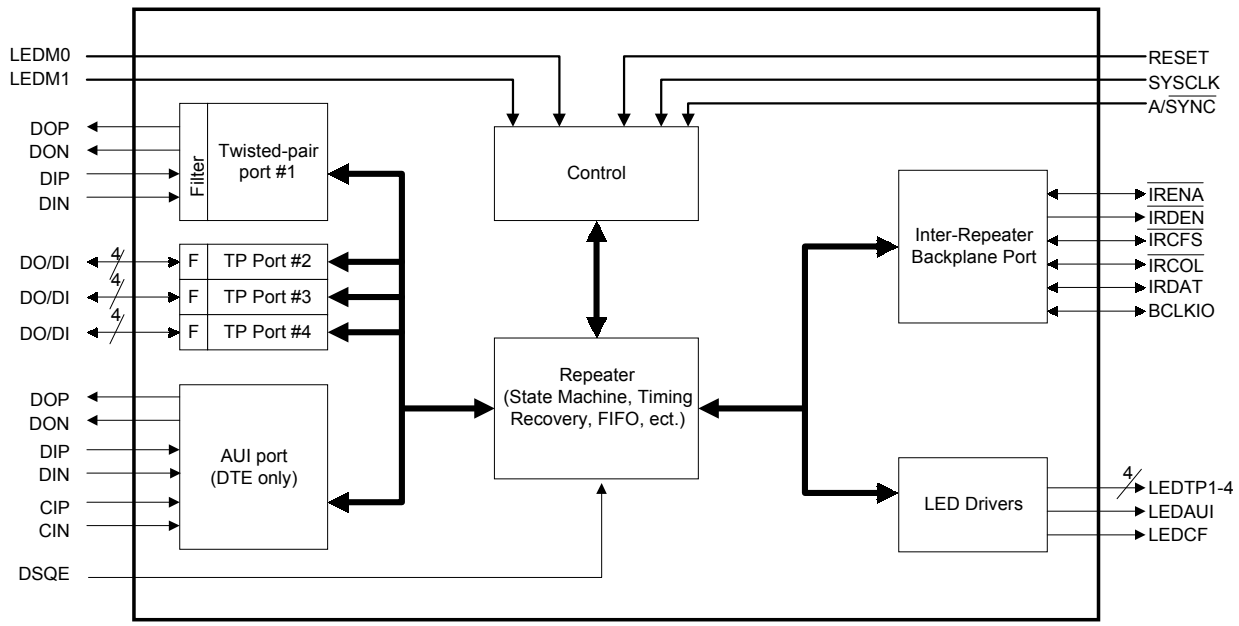
Features

- Four integrated 10BASE-T transceivers and one AUI transceiver on a single chip
- Six integrated LED drivers with four unique operational modes
- On-chip transmit and receive filtering
- Automatic polarity detection and correction
- Synchronous or asynchronous Inter-Repeater Backplane supports “hot swapping”
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10BASE-T ports
- Packaged in 64-pin PQFP

Applications

- Remote or Stand-alone Unmanaged Hubs
- Stackable Unmanaged Hubs

LXT915 Block Diagram



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LXT915 PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT915 Pin Assignments

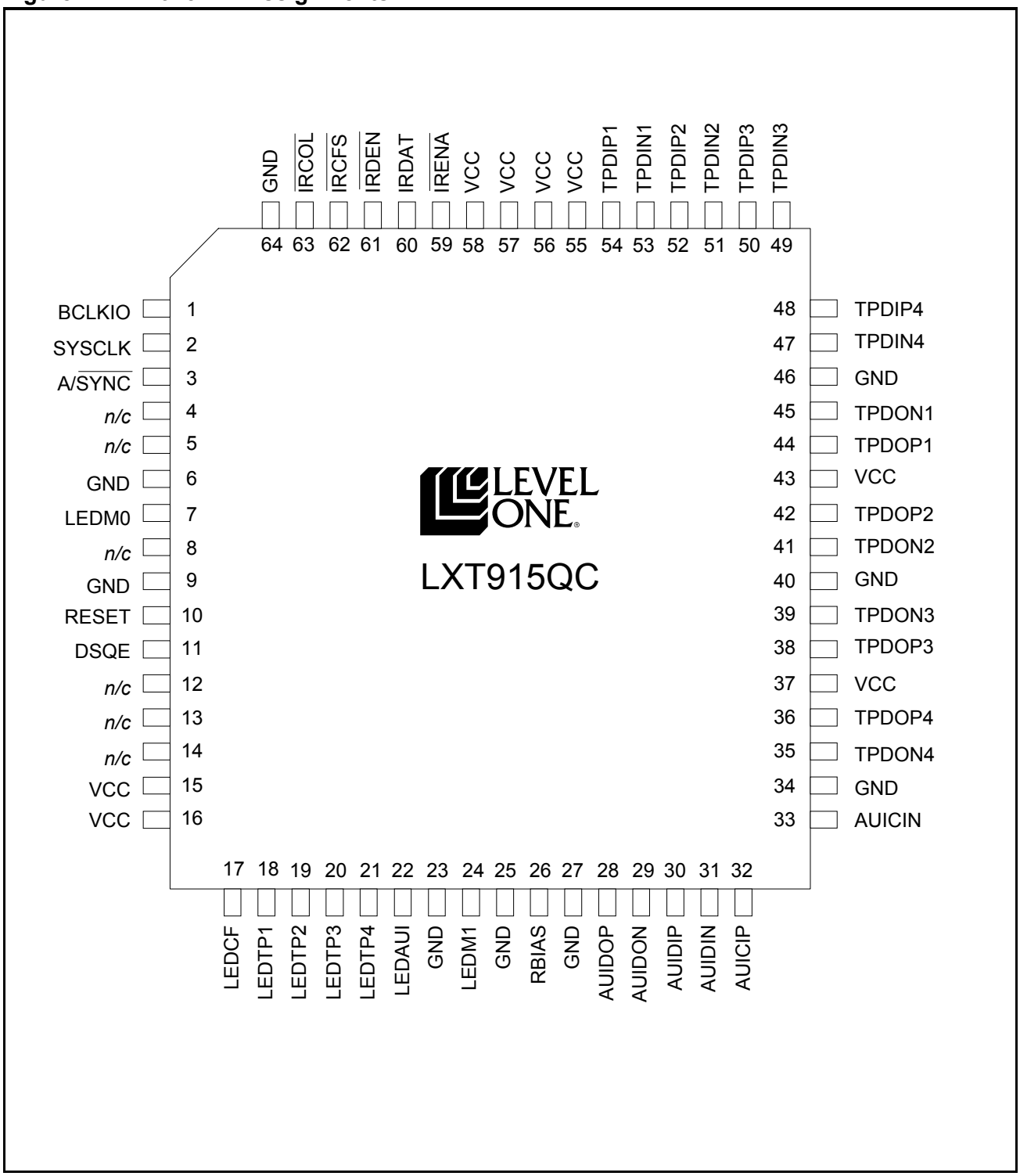


Table 1: Twisted-Pair Port Signal Descriptions

Pin	Symbol	I/O	Description
44 45 42 41 38 39 36 35	TPDOP1 TPDON1 TPDOP2 TPDON2 TPDOP3 TPDON3 TPDOP4 TPDON4	O O O O O O O O	**Twisted-Pair Data Outputs (Positive and Negative).** These pins are the positive (TPDOP1-4) and negative (TPDON1-4) outputs to the network from the respective twisted-pair ports.
54 53 52 51 50 49 48 47	TPDIP1 TPDIN1 TPDIP2 TPDIN2 TPDIP3 TPDIN3 TPDIP4 TPDIN4	I I I I I I I I	**Twisted-Pair Data Inputs (Positive and Negative).** These pins are the positive (TPDIP1-4) and negative (TPDIN1-4) inputs from the network to the respective twisted-pair ports.

Table 2: AUI Port Signal Descriptions

Pin	Symbol	I/O	Description
28 29	AUIDOP AUIDON	O O	**AUI Data Outputs (Positive and Negative)**. These pins are the positive and negative data outputs from the AUI port.
30 31	AUIDIP AUIDIN	I I	**AUI Data Inputs (Positive and Negative).** These pins are the positive and negative data inputs to the AUI port.
32 33	AUICIP AUICIN	I I	**AUI Collision Inputs (Positive and Negative).** These pins are the positive and negative collision inputs to the AUI port.

Table 3: Control, Status and Miscellaneous Signal Descriptions

Pin	Symbol	I/O	Description
2	SYSCLK	I	**System Clock**. The required 20 MHz system clock is input at this pin. Clock must have a 40-60 duty cycle with <10 ns rise time.
10	RESET	I	**Reset**. This pin resets the LXT915 internal circuitry when pulled or driven High for ≥ 1 ms.
11	DSQE	I	**Disable SQE.** When High the SQE function is disabled.
7 24	LEDM0 LEDM1	I I	**LED Mode Select 0 & 1.** These two pins select one of four possible modes of LED operation. The Functional Description section describes the four modes and Table 6 lists the four settings.

Table 3: Control, Status and Miscellaneous Signal Descriptions – continued

Pin	Symbol	I/O	Description
17	LEDCF	O	**Collision & FIFO Error LED Driver.** This tri-state LED driver pin reports collisions and FIFO errors. It pulses Low to report collisions, and pulses High to report FIFO errors. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT915 will simultaneously monitor and report both conditions independently.
18 19 20 21	LEDTP1 LEDTP2 LEDTP3 LEDTP4	O O O O	**TP Port LED Drivers.** These tri-state LED drivers use an alternating pulsed output to report TP port status. Each pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, each pin reports five separate conditions (receive, transmit, link integrity, reverse polarity and auto partition).
22	LEDAUI	O	**AUI Port LED Driver.** This tri-state LED driver uses an alternating pulsed output to report AUI port status. This pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, this pin reports five separate conditions (receive, transmit, receive jabber, receive collision and auto partition).
4 5 8 12 13 14	NC	_	**No Connects**. *Leave these pins unconnected (mandatory).*

Table 4: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	I/O	Description
1	BCLKIO	I/O	**Backplane Clock.** This 10 MHz clock synchronizes multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputting data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
3	A/$\overline{\text{SYNC}}$	I	**Backplane Synch Mode Select.** This pin selects the backplane synch mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/$\overline{\text{SYNC}}$ High). In the asynchronous mode 12 or more LXT915s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/$\overline{\text{SYNC}}$ tied Low), 32 or more LXT915s can be connected to the backplane and an external 10 MHz backplane clock source is required.
59	$\overline{\text{IRENA}}$	I/O	**Inter-Repeater Backplane Enable.** This pin allows individual LXT915 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The $\overline{\text{IRENA}}$ bus must be pulled up locally by a 330 Ω resistor.[1]

1. $\overline{\text{IRENA}}$ and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ cannot be buffered. In multi-board configurations, the total impedance on $\overline{\text{IRCOL}}$ should be no smaller than 330 W. $\overline{\text{IRCFS}}$ should be pulled up only once, by a single 330 Ω, 1% resistor.

Table 4: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	I/O	Description
60	IRDAT	I/O	**IRB Data.** This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be pulled up locally by a 330 Ω resistor.[1]
61	$\overline{\text{IRDEN}}$	O	**IRB Driver Enable.** The $\overline{\text{IRDEN}}$ pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active low signal, maintained for the duration of the data transmission. $\overline{\text{IRDEN}}$ must be pulled up locally by a 330 Ω resistor.
62 63	$\overline{\text{IRCFS}}$ $\overline{\text{IRCOL}}$	I/O I/O	**IRB Collision Flag Sense ($\overline{\text{IRCFS}}$) and IRB Collision ($\overline{\text{IRCOL}}$).** These two pins are used for collision signalling between multiple LXT915 devices on the IRB. Both the $\overline{\text{IRCFS}}$ bus and the $\overline{\text{IRCOL}}$ bus must be pulled up globally with 330 Ω resistors.[1] ($\overline{\text{IRCFS}}$ requires a precision resistor [±1%].)[2]

1. $\overline{\text{IRENA}}$ and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. $\overline{\text{IRCFS}}$ and $\overline{\text{IRCOL}}$ cannot be buffered. In multi-board configurations, the total impedance on $\overline{\text{IRCOL}}$ should be no smaller than 330 W. $\overline{\text{IRCFS}}$ should be pulled up only once, by a single 330 Ω, 1% resistor.

Table 5: LXT915 Power Supply Signal Descriptions

Pin	Symbol	I/O	Description
15 16 37 43 55 56 57 58	VCC	_	**Power Supply.** These pins each require a +5 VDC power supply. These various pins may be supplied from a single power source, but special de-coupling requirements may apply. Each VCC pin must be within ±0.3 V of every other VCC pin.
6 9 23 25 27 34 40 46 64	GND	_	**Ground.** These pins provide ground return paths for the various VCC power supply pins. *Connect these pins to external ground (mandatory).*
26	RBIAS	I	**Bias**. This pin provides bias current for internal circuitry. Connect this pin to ground through an external 12.4k 1% resistor.

FUNCTIONAL DESCRIPTION

Introduction

The LXT915 is an integrated hub repeater for 10BASE-T networks. The hub repeater is the central point for information transfer across the network. The LXT915 offers multiple operating modes to suit a broad range of applications from simple 4-, 8- or 16-port stand-alone models up to 128-port stackable hubs.

The main functions of the LXT915 hub repeater are data recovery and retransmission and collision propagation. Data packets received at the AUI or 10BASE-T ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for retiming and retransmission. Data packets received through the IRB port are essentially passed directly to the core for retransmission. After recovery of a valid data packet, the repeater broadcasts it to all enabled stations, except the originator station.

External Interfaces

The LXT915 includes four 10BASE-T ports with internal filters. The LXT915 also includes an Attachment Unit Interface (AUI) port and an Inter-Repeater Backplane (IRB) port. The IRB port enables multiple LXT915 devices to be interconnected, creating a large, single-segment, multi-port repeater.

10BASE-T Ports

The four 10BASE-T transceiver ports are completely self-contained. Since the transmitters and receivers include the required filtering, only simple, inexpensive transformers are required to complete the 10BASE-T interface. Each individual Twisted-Pair (TP) port is implemented in accordance with the IEEE 802.3 10BASE-T standard. Refer to Table 1 for TP Port signal descriptions.

AUI Port

The AUI port operates in standard DTE mode and allows connection of an external transceiver (10BASE-2, 10BASE-5, 10BASE-T or FOIRL) or a drop cable. Refer to Table 2 for AUI Port signal descriptions.

Inter-Repeater Backplane

The Inter-Repeater Backplane (IRB) allows several LXT915s to function as a single repeater. The IRB also allows several multi-repeater boards to be integrated in a standard rack and to function as a single unit. The IRB supports “hot swapping” for easy maintenance and troubleshooting. Each individual repeater distributes recovered and retimed data to other repeaters on the IRB for broadcast on all ports simultaneously. This simultaneous rebroadcast allows the multi-repeater system to act as a single large repeater unit. The maximum number of repeaters on the IRB is limited by bus loading factors such as parasitic capacitance. The IRB can be operated synchronously or asynchronously. Refer to Table 3 for control signals and to Table 4 for IRB signal descriptions.

Synchronous IRB Operation

In the synchronous mode, a common external source provides the 10 MHz backplane clock (BCLKIO) and the 20 MHz system clock (SYSCLK) to all repeaters. (BCLKIO must be synchronous to SYSCLK and may be derived from SYSCLK using a divide-by-two circuit.) In the synchronous mode 32 or more LXT915 repeaters may be connected on the IRB, providing 128 10BASE-T ports and 32 AUI ports.

Asynchronous IRB Operation

In the asynchronous mode an external BCLKIO source is not required. The repeaters run independently until one takes control of the IRB. The transmitting repeater then outputs its own 10 MHz clock onto the BCLKIO line. All other repeaters sync to that clock for the duration of the transmission. In the asynchronous mode 12 or more LXT915 devices may be connected to the IRB, providing 48 10BASE-T ports and 12 AUI ports.

NOTE

The maximum number of repeaters which may be linked on the backplane is limited by board design factors. The numbers listed above are engineering estimates only. Stronger drivers and reduced capacitive loading in PCB layout may allow an increased device count.

Internal Repeater Circuitry

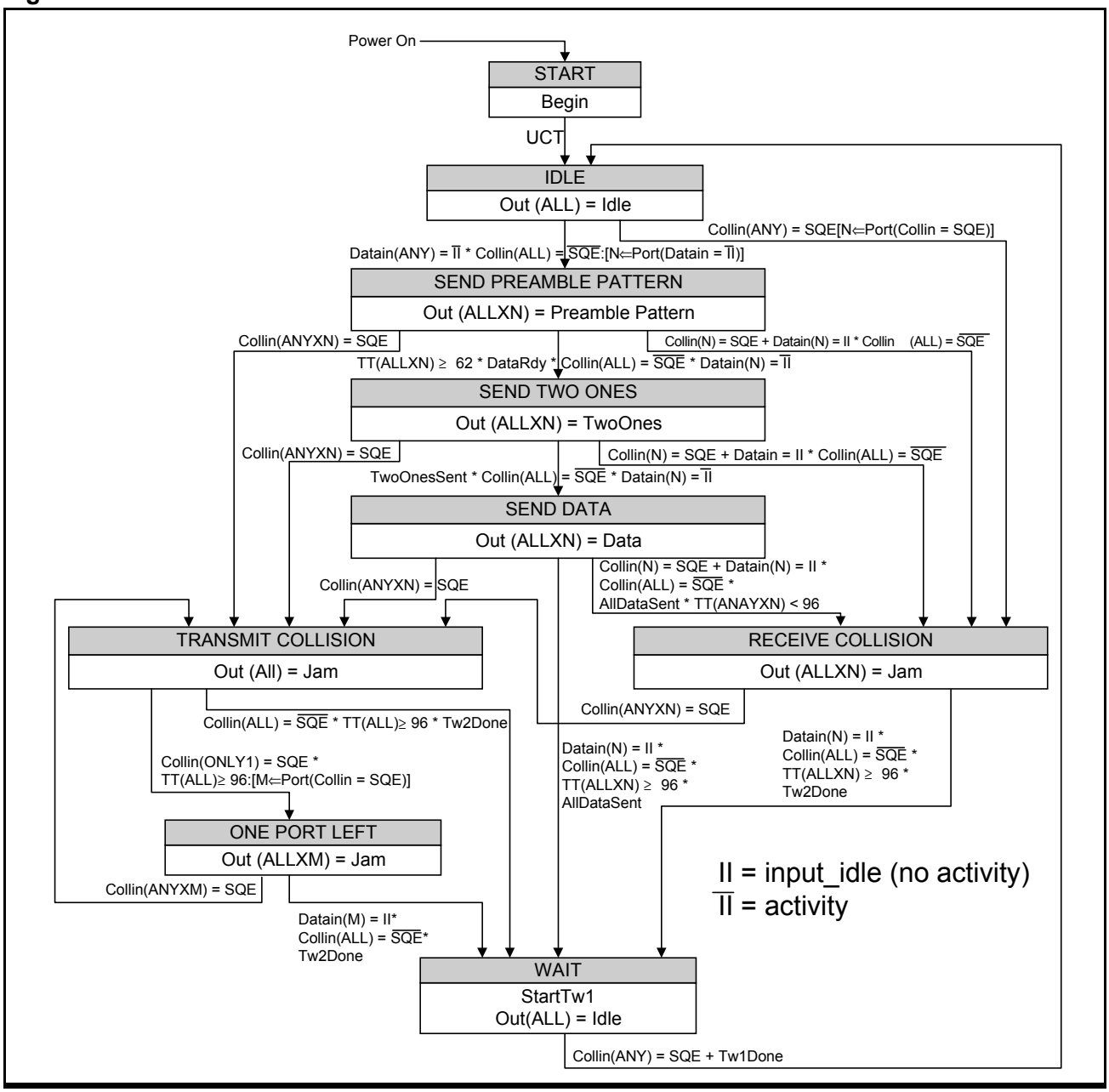
The basic repeater circuitry is shared among all the ports within the LXT915. It consists of a global repeater state machine, several timers and counters and the timing recovery circuit. The timing recovery circuit includes a FIFO for retiming and recovery of the clock which is used to clock the receive data out onto the IRB.

The shared functional blocks of the LXT915 are controlled by the global state machine shown in Figure 2. This diagram and all associated notations used are in strict accordance with section 9.6 of the IEEE 802.3 standard.

The LXT915 also implements the Partition State Diagram as defined by the IEEE 802.3 standard and shown in Figure 3. The value of CCLIMIT as implemented in the LXT915 is 64.

The CCLIMIT value sets the number of consecutive collisions that must occur before the port is subjected to automatic partitioning. Auto-partition/reconnection is also supported by the LXT915 with Tw5 conforming to the standard requirement of 450 to 560 bit times.

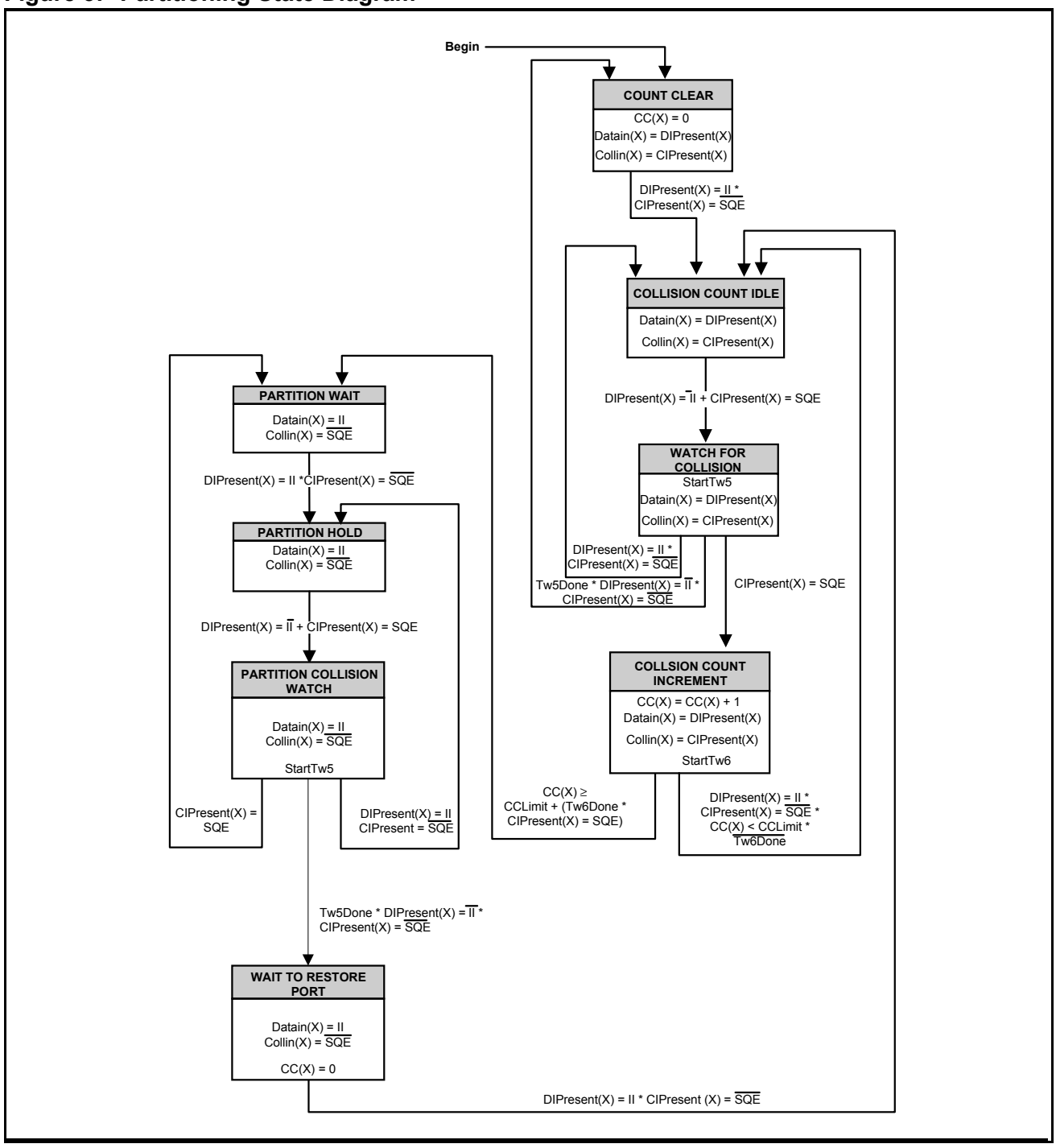
Figure 2: Global State Machine



Initialization

The following description applies to the initial power-on reset and to any subsequent hardware reset. When a reset occurs (RESET pin pulled high for > 1 ms), the device senses the levels at the various control pins (see Tables 3 and 4) to determine the correct operating modes for the LEDs and the IRB.

Figure 3: Partitioning State Diagram



10BASE-T Port Operation

10BASE-T Reception

Each LXT915 10BASE-T port receiver acquires data packets from its twisted-pair input (DIP/DIN). An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. No external filters are required. The receive function is activated only by valid data streams (above the squelch level and with proper timing). If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the port receiver enters the idle state.

Polarity Detection and Correction

The LXT915 10BASE-T ports detect and correct for reversed polarity by monitoring link pulses and end-of-frame sequences. A reversed polarity condition is declared when the port receives sixteen or more incorrect link pulses consecutively, or four frames with reversed start-of-idle sequence. In these cases the receiver reverses the polarity of the signal and thereby corrects for this failure condition. If the port enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.)

10BASE-T Link Integrity Testing

The LXT915 fully supports the 10BASE-T Link Integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. The receiver recognizes link integrity pulses transmitted in the absence of data traffic. With no data packets or link integrity pulses within 100 (±50) ms, the port enters a link fail state and disables its transmitter. The port remains in the link fail state until it detects three or more data packets or link integrity pulses.

10BASE-T Transmission

Each LXT915 10BASE-T port receives NRZ data from the repeater core and passes it through a Manchester encoder. The encoded data is then transmitted to the twisted-pair network (the DO circuit). The advanced integrated pulse shaping and filtering network produces the pre-distorted and pre-filtered output signal to meet the 10 Base-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance.

During idle periods, the LXT915 10BASE-T ports transmit link integrity test pulses in accordance with the 802.3 10BASE-T standard.

Data packets transmitted by the LXT915 contain a minimum of 56 preamble bits before the start of frame delimiter (SFD). In the Asynchronous mode, preamble regeneration takes place on the transmit side. In the Synchronous mode, the preamble is regenerated on the receive side and distributed via the IRB. If the total packet is less than 96 bits including the preamble, the LXT915 extends the packet length to 96 bits by appending a Jam signal (1010...) at the end.

AUI Port Operation

AUI Reception

The LXT915 AUI port receiver acquires data packets from the network (DIP/DIN). Only valid data streams above the squelch level activate the receive function. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the AUI receiver enters the idle state.

AUI Transmission

The LXT915 AUI port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data then goes out on the network (DOP/DON).

Collision Handling

A collision occurs when two or more repeater ports receive simultaneously, or when the AUI CIP/CIN signal is active. The LXT915 fully complies with the IEEE 802.3 collision specifications, both in individual and multi-repeater applications. In multiple-repeater configurations, collision signaling on the IRB allows all repeaters to share collision parameters, acting as a single large repeater.

$\overline{\text{IRCOL}}$ is a digital open-drain pin. $\overline{\text{IRCFS}}$ is an analog/digital port. The $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ lines are pulled up globally (i.e., each signal requires one pull-up resistor for all boards). If there are eight 3-repeater boards in the system, all eight boards share a single pull-up resistor for $\overline{\text{IRCOL}}$ and a single pull-up resistor for $\overline{\text{IRCFS}}$. The global pull-up may be located on one of the boards, or on the backplane. The $\overline{\text{IRCFS}}$ line requires a precision (± 1%) resistor.

The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ lines are each pulled up locally (one pull-up resistor per board) if external bus drivers are used. If no bus drivers are used then only one global pull-up per signal is used.

LED Display

The LED display interface consists of seven integrated LED drivers, one for each of the five network ports and two for common functions. Each pin provides a three-state pulsed output (+5 V, high Z, and 0 V) which allows multiple conditions to be monitored and reported independently. Table 6 shows the LED Mode selected with each LEDM1 and LEDM0 combination. Figure 4 shows the LED Driver output conditions and Tables 7 through 10 list the repeater states associated with each of the five conditions.

LED Mode 0 (Default)

This mode is selected when LEDM1 and LEDM0 are floated or pulled low. Refer to Table 7.

LED Mode 1

This mode is selected when LEDM1 is tied, floated or pulled low and LEDM0 is pulled high by a pull-up resistor. Refer to Table 8.

LED Mode 2

This mode is selected when LEDM1 is pulled high by a pull-up resistor and LEDM0 is floated or pulled low. Refer to Table 9.

LED Mode 3

This mode is selected when LEDM1 is pulled high by a pull-up resistor and LEDM0 is also pulled high by a pull-up resistor. Refer to Table 10.

Table 6: LED Mode Selection

LEDM1 Pin 24	LEDM0 Pin 7	LED Mode Selected
0	0	0 (default)
0	1	1
1	0	2
1	1	3

Table 7: Mode 0 LED Truth Table (Default)

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	FIFO Error
2	Tx Packet	Tx Packet	N/A
3	Reversed Polarity	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	Partitioned Out	Partitioned Out	N/A

Table 8: Mode 1 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	N/A	N/A	N/A
3	N/A	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	N/A	N/A	N/A

Table 9: Mode 2 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	Partitioned Out	Partitioned Out	N/A
3	N/A	N/A	Collision
4	Rx Packet	Rx Packet	N/A
5	N/A	N/A	N/A

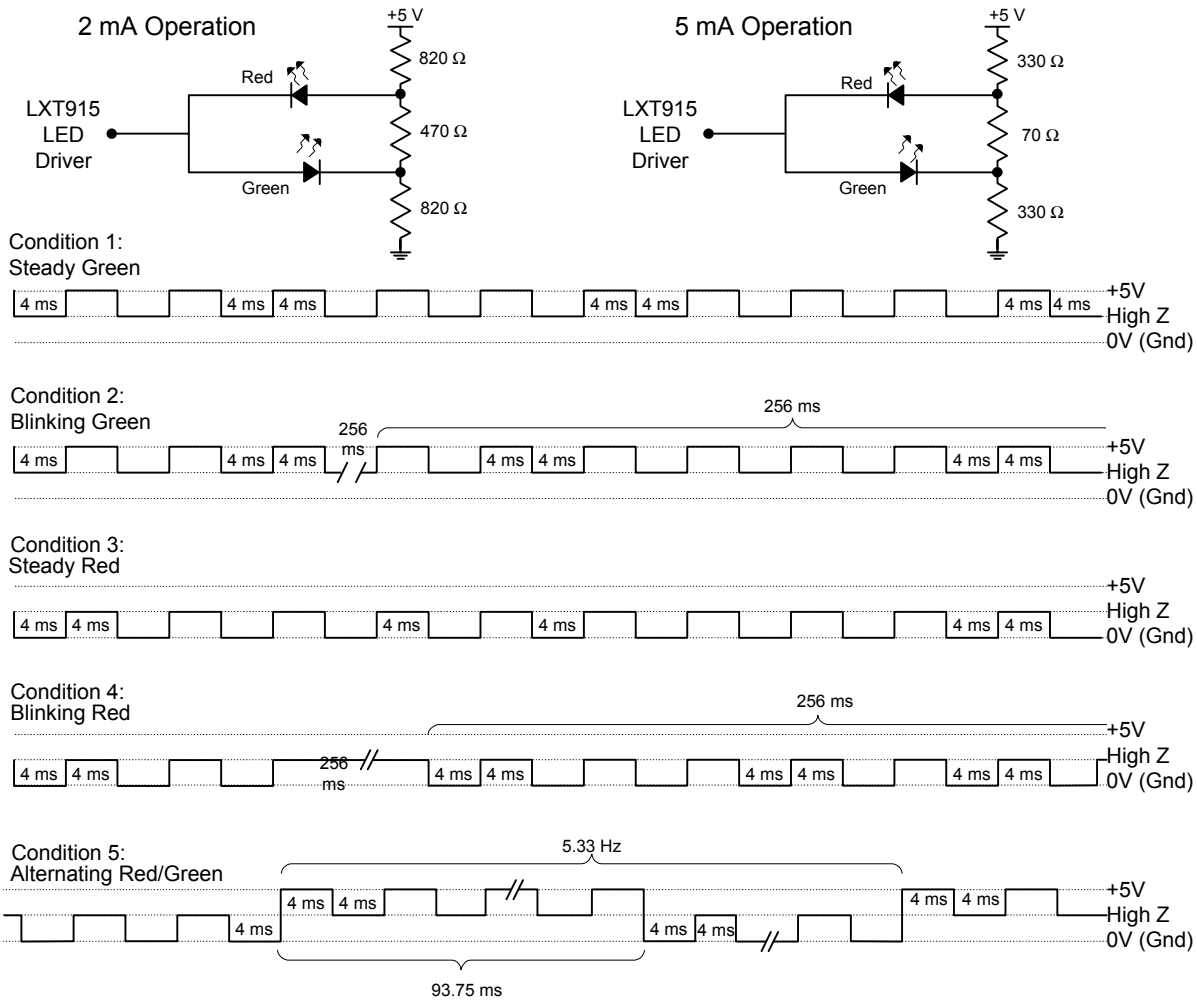
Table 10: Mode 3 LED Truth Table

Condition	LEDTP 1-4	LEDAUI	LEDCF
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)
2	Rx Packet	Rx Packet	N/A
3	Partitioned Out	Partitioned Out	Collision
4	N/A	N/A	N/A
5	N/A	N/A	N/A

Figure 4: Integrated LED Driver Indications

NOTE

The drivers are capable of driving a 10 mA load. The signal is pulsed every 4 ms, making the average current approximately 5 mA.



APPLICATION INFORMATION

Layout Requirements

The Twisted Pair Interface

The four, twisted-pair output circuits are identical. Each TPDOP/TDPON signal has a 24.9 Ω, 1%, series resistor and a 120 pF capacitor differentially across the positive and negative outputs. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TDPIN signals have a 100 Ω resistor across the positive and negative input signals to terminate the 100 Ω signal received from the line. To calculate the impedance on the output line interface, use:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

The layout of the twisted-pair ports is critical in complex designs. Run the signals directly from the device to the discrete termination components (located close to the transformers).

The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes from the transformers to the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers of the LXT915. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals. The LXT915 requires a 12.4 kΩ, 1% resistor directly connected to RBIAS at pin 26. This connection should be as short as possible. The ground rails from pins 25 & 27 should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Unmanaged Hub Application

Figure 5 shows an eight-port unmanaged hub application. The application shows a pair of LXT915s connected using the Asynchronous IRB mode.

Figure 5 (Sheet 1) has the LXT915 set up with the LEDs in Mode 1 with one link LED per port and a single collision LED. In LED Mode 1, the twisted pair port LEDs display link integrity only (refer to Table 8). LED Mode 1 is selected by pulling LEDM0 High with a 1 kΩ resistor on pin 7 and pulling LEDM1 Low with pin 24 attached to ground.

Figure 5 (Sheet 2) shows the second LXT915 set up in the same LED Mode (Mode 1). The AC/DC plug and regulator circuits are commonly used in remote hub applications.

The VCC and GND pins are at the bottom of each diagram. All VCC pins use a single power supply with decoupling capacitors installed between the VCC and GND pins and their respective planes.

Figure 5: LXT915 8-Port Unmanaged Hub Application, LED Mode 1 Selected (sheet 1 of 2)

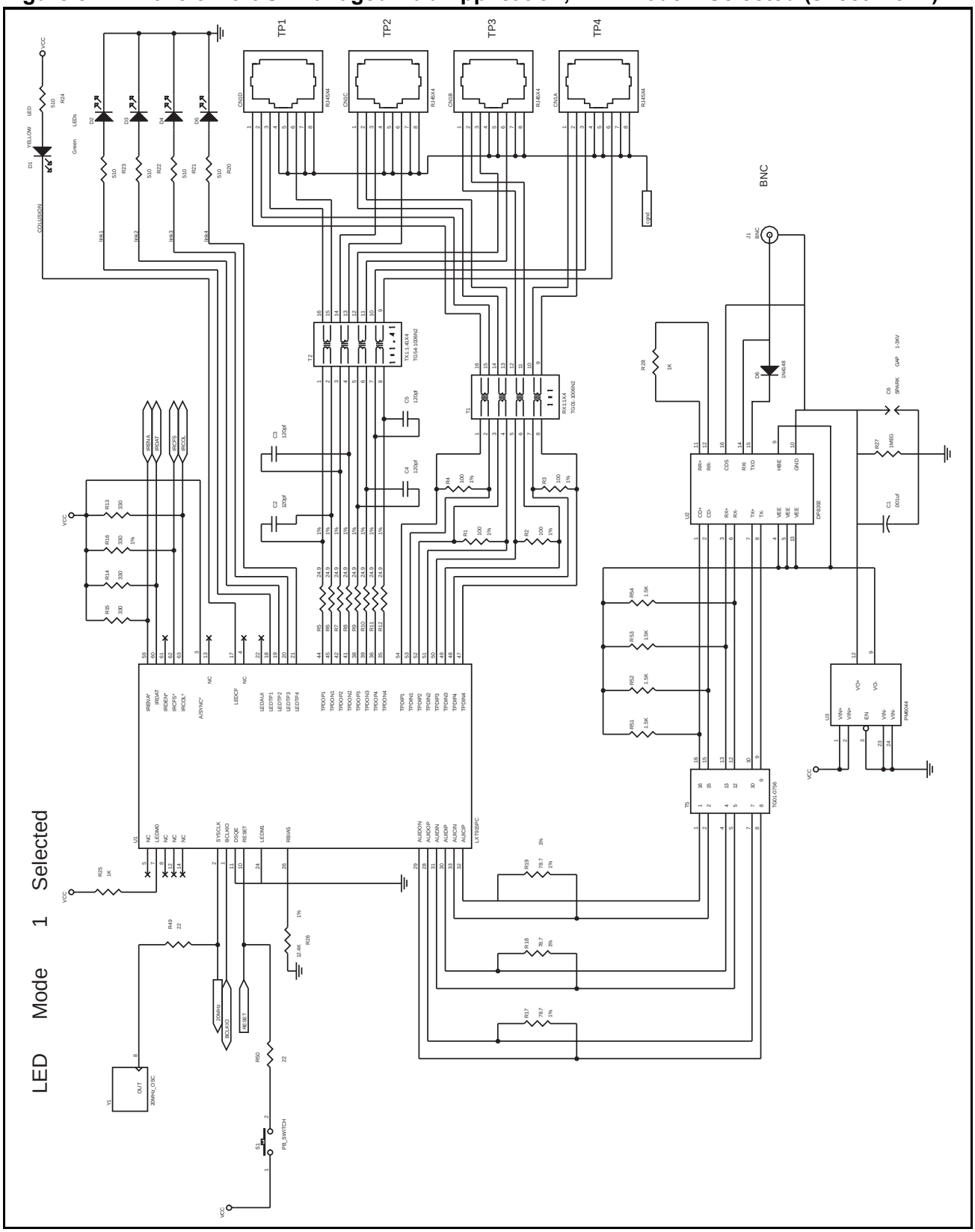
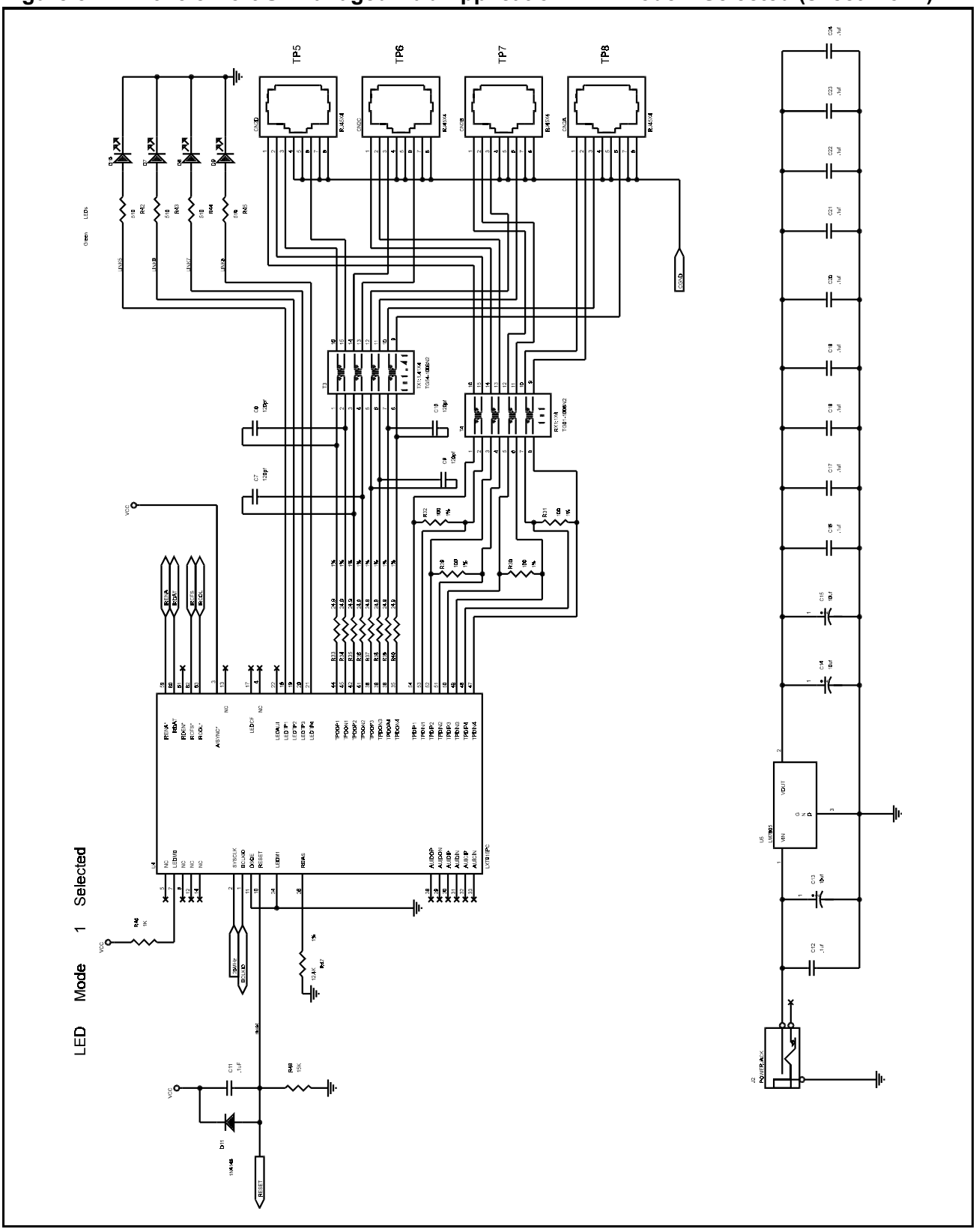


Figure 5: LXT915 8-Port Unmanaged Hub Application LED Mode 1 Selected (sheet 2 of 2)



Magnetics Requirements

The Twisted Pair Interface

The LXT915 requires transformers with a 1:1 ratio for the receive pairs and 1:$\sqrt{2}$ on the transmit pairs. The transformer isolation voltage should be rated at 2 KV to protect the circuitry from static voltages across the connectors and cables. Magnetics suitable for the LXT915 are currently available, and are used on the LXT914 Quad Repeater. Available magnetics include the following options:

- simple per-port Rx/Tx pair transformers
- receive quad transformers and transmit quad transformers
- single 40 pin octal transformers

Component Selection

Table 11 is a list of available Quad and Single port transformers with manufacturers and part numbers. This information was valid as of the printing date of this document. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application.

Table 11: Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Quad Port Tx/Rx
BEL	S553-5999-02	S553-5999-03	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TG44-S010NX TG45-S010NX TG46-S010NX
Nanopulse	5976	5977	
Kappa	TP4003P	TP497P101	
PCA	EPE6009	EPE6010	
TDK	TLA-3T107	TLA-3T106	
VALOR	PT4116	PT4117	

LXT915 TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Tables 12 through 19 and Figure 6 represents the performance specifications of the LXT915 and are guaranteed by test except, where noted, by design

.

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VCC	-0.3	–	6	V
Operating temperature	TOP	0	–	+70	° C
Storage temperature	TST	-65	–	+150	° C

NOTE

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage	VCC	4.75	5.0	5.25	V
Recommended operating temperature	TOP	0	–	70	° C

Table 14: I/O Electrical Characteristics[1] (over recommended range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Supply current	ICC	–	–	180	mA	
Input Low voltage	VIL	–	–	0.8	V	
Input Low voltage (RESET)	$V_{ILRESET}$	–	–	0.8	V	V_{CC} = 5.25 V
Input High voltage	$V_{IHRESET}$	4.0	–	–	V	V_{CC} = 4.75 V
Input High voltage (RESET)	VIH	2.0	–	–	V	
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage	VOL	–	–	10	% V_{CC}	IOL < 10 µA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 5 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA

1. Not applicable to IRB signals; IRB electrical characteristics are specified in Table 17.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 14: I/O Electrical Characteristics[1] (over recommended range) – continued

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Output High voltage	VOH	90	–	–	% V_{CC}	IOH < 10 µA
Output High voltage (LED)	VOHL	4	–	–	V	IOHL = -5 mA
Input Low current	IIL	–	–	2	mA	VOL = .4 V
Output rise / fall time	–	–	3	8	ns	CLOAD = 20 pF
RESET pulse width	PWRESET	1.0	–	–	ms	V_{CC} = 4.75 V
RESET fall time	TFRESET	–	–	20.0	µs	VIHRESET to VILRESET

1. Not applicable to IRB signals; IRB electrical characteristics are specified in Table 17.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 15: AUI Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	IIL	–	–	-700	µA	
Input High current	IIH	–	–	500	µA	
Differential output voltage	VOD	±550	–	±1200	mV	
Receive input impedance	ZIN	–	20	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	VDS	–	220	–	mV	

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and no subject to production testing.

Table 16: TP Electrical Characteristics (over recommended range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	5	–	Ω	
Peak differential output voltage	VOD	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition	–	–	± 6.4	± 10	ns	0 line length
Transmit timing jitter added by the MAU and PLS sections[2]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T
Receive input impedance	ZIN	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	VDS	300	420	565	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.
2. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 17: IRB Electrical Characteristics (over recommended range)

Parameter	Sym	Min.	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	0.3	0.6	V	
Output rise or fall time	TRF	–	4	12	ns	
Input Low voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VILIRB	–	–	0.8	V	RL = 330Ω
Input High voltage: $\overline{\text{IRENA}}$, $\overline{\text{IRCOL}}$ & IRDAT	VIHIRB	3.0	–	–	V	RL = 330Ω
Input Low voltage: BCLKIO	VILBCLK	–	–	0.4	V	RL = 330Ω
Input High voltage: BCLKIO	VIHBCLK	4.0	–	–	V	RL = 330Ω

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 18: Switching Characteristics (over recommended range)

Parameter		Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time	5.0	–	5.5	ms
	Unjab time	–	9.6	–	µs
Link Integrity Timing	Time link loss	–	60	–	ms
	Time between Link Integrity Pulses	10	–	20	ms
	Interval for valid receive Link Integrity Pulses	4.1	–	30	ms

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 6: Inter-Repeater Bus Timing

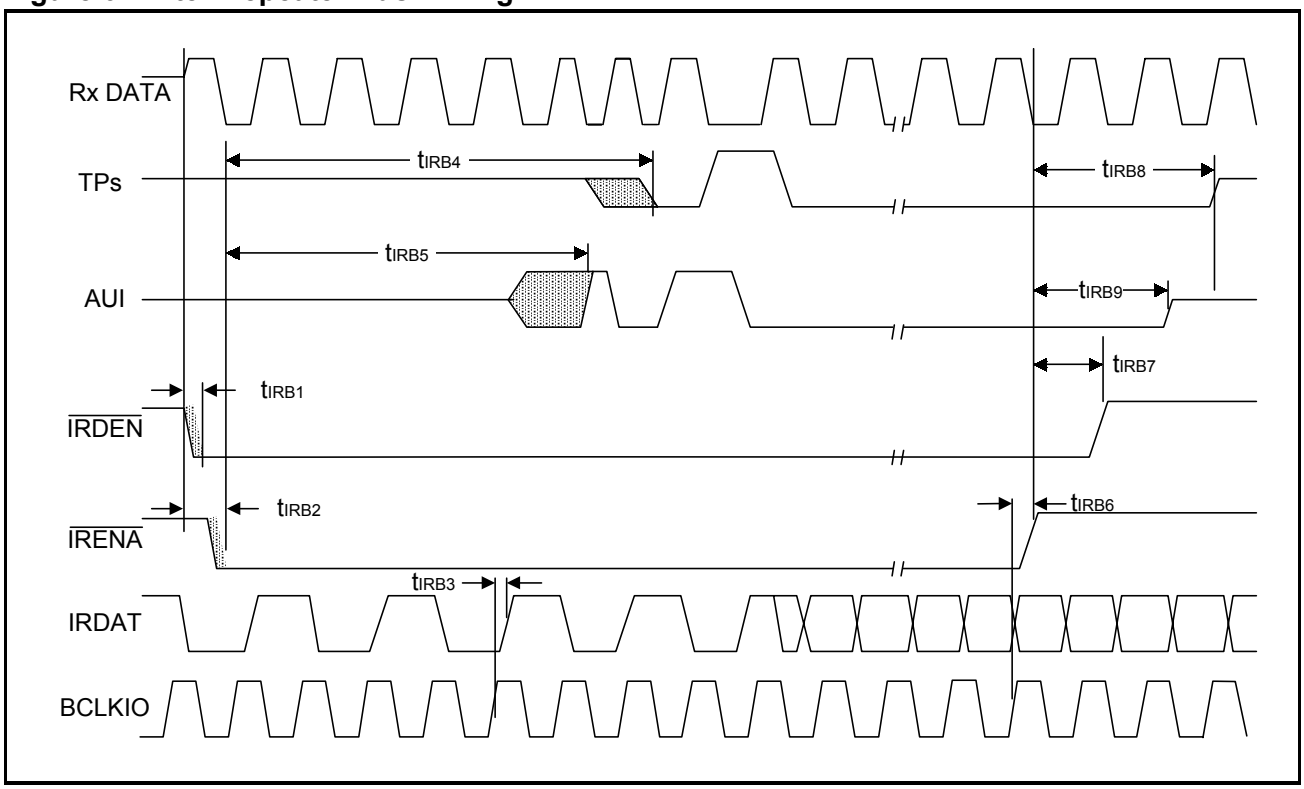


Table 19: Inter-Repeater Bus Timing (over recommended range)

Parameter	Symbol	Min	Typical[1]	Max.	Units
Start of Frame to $\overline{\text{IRDEN}}$ Low (active)	tIRB1	10	–	150	ns
Start of Frame to $\overline{\text{IRENA}}$ Low (active)	tIRB2	125	–	225	ns
BCLKIO to IRDAT valid (Synchronous mode)	tIRB3	5	–	30	ns
BCLKIO to IRDAT valid (Asynchronous mode)	tIRB3	–	50	–	ns
$\overline{\text{IRENA}}$ Low (active) to TP outputs active	tIRB4	525	–	600	ns
$\overline{\text{IRENA}}$ Low (active) to AUI output active	tIRB5	475	–	525	ns
End of Frame clock to $\overline{\text{IRENA}}$ High (inactive)	tIRB6	5	–	30	ns
$\overline{\text{IRENA}}$ High (inactive) to $\overline{\text{IRDEN}}$ High (inactive)	tIRB7	95	–	105	ns
$\overline{\text{IRENA}}$ High (inactive) to TP outputs inactive	tIRB8	575	–	600	ns
$\overline{\text{IRENA}}$ High (inactive) to AUI output inactive	tIRB9	425	–	450	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.