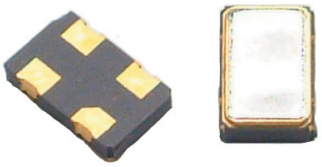
SaRonix™
A PERICOM® COMPANY

S1633 Series

3.3V CMOS Low Jitter Crystal Clock Oscillator (XO)



Actual Size = 3.2 x 5mm

Product Features

- Less than 1.5 ps RMS jitter with fundamental or overtone design
- 3.3V CMOS/TTL compatible logic levels
- Pin-compatible with standard 3.2x5mm packages
- Designed for standard reflow and washing techniques
- Low power standby mode
- Pb-free and RoHS/Green compliant

Product Description

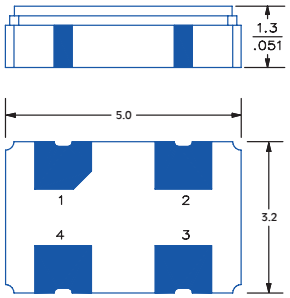
The S1633 Series is a 3.3V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS/LVTTL logic levels. The device, available on tape and reel, is contained in a 3.2x5mm surface-mount ceramic package.

Applications

The S1633 Series is an ideal reference clock for compact, high-density applications requiring low jitter or tight stability, including:

- Ethernet
- FibreChannel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- T1/E1, T3/E3 linecards
- DSLAM
- 802.11a/b/g WiFi

Packaging Outline



Pin Functions

Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V_{DD}

Common Frequencies

Contact SaRonix for additional frequencies

2.0480 MHz	24.5760 MHz	60.0000 MHz
3.6864 MHz	25.0000 MHz	66.0000 MHz
8.0000 MHz	27.0000 MHz	66.6667 MHz
10.0000 MHz	32.0000 MHz	75.0000 MHz
14.3181 MHz	33.0000 MHz	80.0000 MHz
16.0000 MHz	40.0000 MHz	90.0000 MHz
16.3840 MHz	44.0000 MHz	100.0000 MHz
19.4400 MHz	48.0000 MHz	106.2500 MHz
20.0000 MHz	50.0000 MHz	125.0000 MHz
22.0000 MHz		

Ordering Information

S 1633 B - 125.000 (T)

- **SaRonix**
- **Product Series**
- **Frequency Stability**
  *A = ±25 ppM (-20 to +70 °C)
  B = ±50 ppM (-20 to +70 °C)
  E = ±50 ppM (-40 to +85°C)
- **Output Frequency** (MHz)
- **Packaging**
  (T) = Tape & Reel full reel increments
  Blank = Bulk packaged

* Availability varies by frequency.

Electrical Performance

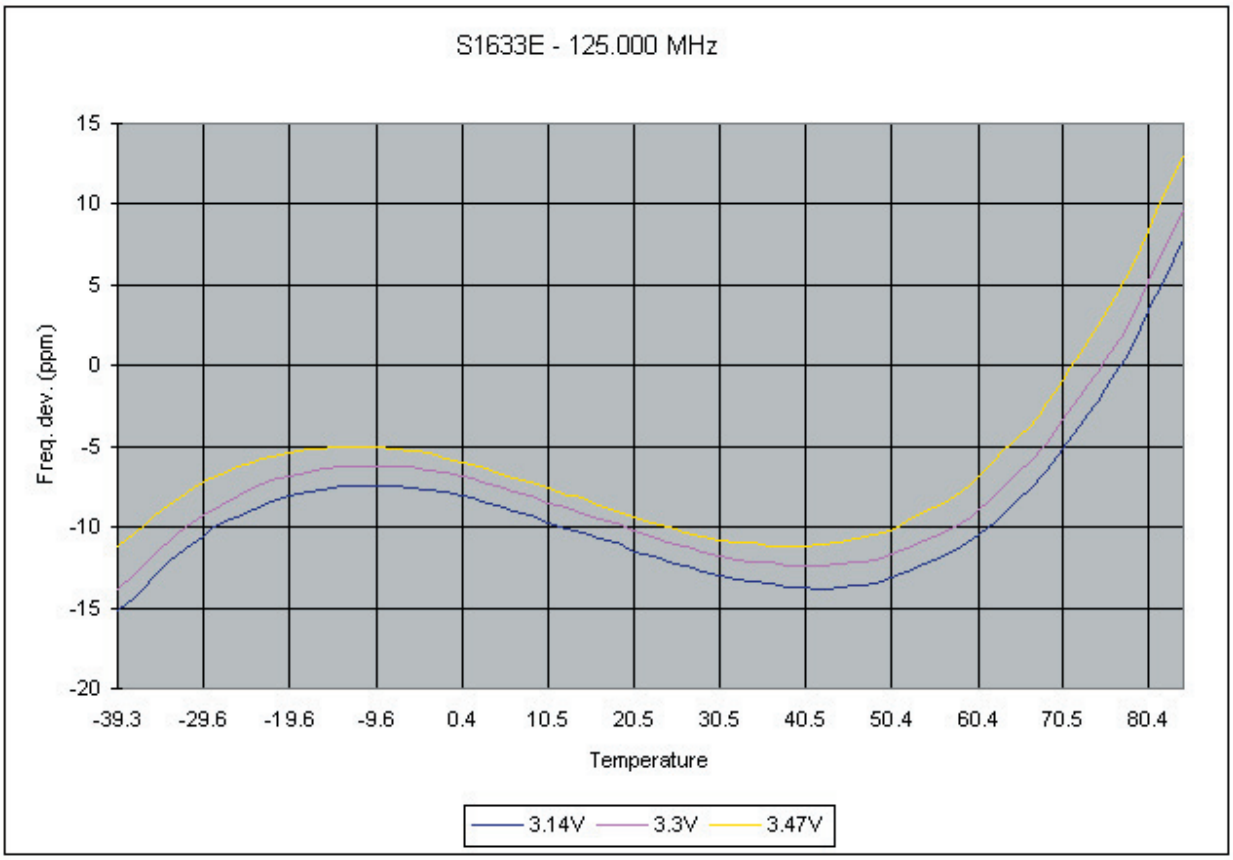
Parameter		Min.	Typ.	Max.	Units	Notes
Output frequency		1.8432		125	MHz	As specified
Supply voltage		+3.135	+3.3	+3.465	V	
Supply current, output enabled				15	mA	1.8432 to <40 MHz
				12		40 to 50 MHz
				25		>50 to <60 MHz
				40		60 to <80 MHz
				55	mA	80 to 125 MHz
Supply current, standby mode				10	µA	Output Hi-Z
Frequency stability				±25 to ±50	ppM	See Note 1 below
Operating temperature		-40		+85	°C	As specified
Output logic 0, VOL				10% V_{DD}	V	
Output logic 1, VOH		90% V_{DD}			V	
Output load		15 pF (max) or 10 LSTTL				
Duty cycle (1.8432 to 79.9999 MHz)		45		55	%	-40 to +85°C measured 50%VDD
Duty cycle (80 to 125 MHz)		45		55	%	-20 to +70°C measured 50%VDD
Duty cycle (80 to 125 MHz)		40		60	%	-40 to +85°C measured 50%VDD
Rise and fall time	<40 MHz			7	ns	measured 20/80% of waveform
	40 to <80 MHz			5		
	80 to 125 MHz			3		
Jitter, Phase	up to <80 MHz			1.5	ps RMS (1-σ)	10kHz to 20 MHz frequency band
	80 to 125 MHz			1		
Jitter, Accumulated	up to <80 MHz			5	ps RMS (1-σ)	20.000 adjacent periods
	80 to 125 MHz			3		
Jitter, Total	up to <80 MHz			50	ps pk-pk	100.000 random periods
	80 to 125 MHz			30		

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	2.2			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.8	V	Output is Hi-Z
Internal pullup resistance	50			kΩ	
Output disable delay			100	ns	
Output enable delay			10	ms	

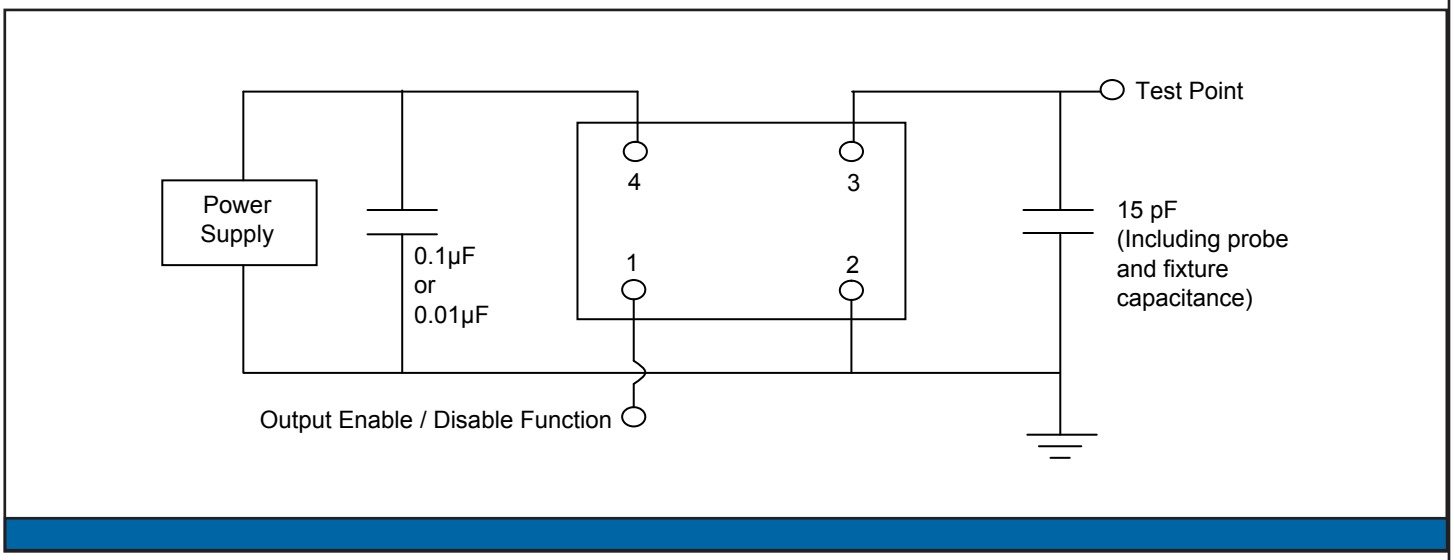
Typical Frequency Stability



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

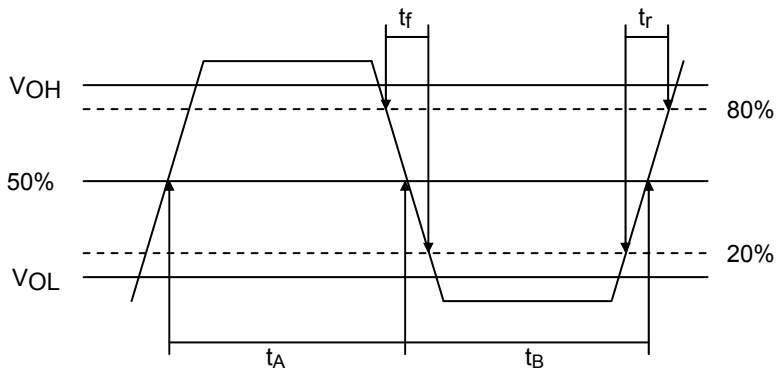


Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

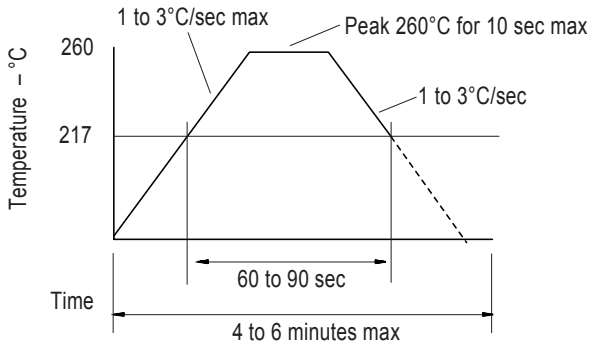
Output Waveform



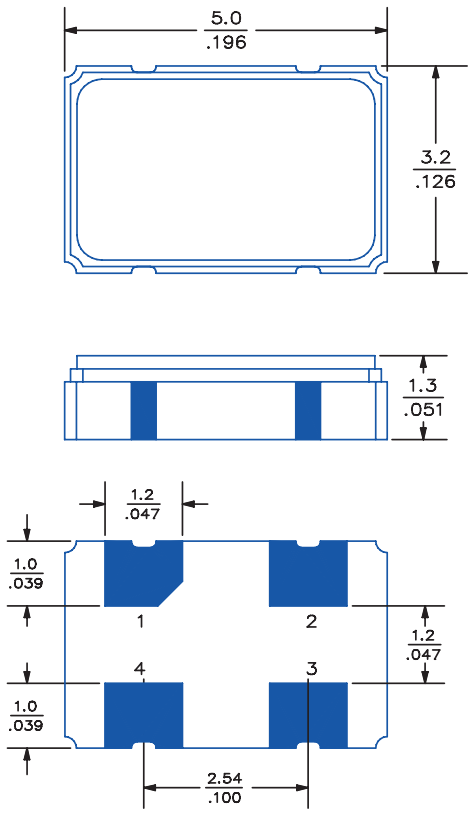
Duty cycle = 100% × (t_A) / (t_A + t_B)

Reflow Soldering Profile

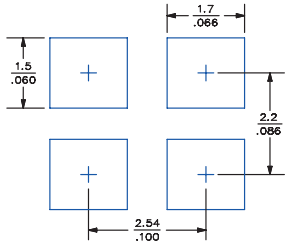
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1:	**S 3 X**	**(SaRonix, Model, Stability code)**
Marking LINE 2:	**Frequency**	**(Frequency code)**
Marking LINE 3:	**● YY WW X**	**(Pin 1, Year, Week, Origin)**

**Exact location of markings may vary.