

# Digital Step Attenuator

50Ω DC-2400 MHz

31.5 dB, 0.5 dB Step

6 Bit, Parallel Control Interface, Dual Supply Voltage

## Product Features

- Dual Supply Voltage:  $V_{DD}=+3V$ ,  $V_{SS}=-3V$
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Parallel control interface
- Fast switching control frequency, 1 MHz typ.
- Low Insertion Loss
- High IP3, +52 dBm Typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm



**DAT-31R5-PN+**  
**DAT-31R5-PN**

+ RoHS compliant in accordance  
with EU Directive (2002/95/EC)

The +suffix identifies RoHS Compliance. See our web site for  
RoHS Compliance methodologies and qualifications.

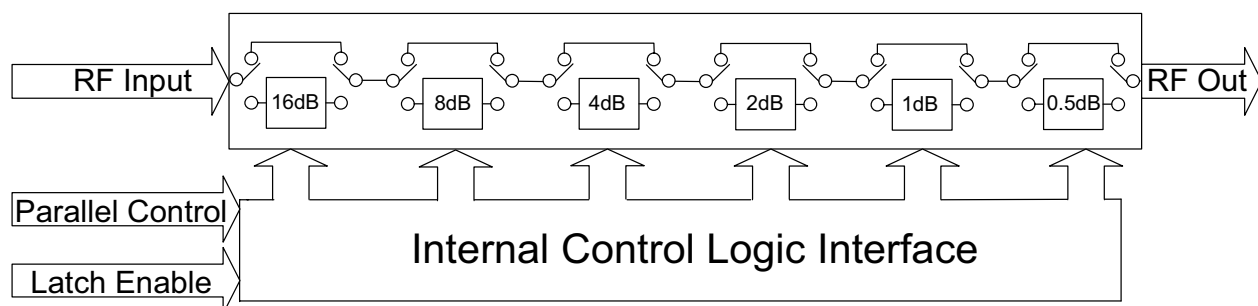
## Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

## General Description

The DAT-31R5-PN is a 50Ω RF digital step attenuator that offers an attenuation range up to 31.5 dB in 0.5 dB steps. The control is a 6-bit parallel interface, operating on dual supply voltage:  $V_{DD}=+3V$ ,  $V_{SS}=-3V$ . The DAT-31R5-PN is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

## Simplified Schematic



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Rev. B  
M106151  
DAT-31R5-PN  
061121  
Page 1 of 12

# Digital Step Attenuator

# DAT-31R5-PN+ DAT-31R5-PN

## RF Electrical Specifications, DC-2400 MHz, $T_{AMB}=25^{\circ}C$ , $V_{DD}=+3V$ , $V_{SS}=-3V$

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ 0.5 dB Attenuation Setting	DC-1	—	0.03	0.1	dB
	1-2.4	—	0.05	0.15	dB
Accuracy @ 1 dB Attenuation Setting	DC-1	—	0.02	0.1	dB
	1-2.4	—	0.05	0.15	dB
Accuracy @ 2 dB Attenuation Setting	DC-1	—	0.05	0.15	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 4 dB Attenuation Setting	DC-1	—	0.07	0.2	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 8 dB Attenuation Setting	DC-1	—	0.03	0.2	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 16 dB Attenuation Setting	DC-1	—	0.1	0.3	dB
	1-2.4	—	0.15	0.3	dB
Insertion Loss <sup>(note1)</sup> @ all attenuator set to 0dB	DC-1	—	1.3	1.9	dB
	1-2.4	—	1.6	2.4	dB
Input IP3 <sup>(note 2)</sup> (at Min. and Max. Attenuation)	DC-2.4	—	+52	—	dBm
Input Power @ 0.2dB Compression* (at Min. and Max. Attenuation)	DC-2.4	—	+24	—	dBm
VSWR	DC-1	—	1.2	1.5	—
	1-2.4	—	1.2	1.5	—

### Notes:

1. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.35dB @1000MHz, 0.60dB @2400MHz, 0.75dB @4000MHz)
2. Input IP3 and 1dB compression degrades below 1 MHz

## DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
$V_{DD}$ , Supply Voltage	2.7	3	3.3	V
$V_{SS}$ , Supply Voltage	-3.3	-3	-2.7	V
$I_{DD}$ (I <sub>SS</sub> ), Supply Current	—	—	100	$\mu A$
Control Input Low	—	—	$0.3xV_{DD}$	V
Control Input High	$0.7xV_{DD}$	—	—	V
Control Current	—	—	1	$\mu A$

## Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	$\mu Sec$
Switching Control Frequency	—	1.0	—	MHz

## Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
$V_{DD}$	-0.3V Min., 4V Max.
$V_{SS}$	-4V Min., 0.3V Max.
Voltage on any input	-0.3V Min., $V_{DD}+0.3V$ Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm



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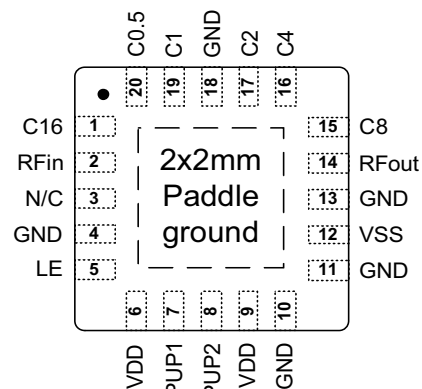
## Pin Description

Function	Pin Number	Description
C16	1	Control for Attenuation bit, 16dB (Note 3)
RF in	2	RF in port (Note 1)
N/C	3	Not connected (Note 4)
GND	4	Ground connection
LE	5	Latch Enable Input (Note 2)
V <sub>DD</sub>	6	Positive Supply Voltage
PUP1	7	Power-up selection
PUP2	8	Power-up selection
V <sub>DD</sub>	9	Positive Supply Voltage
GND	10	Ground connection
GND	11	Ground connection
V <sub>SS</sub>	12	Negative Supply Voltage
GND	13	Ground connection
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB
C4	16	Control for attenuation bit, 4 dB
C2	17	Control for attenuation bit, 2 dB
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB
C0.5	20	Control for attenuation bit, 0.5 dB
GND	Paddle	Paddle ground (Note 5)

### Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 100KΩ resistor to V<sub>DD</sub>.
- Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
- Place a shunt 10KΩ resistor to GND
- The exposed solder pad on the bottom of the package (See Pin configuration) must be grounded for proper device operation.

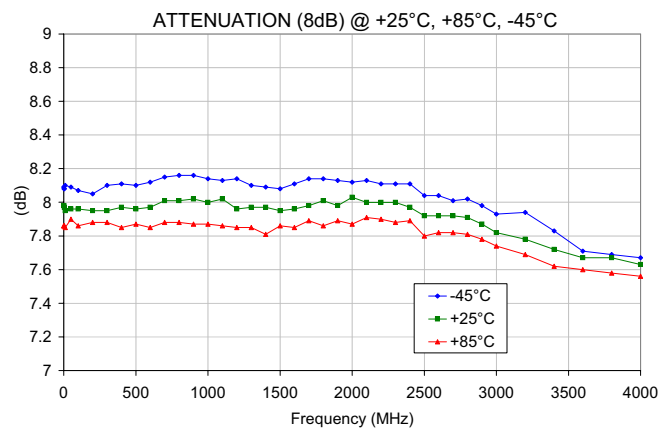
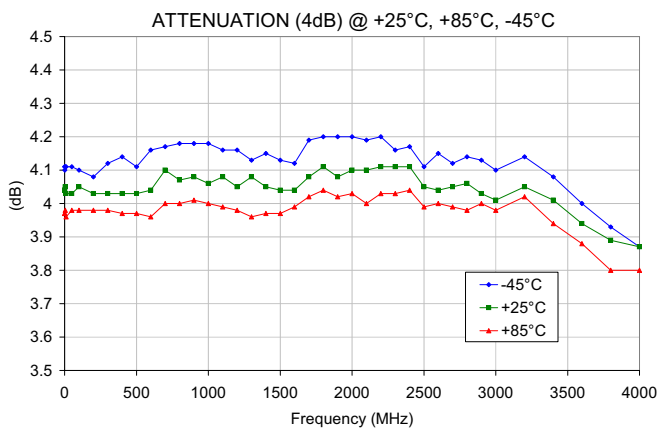
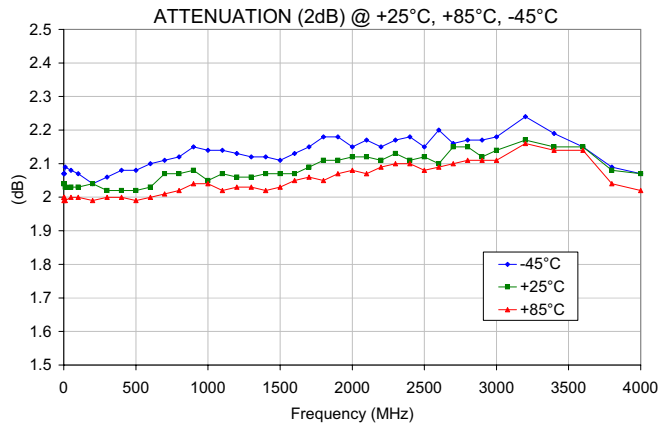
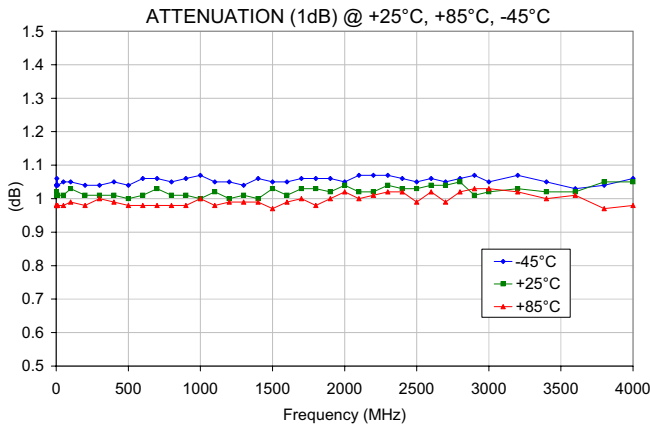
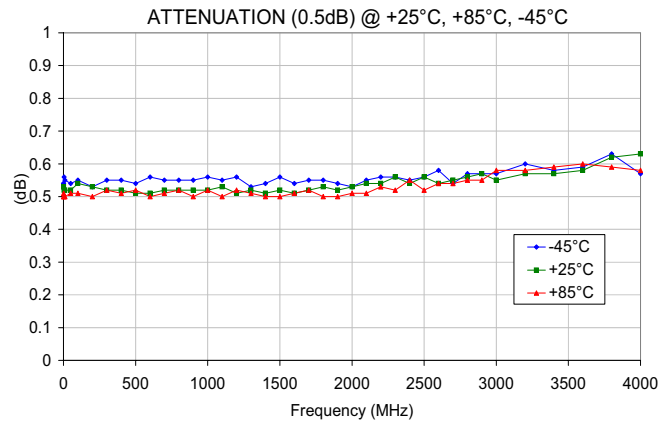
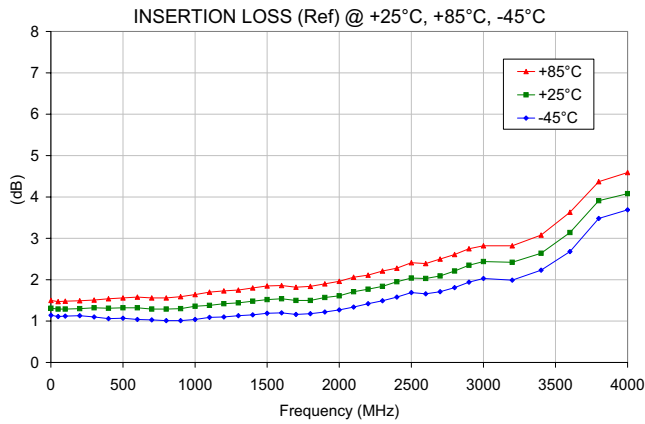
## Pin Configuration (Top View)



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**DAT-31R5-PN+**  
**DAT-31R5-PN**

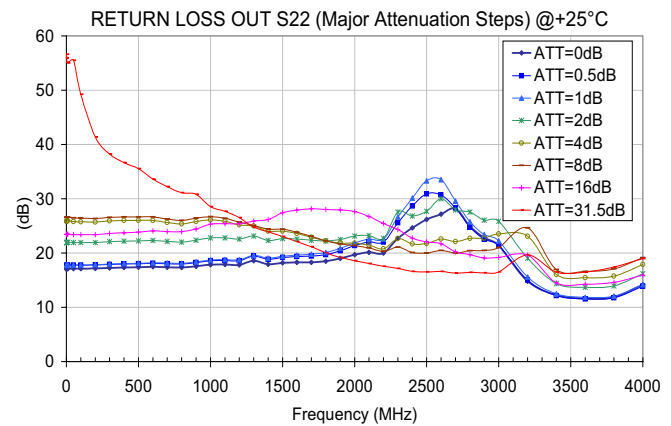
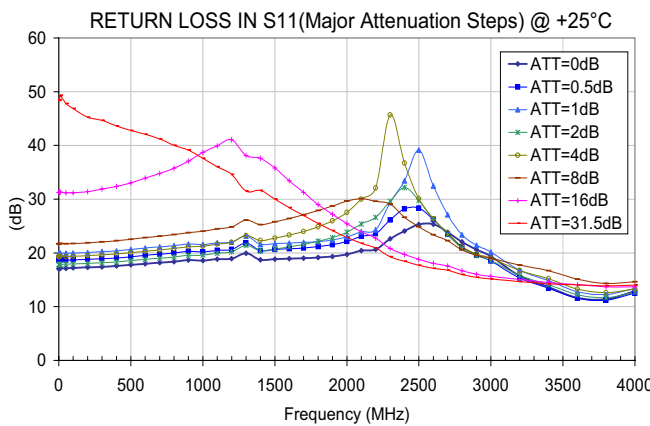
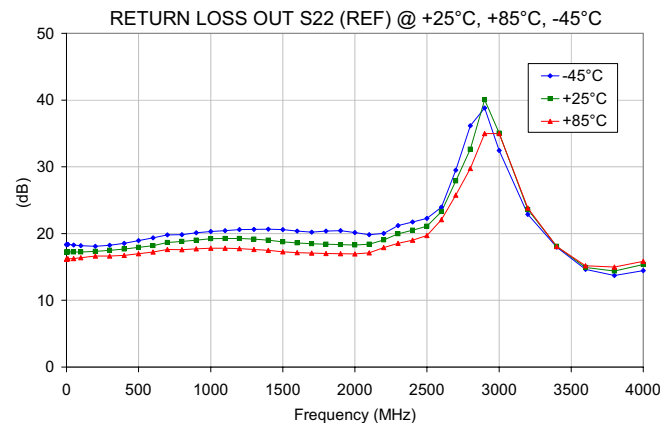
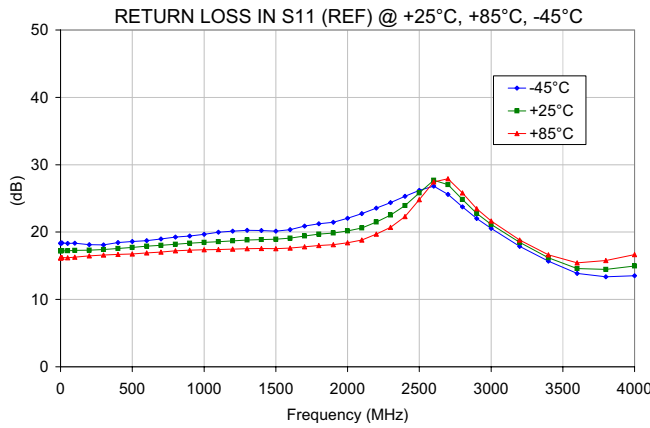
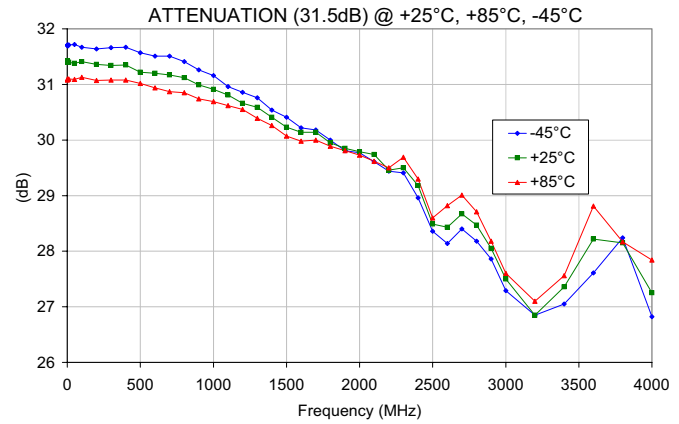
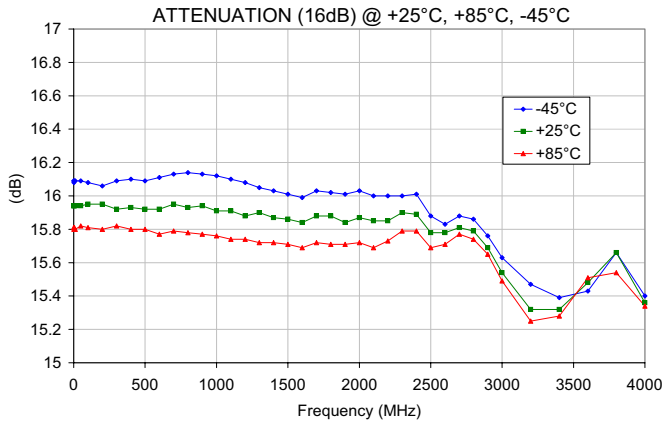
## Typical Performance Curves



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## Typical Performance Curves



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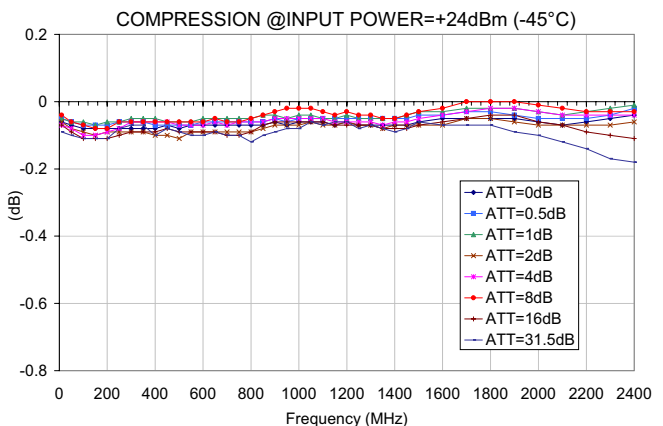
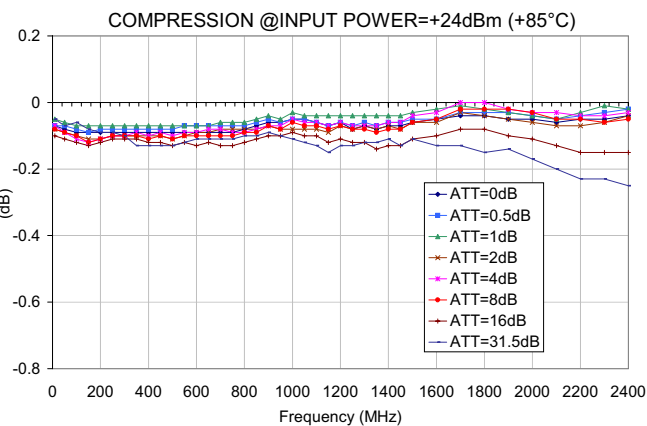
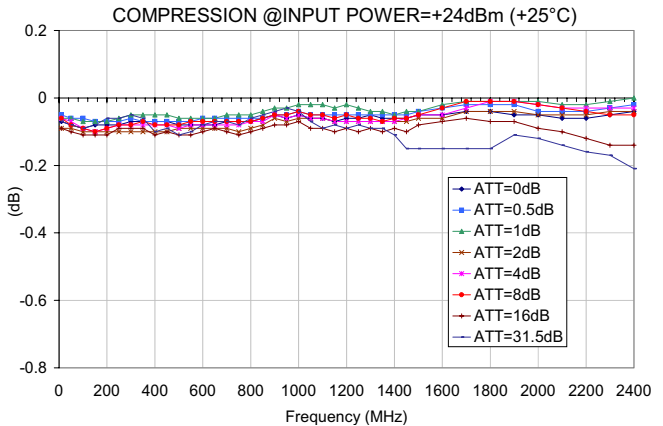
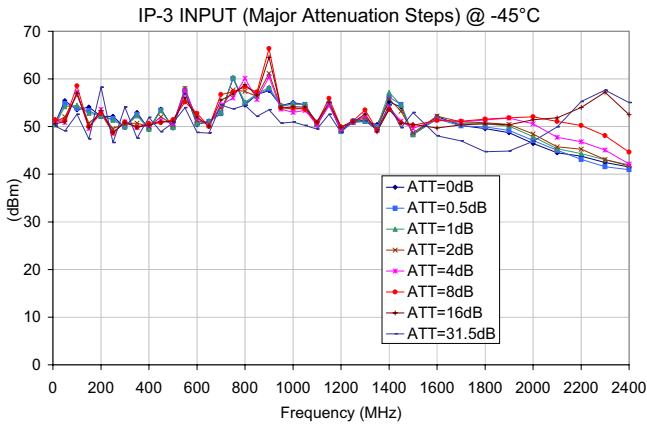
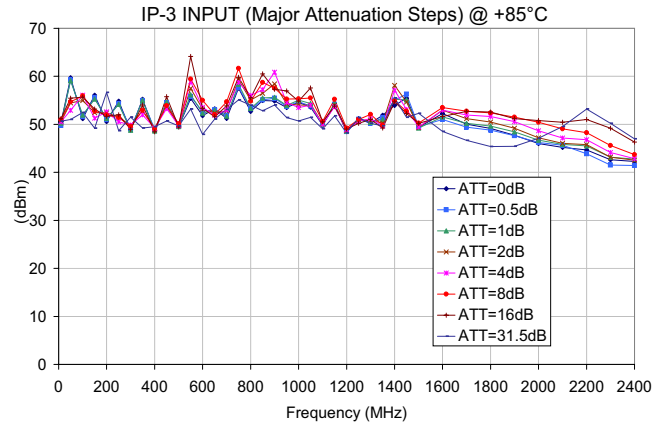
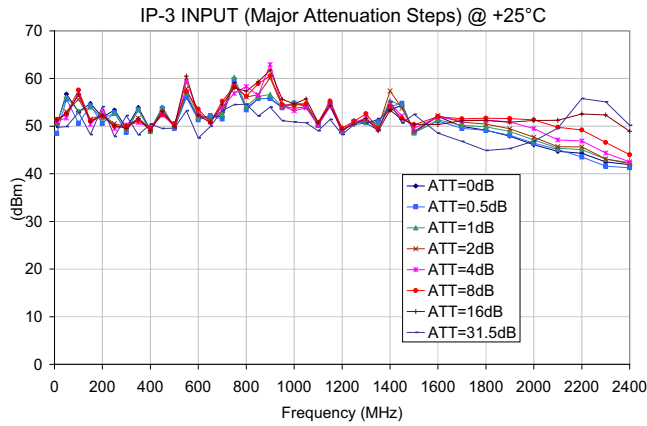
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# DAT-31R5-PN+ DAT-31R5-PN

## Typical Performance Curves



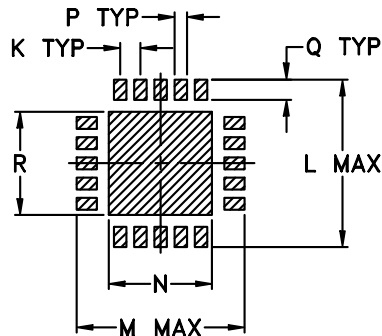
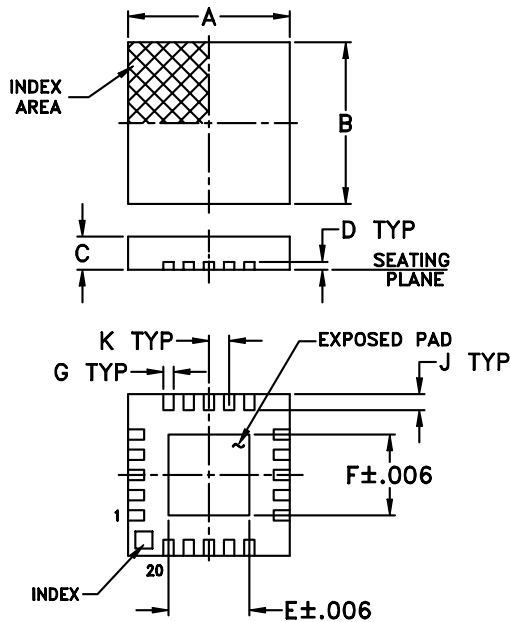
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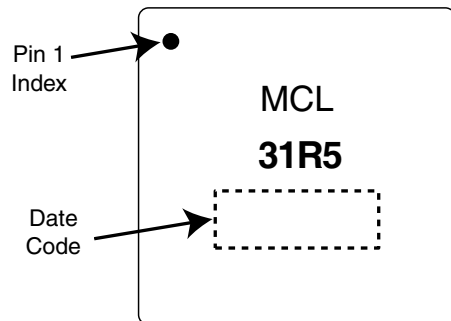
## Outline Drawing (DG983-1)



**SUGGESTED LAYOUT FOR PCB LAND PATTERN**  
PATTERN TO BE WITHIN ±.002

**TOLERANCES**  
±.005  
UNLESS OTHERWISE SPECIFIED

## Device Marking

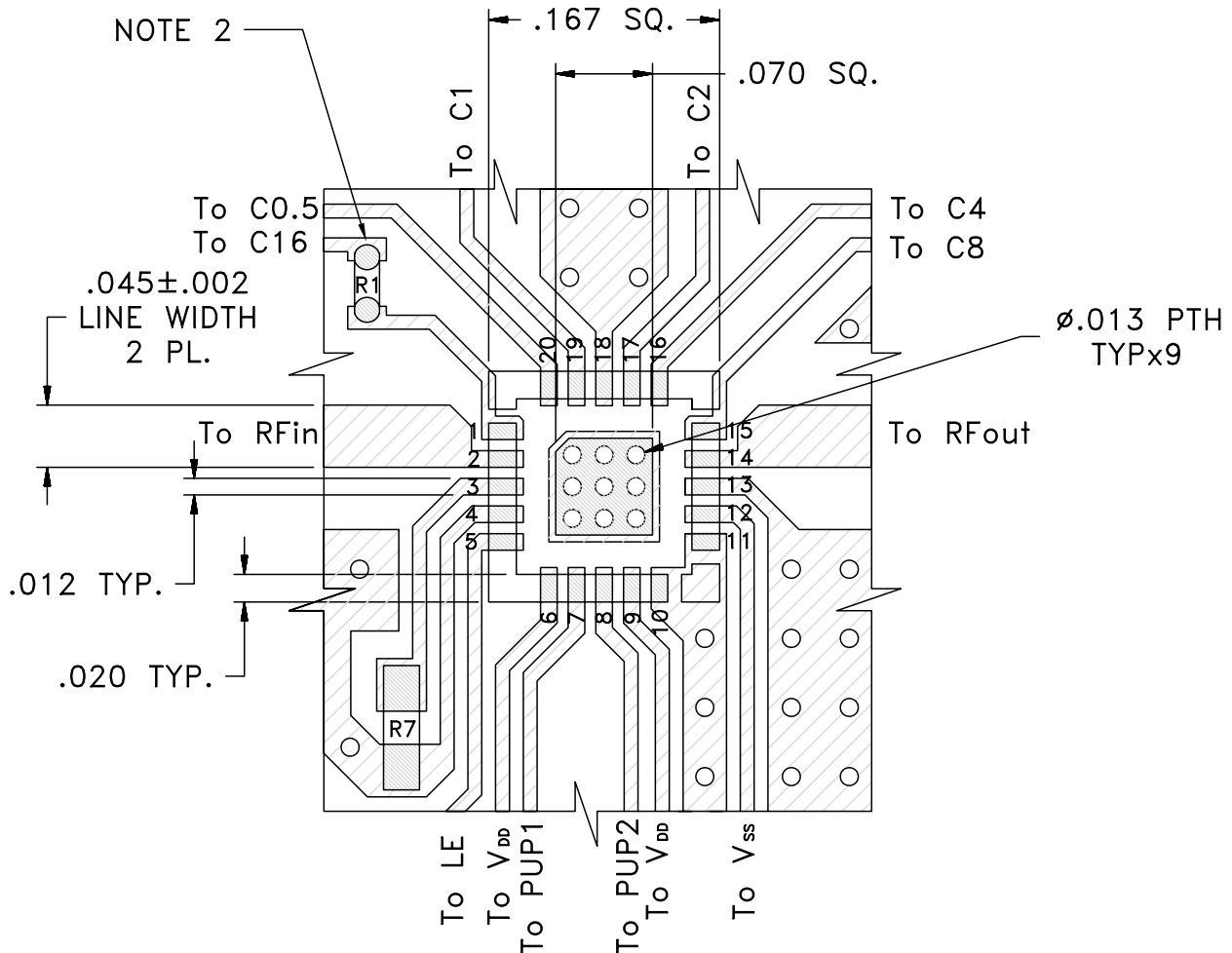


## Outline Dimensions (inch/mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	WT. GRAMS
.157	.157	.035	.008	.081	.081	.010	—	.022	.020	.166	.166	.070	.012	.020	.070	.04
4.00	4.00	0.90	0.20	2.06	2.06	0.25	—	0.56	0.50	4.22	4.22	1.78	0.31	0.51	1.78	



## Suggested Layout for PCB Design (PL-179)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1, R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



**NOTE:**

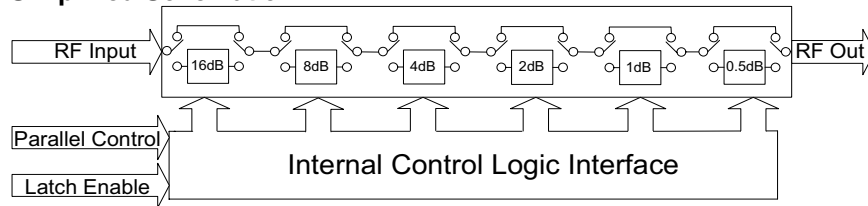
1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. .025"±.002". COPPER: 1/2 OZ. EACH SIDE.  
FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603, 0402 SIZES CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

-  DENOTES PCB COPPER LAYOUT WITH SOMBC ( SOLDER MASK OVER BARE COPPER )
-  DENOTES COPPER LAND PATTERN FREE OF SOLDERMASK



# Digital Step Attenuator

## Simplified Schematic



The DAT-31R5-PN parallel interface consists of 6 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table						
Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1

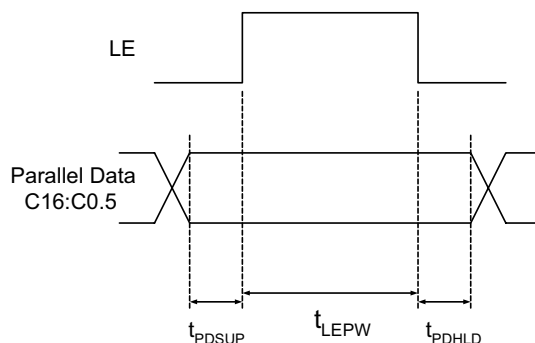
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table

The parallel interface timing requirements are defined by Figure 1 (Parallel Interface Timing Diagram) and Table 2 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

**Figure 1: Parallel Interface Timing Diagram**



**Table 2. Parallel Interface AC Characteristics**

Symbol	Parameter	Min.	Max.	Units
$t_{LEPW}$	LE minimum pulse width	10		ns
$t_{PDSUP}$	Data set-up time before clock rising edge of LE	10		ns
$t_{PDHL}$	Data hold time after clock falling edge of LE	10		ns

## Power-up Control Settings

The DAT-31R5-PN always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided.

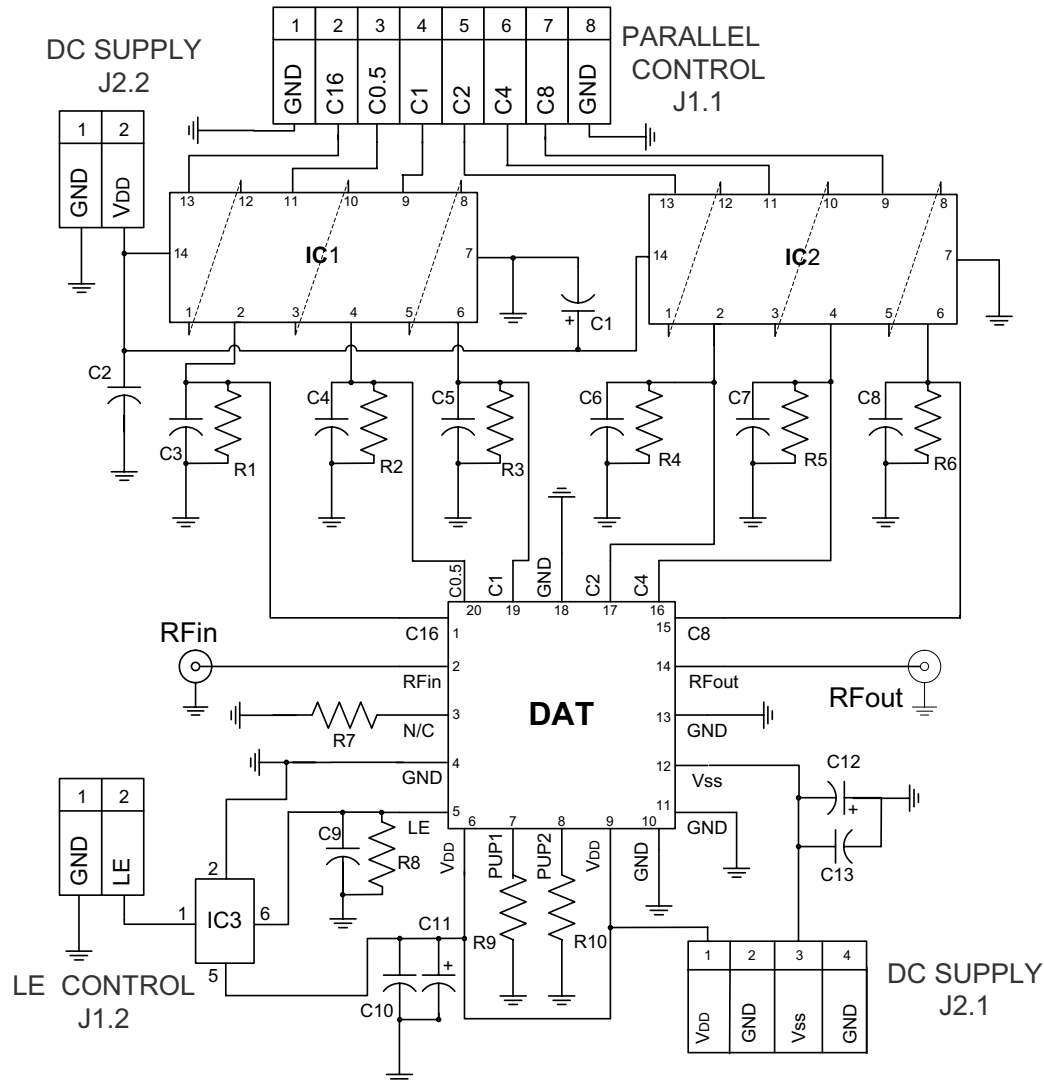
When the attenuator powers up with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in Table 3: (Power-Up Truth Table, Parallel Mode).

<b>Table 3. Power-Up Truth Table, Parallel Mode</b>			
<b>Attenuation State</b>	<b>PUP1</b>	<b>PUP2</b>	<b>LE</b>
Reference	0	0	0
8 (dB)	0	1	0
16 (dB)	1	0	0
31 (dB)	1	1	0
Defined by C0.5-C16 (See Table 1-Truth Table)	X (Note 1)	X (Note 1)	1

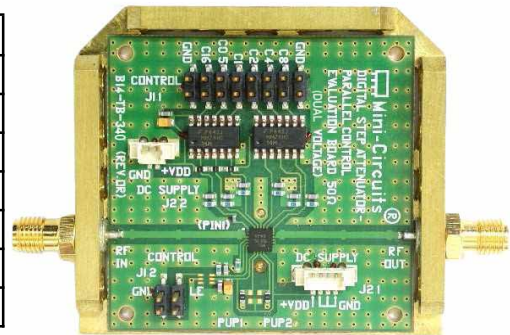
Note 1: PUP1 and PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state.

Power-Up with LE=1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

## TB-340 Evaluation Board Schematic Diagram



Bill of Materials	
R1 - R8	Resistor 0603 10 KOhm +/- 1%
R10, R11	Resistor 0603 470 Ohm +/- 1%
R9	Resistor 0402 10 KOhm +/- 1%
C2 - C10 & C13	NPO Capacitor 0603 100pF +/- 5%
C1, C11 & C12	Tantalum Capacitor 100 nF +/- 10%
IC1, IC2	Hex inverting Schmitt trigger MM74HC14
IC3	Dual non-inverting Schmitt trigger SN74LVC2G17



**TB-340**

