

The 2N3955 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The 2N3955 family are matched JFET pairs for differential amplifiers. The 2N3955 family of general purpose JFETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise and capacitance

The 2N3955 family exhibits low capacitance - 6pF max and a spot noise figure of - 0.5dB max. The part offers a superior tracking ability.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

2N3955 Applications:

- Wideband Differential Amps
- High Input Impedance Amplifiers

FEATURES

LOW DRIFT	$ \Delta V_{GS1-2} / \Delta T = 5\mu V/^{\circ}C$ max.
LOW LEAKAGE	$I_G = 20pA$ TYP.
LOW NOISE	$e_n = 10nV/\sqrt{Hz}$ TYP.

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$-V_{DSO}$	Drain to Source Voltage	60V
$-I_{G(f)}$	Gate Forward Current	50mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	400mW @ 25°C
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MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2} / T $ max.	DRIFT VS. TEMPERATURE	25	$\mu V/^{\circ}C$	$V_{DG}=20V, I_D=200\mu A$ $T_A=-55^{\circ}C$ to $+125^{\circ}C$
$ V_{GS1-2} $ max.	OFFSET VOLTAGE	10	mV	$V_{DG}=20V, I_D=200\mu A$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

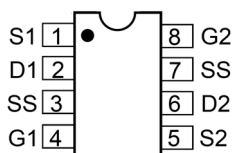
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	60	--	--	V	$V_{DS} = 0$ $I_D=1\mu A$
BV_{GGO}	Gate-To-Gate Breakdown	60	--	--	V	$I_G = 1nA$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
Y_{fss}	Full Conduction	1000	2000	3000	μmho	$V_{DG} = 20V$ $V_{GS} = 0V$ $f = 1kHz$
Y_{fs}	Typical Operation	500	700	1000	μmho	$V_{DG} = 20V$ $I_D = 200\mu A$
$ Y_{FS1-2} / Y_{FS} $	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	2	5	mA	$V_{DG} = 20V$ $V_{GS} = 0V$
$ I_{DSS1-2} / I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
$V_{GS(off)}$ or V_p	Pinchoff voltage	1	2	4.5	V	$V_{DS} = 20V$ $I_D = 1nA$
$V_{GS(on)}$	Operating Range	0.5	--	4	V	$V_{DS} = 20V$ $I_D = 200\mu A$
GATE CURRENT						
$-I_G$	Operating	--	20	50	pA	$V_{DG} = 20V$ $I_D = 200\mu A$
$-I_G$	High Temperature	--	--	50	nA	$T_A = +125^{\circ}C$
$-I_G$	Reduced V_{DG}	--	5	--	pA	$V_{DG} = 10V$ $I_D = 200\mu A$
$-I_{GSS}$	At Full Conduction	--	--	100	pA	$V_{DG} = 20V$ $V_{DS} = 0$
OUTPUT CONDUCTANCE						
Y_{OSS}	Full Conduction	--	--	5	μmho	$V_{DG} = 20V$ $V_{GS} = 0V$
Y_{OS}	Operating	--	0.1	1	μmho	$V_{DG} = 20V$ $I_D = 200\mu A$
$ Y_{OS1-2} $	Differential	--	0.01	0.1	μmho	
COMMON MODE REJECTION						
CMR	$-20 \log V_{GS1-2} / V_{DS} $	--	100	--	dB	$\Delta V_{DS} = 10$ to $20V$ $I_D = 200\mu A$
CMR	$-20 \log V_{GS1-2} / V_{DS} $	--	75	--	dB	$\Delta V_{DS} = 5$ to $10V$ $I_D = 200\mu A$
NOISE						
NF	Figure	--	--	0.5	dB	$V_{DS} = 20V$ $V_{GS} = 0V$ $R_G = 10M\Omega$ $f = 100Hz$ $NBW = 6Hz$
e_n	Voltage	--	--	15	nV/ \sqrt{Hz}	$V_{DS} = 20V$ $I_D = 200\mu A$ $f = 10Hz$ $NBW = 1Hz$
CAPACITANCE						
C_{ISS}	Input	--	--	6	pF	$V_{DS} = 20V$ $V_{GS} = 0V$ $f = 1MHz$
C_{RSS}	Reverse Transfer	--	--	2	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	$V_{DG} = 20V$ $I_D = 200\mu A$

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

2N3955 in PDIP / SOIC
2N3955 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP / SOIC (Top View)



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