FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-10801-4E

Semicustom

CMOS

AccelArray™

CA91 Series

■ DESCRIPTION

AccelArray™* is a new structured ASIC family, offering short development time, and low development cost with pre-diffused IP macros into base masters and pre-designed common 3 to 4 metal layers out of 6 to 7 layers.

By using 0.11 µm CMOS process technology, the devices can support 6 million logic gates, 4.55 Mbits SRAM and 3.125 Gbps high speed transmission macros. Ultra-high pin count FC-BGA (up to 729 pins to 1681 pins) packages are available.

* : AccelArray™ is a trademark of Fujitsu Limited.

■ FEATURES

- High-speed, large scale ASIC produced in short development time:
  TAT = One third compared with Standard Cell ASICs (target value)
- Uses an architecture that simplifies physical design tasks.
- Pre-designed common masters with IR-drop free.
- Pre-designed test circuit insertion to reduce test synthesis tasks.
- Uses a dedicated timing-driven layout tool to reduce development time.
- Signal Integrity Free (pre-designed main clock trees without design verifications)
- Max built-in gate number : 6,000,000 gates or more
- Technology : 0.11 µm Silicon gate CMOS, 6 to 7-metal layers (wiring material: copper), low-k inter-layer film
- Internal cells support high-speed operation
- Power supply voltage : +1.2 V ± 0.1 V/2.5 V ± 0.2 V (Dual power supply. Needs 1.5 V power supply during using HTSL.) .
- Operation junction temperature : –40 °C to +125 °C (standard)
- Max operating frequency: 333 MHz (internal circuit)
- Support for fast interface/macro (200 MHz/400 MHz DDR I/F, 2.5 Gbps PCI Express, 3.125 Gbps XAUI, etc.)
- Special interfaces (P-CML,LVDS,PCI,HSTL,SSTL-2, etc.)
- Embedded macro : PLL, SRAM
- 8-channel clock supply system incorporating a PLL
- Supports Memory-BIST/Boundary-SCAN
- Package : FC-BGA (729 pins to 1681 pins)
- ARM core is supported.

Note : It contains under planning.

FUJITSU

■ MACRO LIBRARY

1. Unit cell

- Flip Flop, with clear/preset (support for Mux-D Scan, with Lock up latch)
- Clock Buffer
- Other combination circuits (approximately 50 different types)

2. APLL

- Input frequency : 25 MHz to 800 MHz
- Output frequency : 400 MHz to 800 MHz
- User frequency : 25 MHz to 800 MHz
- Phase shift : 0/90/180/270 deg.

3. SRAM

- 1R1W-SRAM : 32 words × 40 bits
- 2RW-SRAM : 512 words × 40 bits
  Bit Select 1 : 1, 2 : 1, 4 : 1, 8 : 1
  1 RW operation accesses specified port bit-width

4. I/O

- HSTL *1 (250 MHz)
- 2.5 V LVCMOS (200 MHz (input buffer), 75 MHz to 100 MHz (output buffer))
- PCML (250 MHz)
- LVDS (311 MHz)
- SSTL2 (250 MHz)
- PCI-66 *2 (66 MHz)
- PCI-X *2 (133 MHz)
- 3.3 V tolerant (200 MHz (input buffer), 75 MHz to 100 MHz (output buffer))

*1 : Needs 1.5 V power supply

*2 : As the I/F is 3.3V tolerant, it does not satisfy the PCI standard in some cases.

Dedicated for Giga Frame

- SPI-4P2 (622 Mbps to 800 Mbps)
- XAUI (3.125 Gbps)
- Fibre Channel (1.0 Gbps, 2.0 Gbps)
- Serial Rapid IO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)
- PCI Express (2.5 Gbps)

5. Memory interface

- DDR-SDRAM (400 Mbps)
- QDR-SDRAM (400 Mbps)
- Peer to Peer SDR (200 Mbps)
- Peer to Peer DDR (200 Mbps)
- SDR-SDRAM (167 Mbps)

■ ABSOLUTE MAXIMUM RATINGS

(VSS = 0 V)

Parameter	Symbol	Application	Rating		Unit
			Min	Max	
Power supply voltage	VDD	VDDI (Core)	− 0.5	1.8	V
		VDDE (for 2.5 V CMOS I/Os, 3.3 V Tolerant I/Os)	− 0.5	3.6	V
		VDDE (for 1.5 V I/Os*4)	− 0.5	3.6	V
Input voltage *1	VI	2.5 V CMOS	− 0.5	VDDE + 0.5 (≤ 3.6)	V
		3.3 V Tolerant	− 0.5	VDDE + 3.6 (≤ 4.0)	V
Output voltage	VO	2.5 V CMOS	− 0.5	VDDE + 0.5 (≤ 3.6)	V
		3.3 V Tolerant (H/L-State)	− 0.5	VDDE + 0.5 (≤ 4.0)	V
		3.3 V Tolerant (Z-State)	− 0.5	4.0	V
Storage temperature	Tst	—	− 55	+ 125	°C
Operation junction temperature	Tj	—	− 40	+ 125	°C
Power supply pin current *2	ID	Each VDDE pin	—	180	mA
		Each VDDI pin	—	200	mA
		Each VSS pin	—	200	mA
Output current *3	IO	2.5 V CMOS	—	±10	mA
		3.3 V Tolerant	—	±7.5	mA

*1 : Different limit values apply for LVDS, etc.

*2 : Maximum supply current in normal operation. Supply current depends on the frame or the package.

*3 : Maximum output current in normal operation

*4 : Required when using HSTL I/O.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Dual power supply (VDDI = +1.2 V ± 0.1 V, VDDE = +2.5 V ± 0.2 V, (+1.5 V ± 0.1 V))

(VSS = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	Power supply voltage for core	VDDI	1.1	1.2	1.3	V
	Power supply voltage for 2.5 V I/Os	VDDE	2.3	2.5	2.7	V
	Power supply voltage for 1.5 V I/Os *	VDDE	1.4	1.5	1.6	V
“H” level input voltage	2.5 V CMOS	VIH	1.7	—	VDDE + 0.3	V
	3.3 V Tolerant		1.7	—	3.6	V
“L” level input voltage	2.5 V CMOS	VIL	− 0.3	—	0.7	V
	3.3 V Tolerant		− 0.3	—	0.7	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

* : Applicable to HSTL I/O.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

(VDDI = 1.2 V ± 0.1 V, VDDE = 2.5 V ± 0.2 V, VSS = 0 V, Tj = – 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	VOH	IOH = – 100 μA	VDDE – 0.2	—	VDDE	V
"L" level output voltage	VOL	IOL = 100 μA	0	—	0.2	V
Input leak current *	IL	—	– 10	—	+ 10	μA
Pull-up/Pull-down resistor	RP	2.5 V CMOS pin, VIL = 0 V at pull-up, VIH = VDDE at pull-down	10	25	55	kΩ
		3.3 V Tolerant pin, VIH = 3.0 V to 3.6 V at pull-down	12	33	85	kΩ

* : The input leak current may exceed the above value if an input buffer with pull-up or pull-down resistor is used.

Note : Refer to the application note for details of HSTL I/O.

2. AC CHARACTERISTICS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	tpd *1	typ *2 × tmin *3	typ *2 × ttyp *3	typ *2 × tmax *3	ns

*1 : Delay time = propagation delay time, enable time, and disable time.

*2 : typ can be estimated from the cell specification.

*3 : Measurement condition

Measurement condition	tmin	ttyp	tmax
VDD = 1.2 V ± 0.1 V, VSS = 0 V, Tj = – 40 °C to + 125 °C	0.73	1.00	1.43

Note : Obtains the tpd max corresponding to the maximum junction temperature Tj.

■ I/O PIN CAPACITANCE

(Tj = +25 °C, VDDE = VI = 0 V, f = 1 MHz)

Parameter	Symbol	Value	Unit
Input pin	CIN	Max 16	pF
Output pin	COUT	Max 16	pF
I/O pin	CI/O	Max 16	pF

Note : The capacity depends on the package, pin positions, and similar.

■ DESIGN METHODOLOGY

- To make development faster, the number of layers customizable in AccelArray is restricted to 3 to 4. Blocks that do not need to be redesigned for each product can be designed once and then incorporated into the architecture. As only 3 to 4 customizable layers are available for development of each product, the requirements of the layout tool are low. The requirements for timing design, where excessive complexity causes convergence to be slow, are also low. As result, the time required for design work is reduced. Primarily, tools supplied by Fujitsu are used for logic design.

- A special-purpose tool is used to determine the pin layout. This produces speedy and reliable results.

■ SUPPORT TOOL

- Frame estimation
  FUJITSU LIMITED : FESTA
- Pin assignment
  FUJITSU LIMITED : PASTEL
- Logic synthesis
  Synopsys, Inc. : Design Compiler, Cadence Design Systems, Inc. : BuildGates
- Physical synthesis
  Synplicity, Inc. : Amplify AccelAllay
- Format verification
  Cadence Design Systems, Inc. : Conformal ASIC, Synopsys, Inc. : Formality
  FUJITSU LIMITED : ASSURE
- Delay calculation
  FUJITSU LIMITED : LCADFE
- Timing analysis
  Synopsys, Inc. : PrimeTime, FUJITSU LIMITED : GISTA
- Simulation
  Cadence Design Systems, Inc. : NC-Verilog/NC-VHDL, Synopsys, Inc. : VCS,
  Mentor Graphics Corporation : ModelSim, FUJITSU LIMITED : LCADFE
- Layout
  FUJITSU LIMITED : AccelBuilder
- Power calculation
  FUJITSU LIMITED : PScope
- Power analysis
  Cadence Design Systems, Inc. : VoltageStorm
- Test synthesis
  FUJITSU LIMITED : DFTPlanner
- ATPG
  FUJITSU LIMITED : FANTCAD/X-Pax/TERBAN
- Validation
  FUJITSU LIMITED : LCADVL
- Fault simulation
  FUJITSU LIMITED : FANSCAD

Note : The company names and the product names are the trademarks or registered trademarks of their respective owners.

■ FRAME LINE UP

2 groups are provided depending on the I/O transmission speed: Mega Frame (400 Mbps) and Giga Frame (622 Mbps to 3.125 Gbps).

Mega Frame Line Up

Frame name		M20	M30	M40	M50	M52	A50*2
I/O cell count *1		696	824	952	1176	1176	1176
FF cell count (× 1000)		50	70	93	150	233	186
Available gate count (× 1000)		720	1008	1344	2160	3689	2872
ASIC equivalent gate count (× 1000)		1219	1707	2276	3658	6019	4736
SRAM size (Kbits)	2RW-SRAM	1680	2240	2880	4400	2400	2960
	1R/1W-SRAM	90	105	120	150	150	150
	Total (Max)	1770	2345	3000	4550	2550	3110
PLL macro count		8	8	8	8	8	8
Package (The value inside [ ] is body size, Ball pitch 1.00 mm)	FC-BGA729 [29 mm sq.]	○	—	—	—	—	—
	FC-BGA961 [33 mm sq.]	○	○	○	—	—	—
	FC-BGA1156 [35 mm sq.]	—	○	○	○	○	○
	FC-BGA1681 [42.5 mm sq.]	—	—	—	○	○	○

*1 : Actual available I/O count varies with the interface type.

*2 : ARM9 core is supported.

Giga Frame Line Up (including frames under planning)

Frame name		G30	G40	G45	G50	G55
4 channels G-phy (Tx + Rx)		3	4	2	6	2
S-phy (Tx + Rx)		0	0	2	0	2
I/O cell count (excluding high-speed IF) *		612	688	554	864	760
FF cell count (× 1000)		69	93	93	206	149
Available gate count (× 1000)		1007	1343	1343	3133	2158
ASIC equivalent gate count (× 1000)		1706	2275	2275	5196	3656
SRAM size (Kbits)	2RW-SRAM	1960	2560	2560	3040	4000
	1R/1W-SRAM	45	52	52	75	67
	Total (Max)	2005	2612	2612	3115	4067
PLL macro count		8	8	8	8	8
Package (The value inside [ ] is body size, Ball pitch 1.00 mm)	FC-BGA961 [33 mm sq.]	○	○	○	—	—
	FC-BGA1156 [35 mm sq.]	○	○	○	○	○
	FC-BGA1681 [42.5 mm sq.]	—	—	—	○	○

* : Actual available I/O count varies with the interface type.

■ PACKAGE

High pin count FC-BGAs using fine solder bump pitch technology are available for high speed data networking applications.

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0506