15HSC Series

RADIATION HARD HIGH SPEED CMOS/SOS LOGIC

The 15HSC Series offer the conbined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and high level of radiation hardness of Silicon on Sapphire technology.

The 15HSC Series of CMOS/SOS devices are pin compatible with the 54LS Series and the 54HSC Series, but with a higher speed capability.

Further device types to those listed will be available shortly. Please contact GPS for further information.

FEATURES

- Radiation Hard to 1.5µm CMOS/SOS Technology
- High SEU Immunity
- Latch Up Free
- Low Power CMOS/SOS Technology
- Plug In Replacement for 54/74LS, HC and HCT
- Dual In Line or Flatpack Packages
- High Speed (Toggle Rate 100MHz)

DEVICE TYPES

15HSC138	3-Line to 8-Line Decoder/Multiplexer
15HSC163	Synchronous 4-Bit Counter

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	10	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-25	+25	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	HST Input High Voltage	-	2.0	-	-	V
V_{IL1}	HST Input Low Voltage	-	-	-	0.8	V
V_{IH2}	HSC Input High Voltage	-	3.5	-	-	V
V_{IL2}	HSC Input Low Voltage	-	-	-	1.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}				
		I_{OH} = -20µA*	V_{DD}-0.1	-	-	V
		I_{OH} = -6.0mA*	3.7	-	-	V
		I_{OH} = -11.0mA	2.5	-	-	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}				
		I_{OL} = 20µA*	-	-	0.1	V
		I_{OL} = 6.0mA*	-	-	0.2	V
		I_{OL} = 9.0mA	-	-	0.4	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS} All inputs	-	-	±10	µA
I_{OL}	Output Leakage Current	$V_{OUT} = V_{DD}$ or V_{SS} Outputs disabled	-	-	50	µA
I_{DD}	Quiescent Current	$V_{IN} = V_{DD}$ Outputs unloaded	-	-	1	mA

V_{DD} = 5V±10%, over full operating temperature range.
* = Guaranteed but not tested.

Figure 2: Electrical Characteristics

15HSC138 : 3-Line to 8-Line Decoder/Multiplexer

Enable Inputs			Select Inputs			Outputs							
G_1	GN_{2A}	GN_{2B}	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 3: Function Table

Symbol	Parameter	Spice Simulation	Max.	Units
t_{PLH}	Propagation delay. Address to Output	7.6	15	ns
t_{PHL}	Propagation delay. Address to Output.	7.4	15	ns
t_{PLH}	Propagation delay. G to Output	9.3	15	ns
t_{PHL}	Propagation delay. G to Output	8.8	15	ns

Figure 4: Switching Characteristics

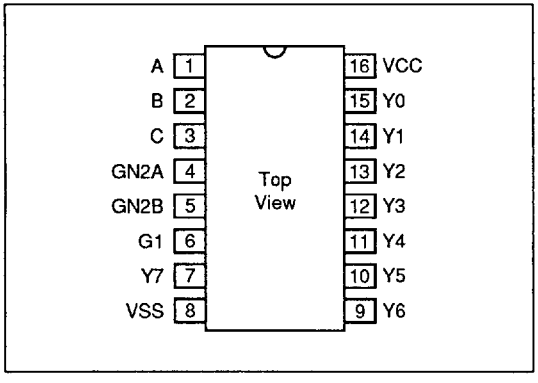


Figure 5: DIL Pin Out

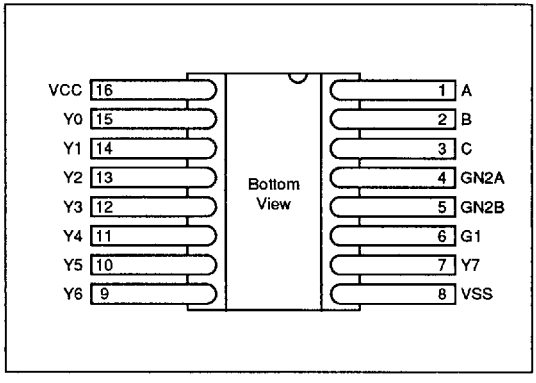


Figure 6: Flatpack Pin Out

15HSC163 : 4-Bit Counter with Synchronous Clear

Symbol	Parameter	Spice Simulation	Max.	Units
t_{PLH}	Propagation delay. Clock to RCO	11.5	15	ns
t_{PHL}	Propagation delay. Clock to RCO	11.4	15	ns
t_{PLH}	Propagation delay. Clock to any Q	9.4	15	ns
t_{PHL}	Propagation delay. Clock to any Q	9.6	15	ns
t_{PLH}	Propagation delay. ENT to RCO	8.5	15	ns
t_{PHL}	Propagation delay. ENT to RCO	8.4	15	ns

Figure 7: Switching Characteristics

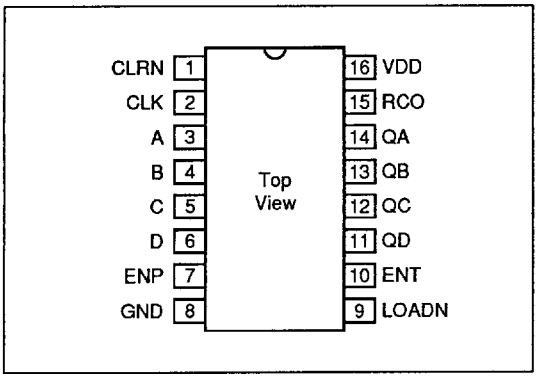


Figure 8: DIL Pin Out

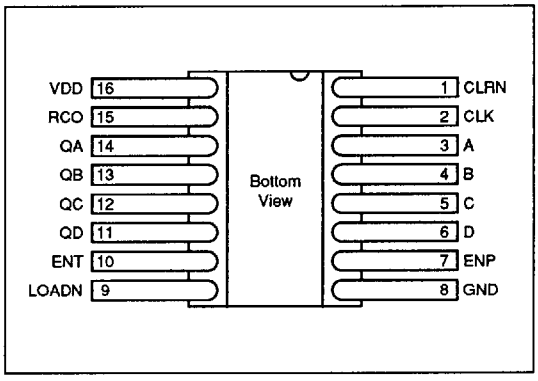


Figure 9: Flatpack Pin Out

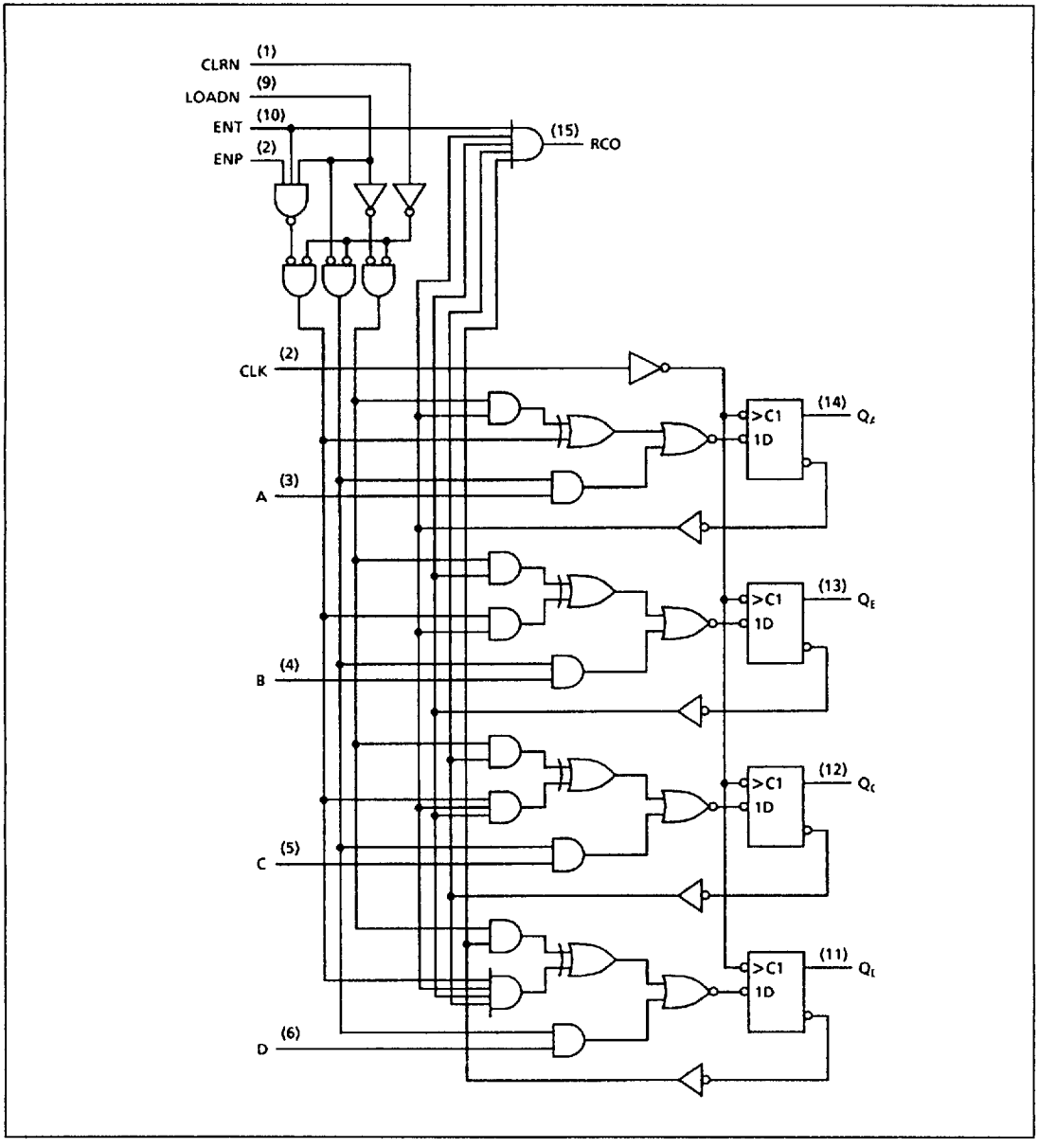


Figure 10: Logic Diagram

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.60	-	-	0.220
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	20.58	-	-	0.810
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	7.62 Typ.	-	-	0.300 Typ.	-
H	4.45	-	5.38	0.175	-	0.212
Me	-	-	8.30	-	-	0.326
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG402

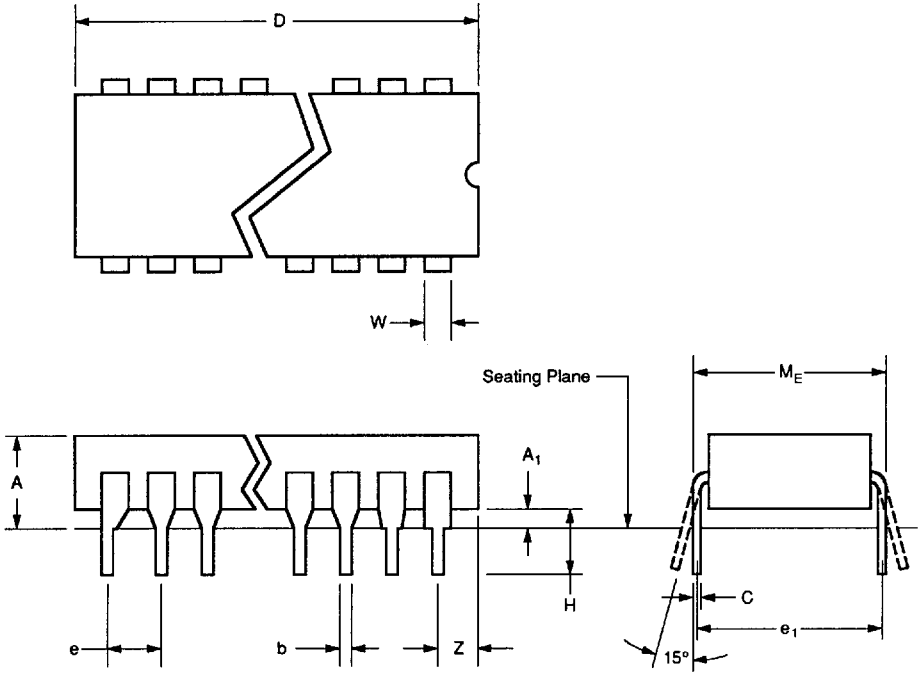


Figure 11: 16-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Inches		
	Min.	Nom.	Max.
A	-	-	0.103
A1	0.026	-	-
b	0.015	-	0.019
c	0.004	-	0.006
D	0.392	-	0.408
e	-	0.050	-
L	0.250	-	0.305
M	0.264	-	0.276
E2	0.184	-	0.196
Z	0.005	-	-

XG534

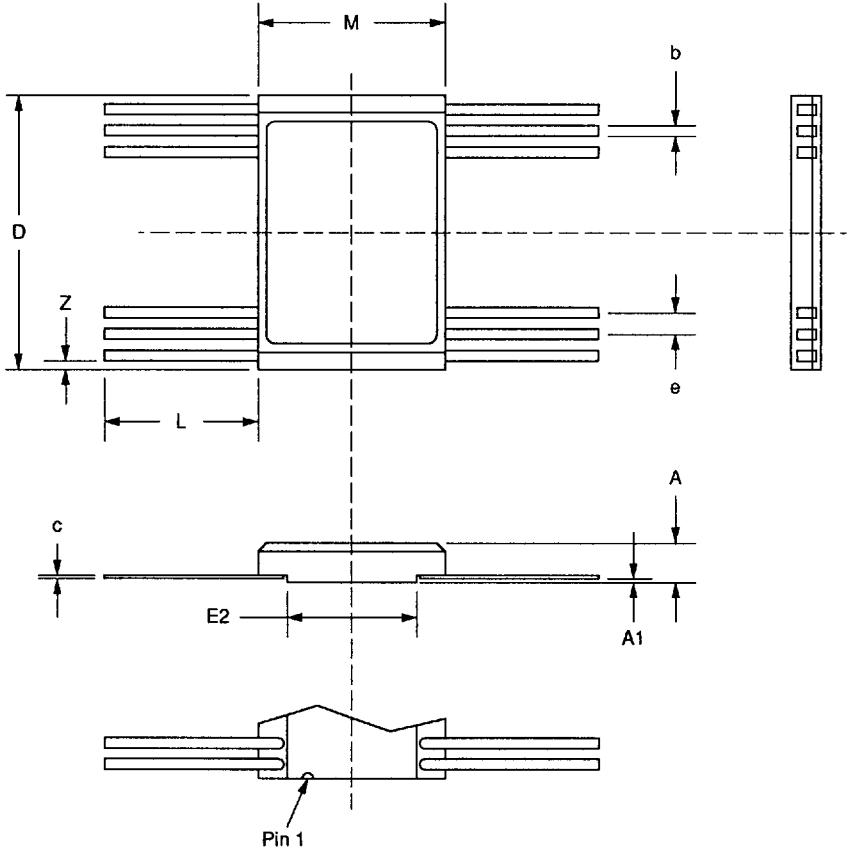


Figure 12: 16-Lead Bottom Braize Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

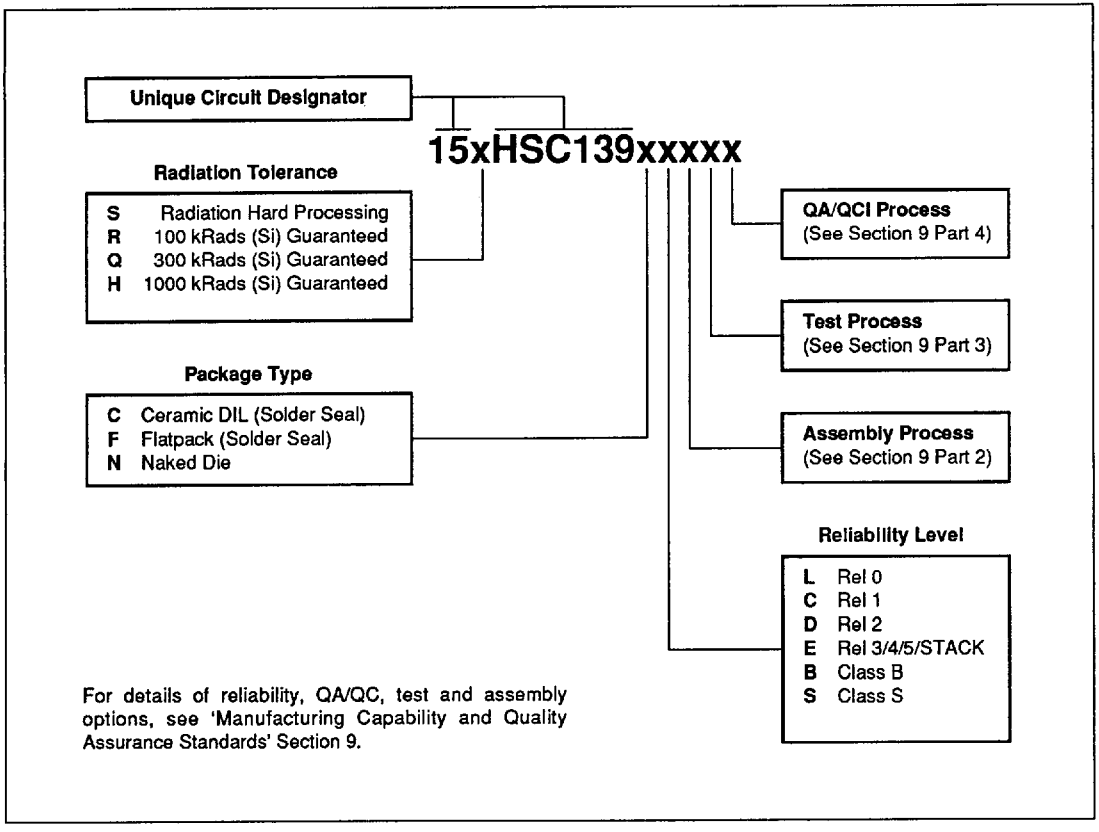
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 13: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.