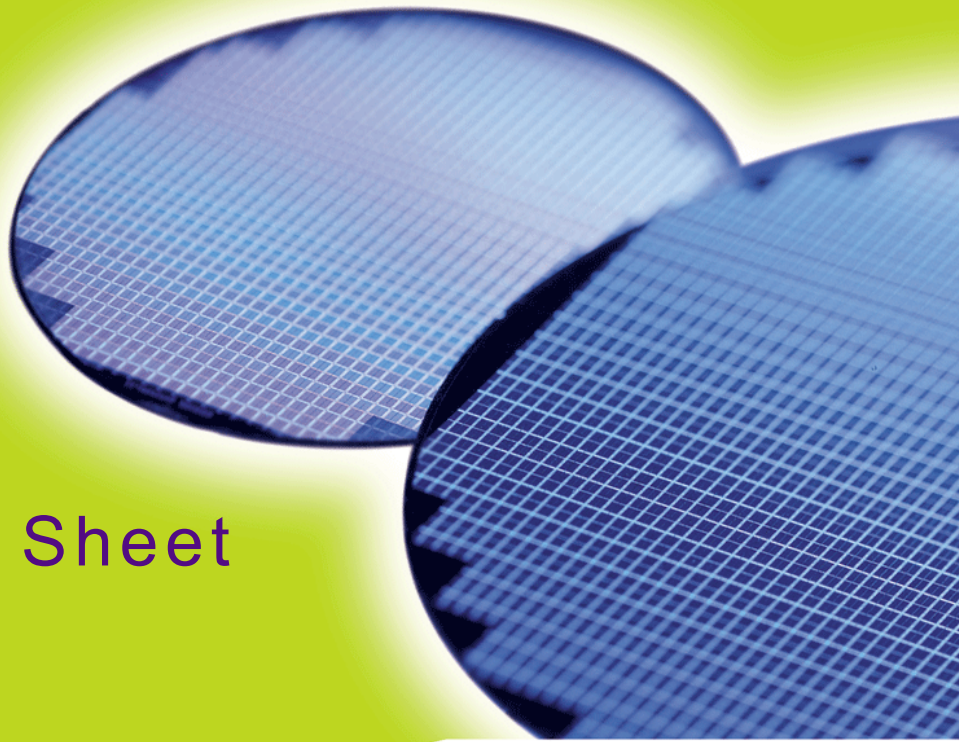


**HYB25D512400D[E/F/T]  
HY[B/I]25D512800D[C/E/F/T](L)  
HY[B/I]25D512160D[C/E/F/T](L)**

*512-Mbit Double-Data-Rate SDRAM  
DDR SDRAM*



## Internet Data Sheet

*Rev. 1.01*

HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

<b>Revision History: Rev. 1.01, 2008-07</b>	
All	Adapted internet edition
<b>Page 29</b>	Changed tCK.MAX at CL=3 for -5 speed
Previous Revision: Rev. 1.00, 2007-08	
<b>Page 33</b>	Added new IDD values
<b>Previous Revision: Rev. 0.5, 2007-08</b>	
All	New data sheet

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# 1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate SDRAM product family and describes its main characteristics.

## 1.1 Features

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and  $\overline{\text{CK}}$ )
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Programmable CAS latency: 2, 2.5, 3 and 4
- Programmable burst lengths: 2, 4, or 8
- Programmable drive strength: normal, weak
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- RAS-lockout supported  $t_{\text{RAP}} = t_{\text{RCD}}$
- 7.8  $\mu\text{s}$  Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL\_2 compatible) I/O
- $V_{\text{DD}} = 2.5 \text{ V} \pm 0.2 \text{ V}$
- $V_{\text{DDQ}} = 2.5 \text{ V} \pm 0.2 \text{ V}$
- Packages: PG-TFBGA-60, P-TFBGA-60, PG-TSOP11-66, P-TSOP11-66

**TABLE 1**  
Performance

Part Number Speed Code			-5	-6	Unit
Speed Grade			DDR400B	DDR333B	—
Max. Clock Frequency	@CL4	$f_{\text{CK4}}$	200	166	MHz
	@CL3	$f_{\text{CK3}}$	200	166	MHz
	@CL2.5	$f_{\text{CK2.5}}$	166	166	MHz
	@CL2	$f_{\text{CK2}}$	133	133	MHz

HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

## 1.2 Description

The 512-Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 536, 870, 912 bits. It is internally configured as a quad-bank DRAM.

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $2n$  prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512-Mbit Double-Data-Rate SDRAM effectively consists of a single  $2n$ -bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512-Mbit Double-Data-Rate SDRAM operates from a differential clock (CK and  $\overline{\text{CK}}$ ; the crossing of CK going HIGH and  $\overline{\text{CK}}$  going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the Industry Standard for SSTL\_2. All outputs are SSTL\_2, Class II compatible.

*Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.*



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**TABLE 2**

**Ordering Information for RoHS Compliant Products**

Product Type <sup>1)</sup>	Org.	Speed	CAS-RCD-RP Latencies <sup>2)3)4)</sup>	Clock (MHz)	Package	Note <sup>5)</sup>	
<b>Standard Temperature Range (0 °C - 70 °C)</b>							
<b>DDR400B( 3-3-3 )</b>							
HYB25D512800DF-5	×8	DDR400B	3-3-3	200	PG-TFBGA-60		
HYB25D512160DF-5	×16	DDR400B	3-3-3	200	PG-TFBGA-60		
HYB25D512400DE-5	×4	DDR400B	3-3-3	200	PG-TSOPII-66		
HYB25D512160DE-5	×16	DDR400B	3-3-3	200	PG-TSOPII-66		
HYB25D512400DF-5	×4	DDR400B	3-3-3	200	PG-TFBGA-60		
HYB25D512800DE-5	×8	DDR400B	3-3-3	200	PG-TSOPII-66		
<b>DDR333B( 2.5-3-3 )</b>							
HYB25D512160DEL-6	×16	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYB25D512160DF-6	×16	DDR333B	2.5-3-3	166	PG-TFBGA-60		
HYB25D512400DE-6	×4	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYB25D512800DEL-6	×8	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYB25D512160DE-6	×16	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYB25D512800DE-6	×8	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYB25D512400DF-6	×4	DDR333B	2.5-3-3	166	PG-TFBGA-60		
HYB25D512800DF-6	×8	DDR333B	2.5-3-3	166	PG-TFBGA-60		
<b>Industrial Temperature Range (-40 °C - 85 °C)</b>							
<b>DDR400B( 3-3-3 )</b>							
HYI25D512800DE-5	×8	DDR400B	3-3-3	200	PG-TSOPII-66		
HYI25D512160DE-5	×16	DDR400B	3-3-3	200	PG-TSOPII-66		
HYI25D512800DF-5	×8	DDR400B	3-3-3	200	PG-TFBGA-60		
HYI25D512160DF-5	×16	DDR400B	3-3-3	200	PG-TFBGA-60		
<b>DDR333B( 2.5-3-3 )</b>							
HYI25D512800DE-6	×8	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYI25D512160DE-6	×16	DDR333B	2.5-3-3	166	PG-TSOPII-66		
HYI25D512800DF-6	×8	DDR333B	2.5-3-3	166	PG-TFBGA-60		
HYI25D512160DF-6	×16	DDR333B	2.5-3-3	166	PG-TFBGA-60		

1) For detailed information regarding product type of Qimonda please see chapter "Product Nomenclature" of this data sheet.

2) CAS: Column Address Strobe

3) RCD: Row Column Delay

4) RP: Row Precharge

5) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit [www.qimonda.com/green\\_products](http://www.qimonda.com/green_products).



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**TABLE 3**

**Ordering Information for Lead-Containing Products**

Product Type <sup>1)</sup>	Org.	Speed	CAS-RCD-RP Latencies <sup>2)3)4)</sup>	Clock (MHz)	Package	Note
<b>Standard Temperature Range (0 °C - 70 °C)</b>						
<b>DDR400B( 3-3-3 )</b>						
HYB25D512160DC-5	×16	DDR400B	3-3-3	200	P-TFBGA-60	
HYB25D512160DT-5	×16	DDR400B	3-3-3	200	P-TSOPII-66	
HYB25D512400DT-5	×4	DDR400B	3-3-3	200	P-TSOPII-66	
HYB25D512800DT-5	×8	DDR400B	3-3-3	200	P-TSOPII-66	
HYB25D512800DC-5	×8	DDR400B	3-3-3	200	P-TFBGA-60	
<b>DDR333B( 2.5-3-3 )</b>						
HYB25D512160DC-6	×16	DDR333B	2.5-3-3	166	P-TFBGA-60	
HYB25D512160DT-6	×16	DDR333B	2.5-3-3	166	P-TSOPII-66	
HYB25D512400DT-6	×4	DDR333B	2.5-3-3	166	P-TSOPII-66	
HYB25D512800DC-6	×8	DDR333B	2.5-3-3	166	P-TFBGA-60	
HYB25D512800DT-6	×8	DDR333B	2.5-3-3	166	P-TSOPII-66	
<b>Industrial Temperature Range (-40 °C - 85 °C)</b>						
<b>DDR400B( 3-3-3 )</b>						
HYI25D512160DT-5	×16	DDR400B	3-3-3	200	P-TSOPII-66	
HYI25D512160DC-5	×16	DDR400B	3-3-3	200	P-TFBGA-60	
<b>DDR333B( 2.5-3-3 )</b>						
HYI25D512160DT-6	×16	DDR333B	2.5-3-3	166	P-TSOPII-66	
HYI25D512160DC-6	×16	DDR333B	2.5-3-3	166	P-TFBGA-60	

- 1) For detailed information regarding product type of Qimonda please see chapter "Product Nomenclature" of this data sheet.
- 2) CAS: Column Address Strobe
- 3) RCD: Row Column Delay
- 4) RP: Row Precharge



## 2 Configuration

This chapter contains the chip configuration and block diagrams.

### 2.1 Configuration for TFBGA-60

The ball configuration of a DDR SDRAM is listed by function in **Table 4**. The abbreviations used in the Ball#/Buffer Type column are explained in **Table 5** and **Table 6** respectively.

**TABLE 4**  
Configuration

Ball#	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
G2	CK1	I	SSTL	<b>Clock Signal</b>
G3	$\overline{\text{CK1}}$	I	SSTL	<b>Complementary Clock Signal</b>
H3	CKE	I	SSTL	<b>Clock Enable</b>
<b>Control Signals</b>				
H7	$\overline{\text{RAS}}$	I	SSTL	<b>Row Address Strobe</b>
G8	$\overline{\text{CAS}}$	I	SSTL	<b>Column Address Strobe</b>
G7	$\overline{\text{WE}}$	I	SSTL	<b>Write Enable</b>
H8	$\overline{\text{CS}}$	I	SSTL	<b>Chip Select</b>
<b>Address Signals</b>				
J8	BA0	I	SSTL	<b>Bank Address Bus</b>
J7	BA1	I	SSTL	
K7	A0	I	SSTL	<b>Address Bus</b>
L8	A1	I	SSTL	
L7	A2	I	SSTL	
M8	A3	I	SSTL	
M2	A4	I	SSTL	
L3	A5	I	SSTL	
L2	A6	I	SSTL	
K3	A7	I	SSTL	
K2	A8	I	SSTL	
J3	A9	I	SSTL	
K8	A10	I	SSTL	
	AP	I	SSTL	
J2	A11	I	SSTL	
H2	A12	I	SSTL	



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

Ball#	Name	Pin Type	Buffer Type	Function
<b>Data Signals ×4 Organization</b>				
B7	DQ0	I/O	SSTL	<b>Data Signal Bus 3:0</b>
D7	DQ1	I/O	SSTL	
D3	DQ2	I/O	SSTL	
B3	DQ3	I/O	SSTL	
<b>Data Strobe ×4 Organization</b>				
E3	DQS	I/O	SSTL	<b>Data Strobe</b>
<b>Data Mask ×4 Organization</b>				
F3	DM	I	SSTL	<b>Data Mask</b>
<b>Data Signals ×8 Organization</b>				
A8	DQ0	I/O	SSTL	<b>Data Signal Bus 7:0</b>
B7	DQ1	I/O	SSTL	
C7	DQ2	I/O	SSTL	
D7	DQ3	I/O	SSTL	
D3	DQ4	I/O	SSTL	
C3	DQ5	I/O	SSTL	
B3	DQ6	I/O	SSTL	
A2	DQ7	I/O	SSTL	
<b>Data Strobe ×8 Organization</b>				
E3	DQS	I/O	SSTL	<b>Data Strobe</b>
<b>Data Mask ×8 Organization</b>				
F3	DM	I	SSTL	<b>Data Mask</b>
<b>Data Signals ×16 Organization</b>				
A8	DQ0	I/O	SSTL	<b>Data Signal 15:0</b>
B9	DQ1	I/O	SSTL	
B7	DQ2	I/O	SSTL	
C9	DQ3	I/O	SSTL	
C7	DQ4	I/O	SSTL	
D9	DQ5	I/O	SSTL	
D7	DQ6	I/O	SSTL	
E9	DQ7	I/O	SSTL	
E1	DQ8	I/O	SSTL	
D3	DQ9	I/O	SSTL	
D1	DQ10	I/O	SSTL	
C3	DQ11	I/O	SSTL	
C1	DQ12	I/O	SSTL	
B3	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
A2	DQ15	I/O	SSTL	





HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

Ball#	Name	Pin Type	Buffer Type	Function
<b>Data Strobe ×16 Organization</b>				
E3	UDQS	I/O	SSTL	Data Strobe Upper Byte
E7	LDQS	I/O	SSTL	Data Strobe Lower Byte
<b>Data Mask ×16 Organization</b>				
F3	UDM	I	SSTL	Data Mask Upper Byte
F7	LDM	I	SSTL	Data Mask Lower Byte
<b>Power Supplies</b>				
F1	V <sub>REF</sub>	AI	—	I/O Reference Voltage
A9, B2, C8, D2, E8	V <sub>DDQ</sub>	PWR	—	I/O Driver Power Supply
A7, F8, M7	V <sub>DD</sub>	PWR	—	Power Supply
A1, B8, C2, D8, E2	V <sub>SSQ</sub>	PWR	—	Power Supply
A3, F2, M3	V <sub>SS</sub>	PWR	—	Power Supply
<b>Not Connected ×4 Organization</b>				
A2, A8, B1, B9, C1, C3, C7, C9, D1, D9, E1, E7, E9, F7, F9	NC	NC	—	Not Connected
<b>Not Connected ×8 Organization</b>				
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7, F9	NC	NC	—	Not Connected
<b>Not Connected ×16 Organization</b>				
F9	NC	NC	—	Not Connected

**TABLE 5**  
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only pin. Digital levels
O	Output. Digital levels
I/O	I/O is a bidirectional input/output signal
AI	Input. Analog levels
PWR	Power
GND	Ground
NC	Not Connected

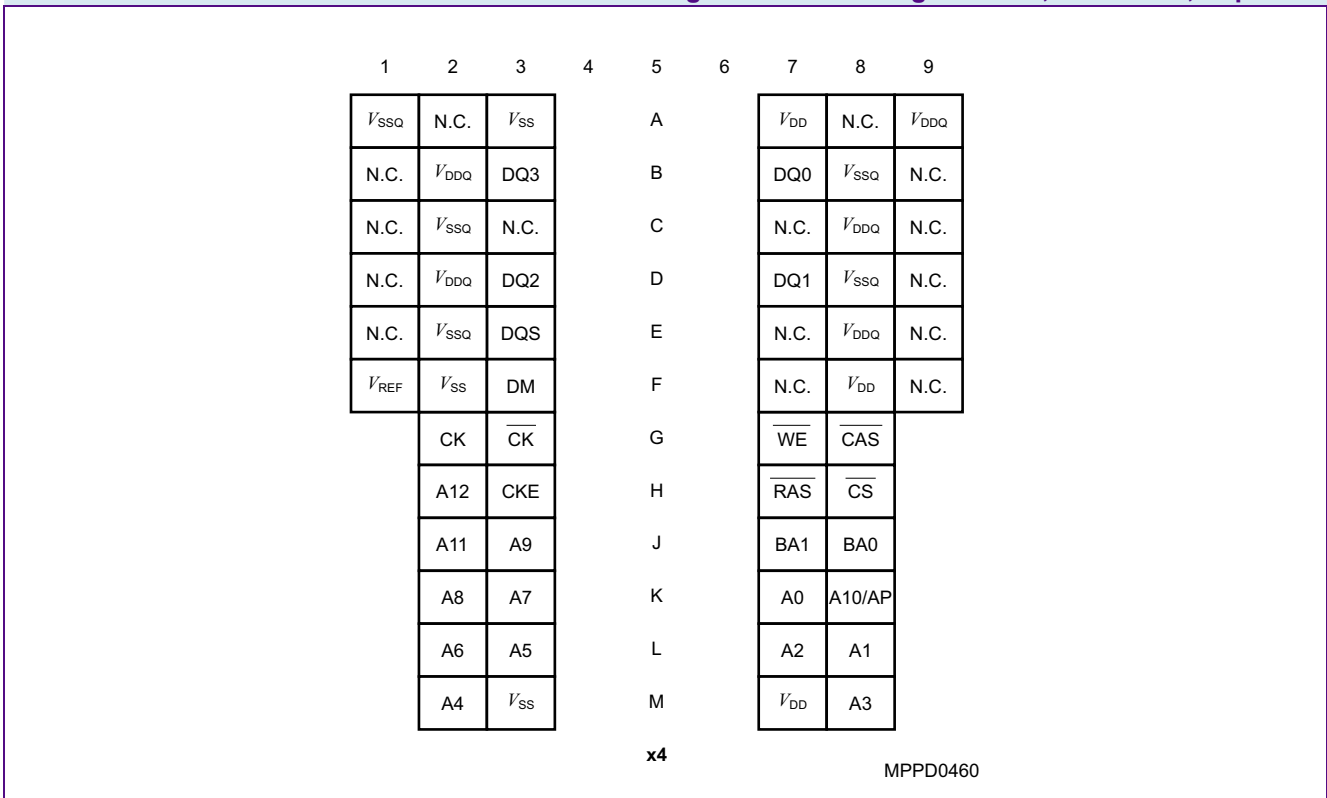


HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**TABLE 6**  
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR

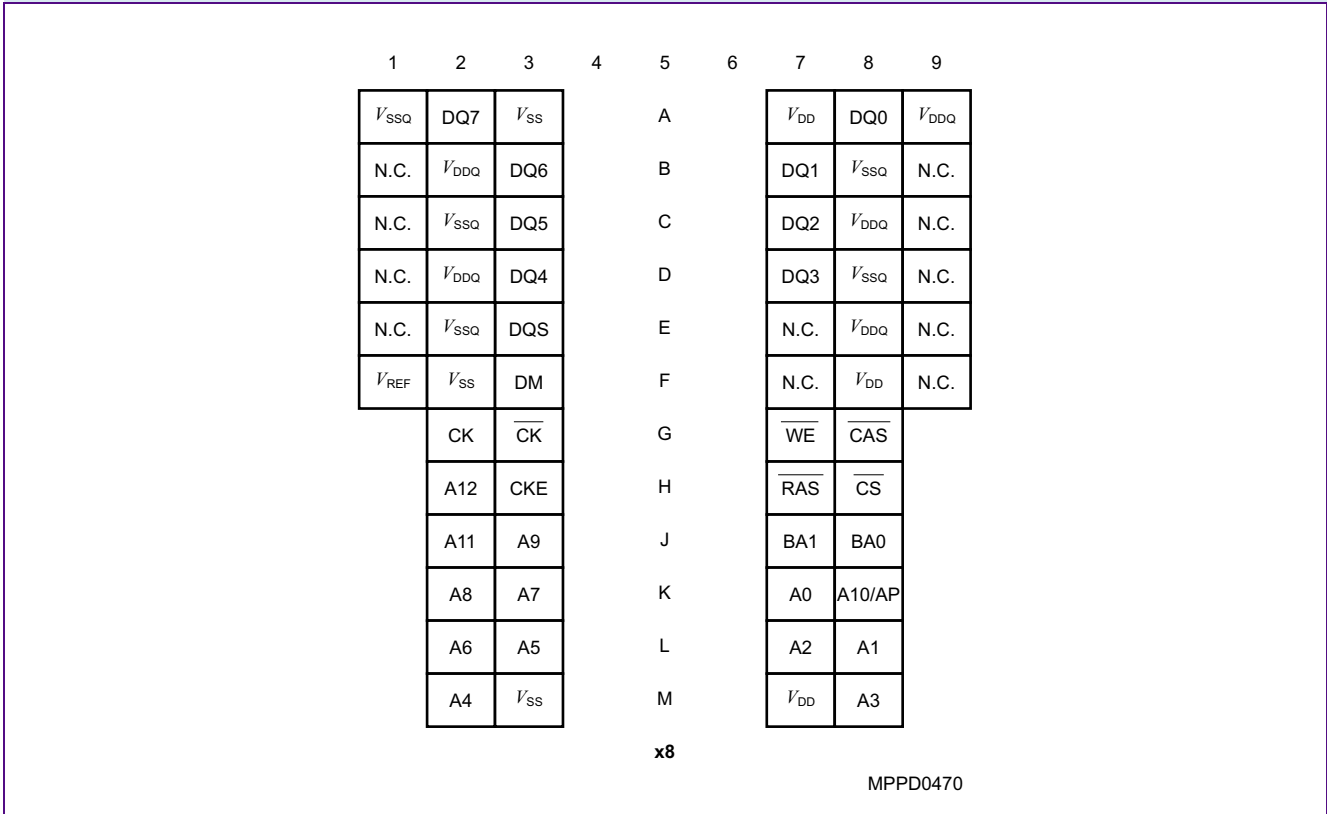
**FIGURE 1**  
Configuration for x4 Organization, TFBGA-60, Top View





HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

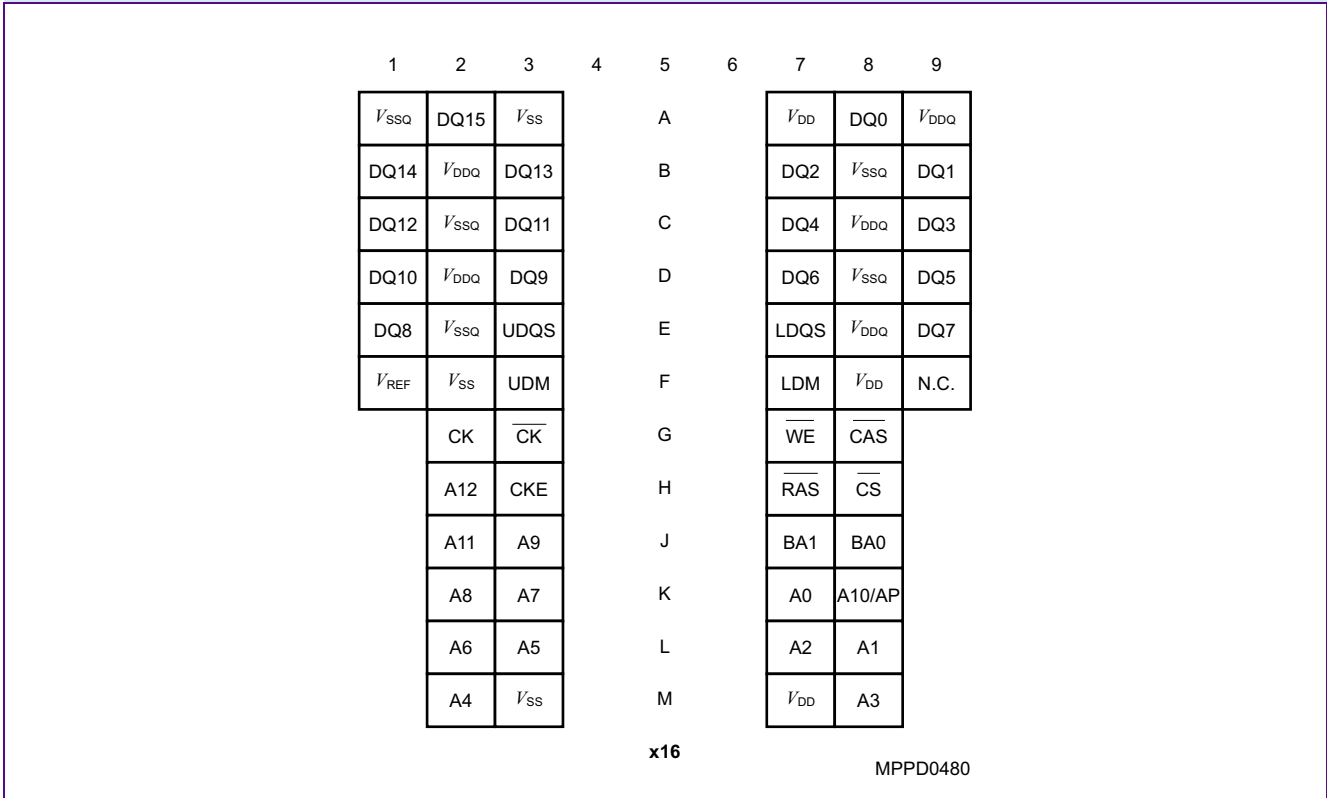
**FIGURE 2**  
Configuration for x8 Organization, TFBGA-60, Top View





HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**FIGURE 3**  
Configuration for x16 Organization, TFBGA-60, Top View





## 2.2 Configuration for TSOP11-66

The pin configuration of a DDR SDRAM is listed by function in **Table 7**. The abbreviations used in the Pin#/Buffer Type column are explained in **Table 8** and **Table 9** respectively.

**TABLE 7**  
Configuration

Pin#	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
45	CK	I	SSTL	<b>Clock Signal</b>
46	$\overline{\text{CK}}$	I	SSTL	<b>Complementary Clock Signal</b>
44	CKE	I	SSTL	<b>Clock Enable</b>
<b>Control Signals</b>				
23	$\overline{\text{RAS}}$	I	SSTL	<b>Row Address Strobe</b>
22	$\overline{\text{CAS}}$	I	SSTL	<b>Column Address Strobe</b>
21	$\overline{\text{WE}}$	I	SSTL	<b>Write Enable</b>
24	$\overline{\text{CS}}$	I	SSTL	<b>Chip Select</b>
<b>Address Signals</b>				
26	BA0	I	SSTL	<b>Bank Address Bus</b>
27	BA1	I	SSTL	
29	A0	I	SSTL	<b>Address Bus</b>
30	A1	I	SSTL	
31	A2	I	SSTL	
32	A3	I	SSTL	
35	A4	I	SSTL	
36	A5	I	SSTL	
37	A6	I	SSTL	
38	A7	I	SSTL	
39	A8	I	SSTL	
40	A9	I	SSTL	
28	A10	I	SSTL	
	AP	I	SSTL	
41	A11	I	SSTL	
42	A12	I	SSTL	
<b>Data Signals ×4 Organization</b>				
5	DQ0	I/O	SSTL	<b>Data Signal Bus 3:0</b>
11	DQ1	I/O	SSTL	
56	DQ2	I/O	SSTL	
62	DQ3	I/O	SSTL	
<b>Data Strobe ×4 Organization</b>				
51	DQS	I/O	SSTL	<b>Data Strobe</b>



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

Pin#	Name	Pin Type	Buffer Type	Function
<b>Data Mask ×4 Organization</b>				
47	DM	I	SSTL	Data Mask
<b>Data Signals × 8 Organization</b>				
2	DQ0	I/O	SSTL	Data Signal Bus 7:0
5	DQ1	I/O	SSTL	
8	DQ2	I/O	SSTL	
11	DQ3	I/O	SSTL	
56	DQ4	I/O	SSTL	
59	DQ5	I/O	SSTL	
62	DQ6	I/O	SSTL	
65	DQ7	I/O	SSTL	
<b>Data Strobe × 8 Organization</b>				
51	DQS	I/O	SSTL	Data Strobe
<b>Data Mask × 8 Organization</b>				
47	DM	I	SSTL	Data Mask
<b>Data Signals ×16 Organization</b>				
2	DQ0	I/O	SSTL	Data Signal 15:0
4	DQ1	I/O	SSTL	
5	DQ2	I/O	SSTL	
7	DQ3	I/O	SSTL	
8	DQ4	I/O	SSTL	
10	DQ5	I/O	SSTL	
11	DQ6	I/O	SSTL	
13	DQ7	I/O	SSTL	
54	DQ8	I/O	SSTL	
56	DQ9	I/O	SSTL	
57	DQ10	I/O	SSTL	
59	DQ11	I/O	SSTL	
60	DQ12	I/O	SSTL	
62	DQ13	I/O	SSTL	
63	DQ14	I/O	SSTL	
65	DQ15	I/O	SSTL	
<b>Data Strobe ×16 Organization</b>				
51	UDQS	I/O	SSTL	Data Strobe Upper Byte
16	LDQS	I/O	SSTL	Data Strobe Lower Byte
<b>Data Mask ×16 Organization</b>				
47	UDM	I	SSTL	Data Mask Upper Byte
20	LDM	I	SSTL	Data Mask Lower Byte
<b>Power Supplies</b>				
49	V <sub>REF</sub>	AI	—	I/O Reference Voltage



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

Pin#	Name	Pin Type	Buffer Type	Function
3, 9, 15, 55, 61	V <sub>DDQ</sub>	PWR	—	I/O Driver Power Supply
1, 18, 33	V <sub>DD</sub>	PWR	—	Power Supply
6, 12, 52, 58, 64	V <sub>SSQ</sub>	PWR	—	Power Supply
34,48, 66	V <sub>SS</sub>	PWR	—	Power Supply
<b>Not Connected ×4 Organization</b>				
2, 4, 7, 8, 10, 13, 14, 16, 17, 19, 20, 25, 43, 50, 53, 54, 57, 59, 60, 63, 65	NC	NC	—	Not Connected
<b>Not Connected × 8 Organization</b>				
4, 7, 10, 13, 14, 16, 17, 19, 20, 25, 43, 50, 53, 54, 57, 60, 63	NC	NC	—	
<b>Not Connected ×16 Organization</b>				
14, 17, 19, 25, 43, 50, 53	NC	NC	—	

**TABLE 8**  
Abbreviations for Pin Type

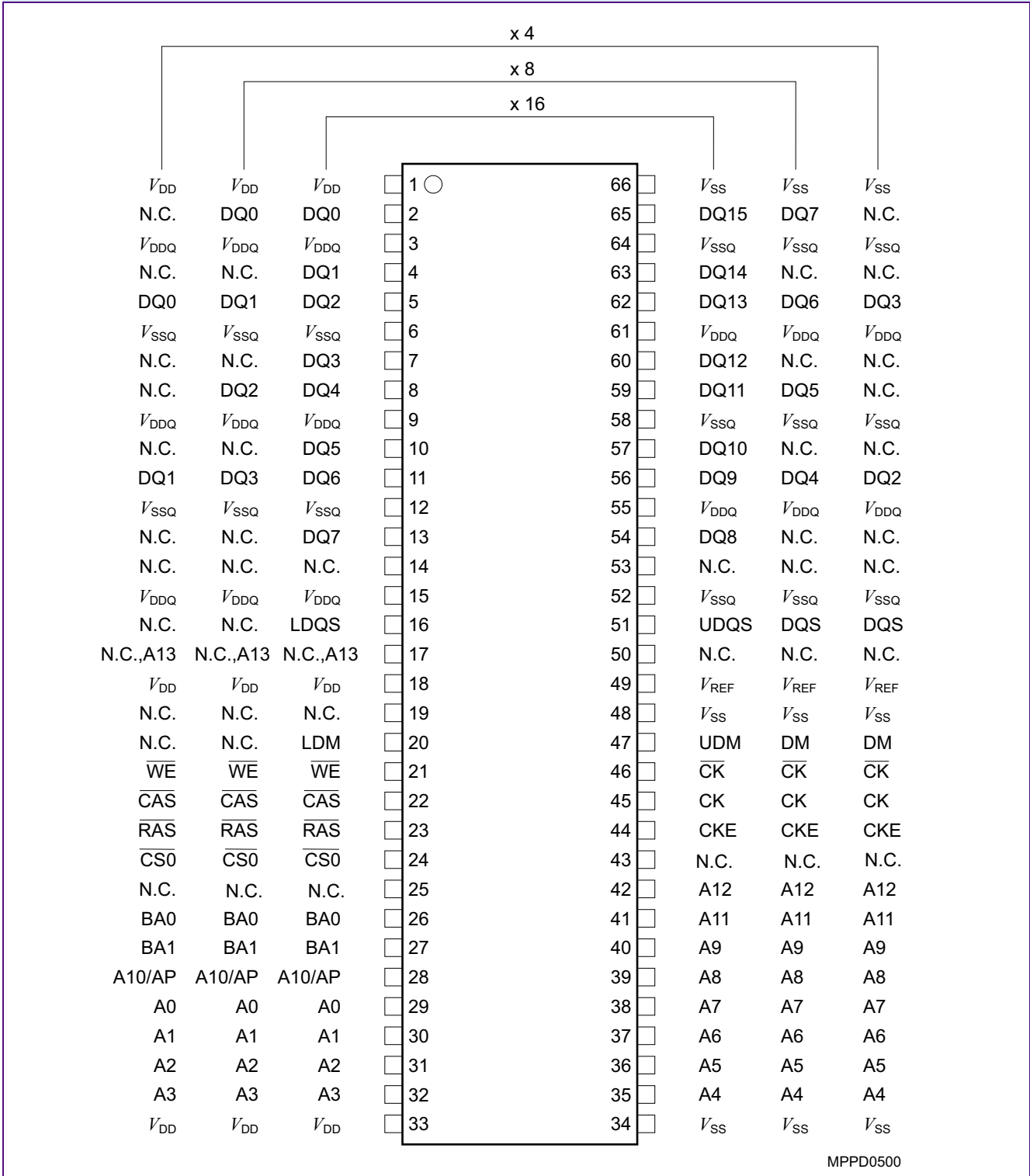
Abbreviation	Description
I	Standard input-only pin. Digital levels
O	Output. Digital levels
I/O	I/O is a bidirectional input/output signal
AI	Input. Analog levels
PWR	Power
GND	Ground
NC	Not Connected

**TABLE 9**  
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR



**FIGURE 4**  
Configuration TSOPII-66, Top View





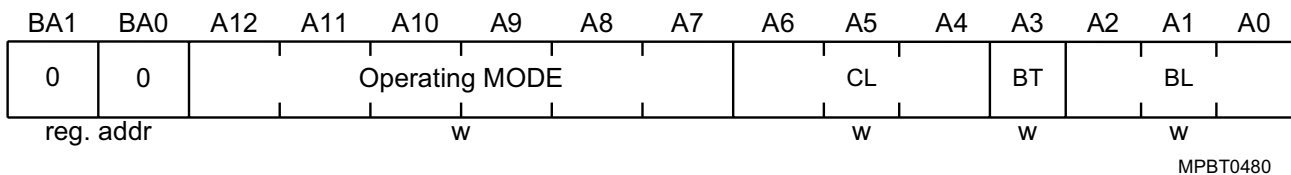


# 3 Functional Description

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation.

## 3.1 Mode Register Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM.



**TABLE 10**  
Mode Register Definition

Field	Bits	Type <sup>1)</sup>	Description
<b>BL</b>	[2:0]	W	<b>Burst Length</b> <i>Note: All other bit combinations are RESERVED.</i> 001 <sub>B</sub> 2 010 <sub>B</sub> 4 011 <sub>B</sub> 8
<b>BT</b>	3		<b>Burst Type</b> 0 Sequential 1 Interleaved
<b>CL</b>	[6:4]		<b>CAS Latency</b> <i>Note: All other bit combinations are RESERVED.</i> 010 <sub>B</sub> 2 110 <sub>B</sub> 2.5 011 <sub>B</sub> 3 100 <sub>B</sub> 4
<b>MODE</b>	[12:7]		<b>Operating Mode</b> <i>Note: All other bit combinations are RESERVED.</i> 000000 Normal Operation without DLL Reset 000010 Normal Operation with DLL Reset

1) W = write only register bit



### 3.1.1 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 11**.

**TABLE 11**  
Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

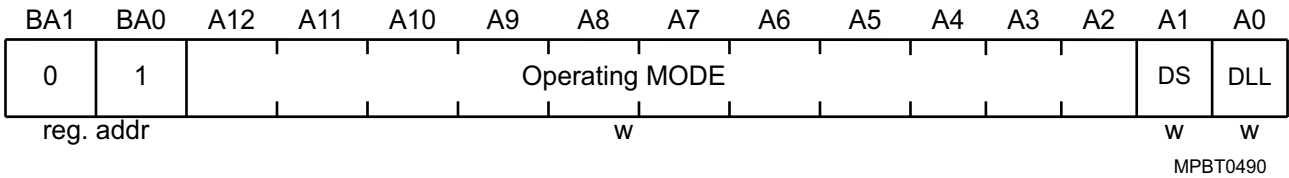
**Notes**

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data-element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.



### 3.2 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register.



**TABLE 12**  
Extended Mode Register

Field	Bits	Type <sup>1)</sup>	Description
<b>DLL</b>	0	w	<b>DLL Status</b> 0 <sub>B</sub> <b>Enabled</b> 1 <sub>B</sub> <b>Disabled</b>
<b>DS</b>	1		<b>Drive Strength</b> 0 <sub>B</sub> <b>Normal</b> 1 <sub>B</sub> <b>Weak</b>
<b>MODE</b>	[12:2]		<b>Operating Mode</b> 0000000000 <sub>B</sub> <b>Normal Operation</b>  <b>Notes</b> 1. A2 must be 0 to provide compatibility with early DDR devices. 2. All other bit combinations are RESERVED.

1) w = write only register bit



## 4 Truth Tables

The truth tables in this chapter summarize the commands and their signal coding to control a standard Double-Data-Rate SDRAM.

**TABLE 13**  
Truth Table 1: Commands

Name (Function)	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address	MNE	Note
Deselect (NOP)	H	X	X	X	X	NOP	1)2)
No Operation (NOP)	L	H	H	H	X	NOP	1)2)
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1)3)
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1)4)
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1)4)
Burst Terminate	L	H	H	L	X	BST	1)5)
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1)6)
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR/SR	1)7)8)
Mode Register Set	L	L	L	L	Op-Code	MRS	1)9)

- 1) CKE is HIGH for all commands shown except Self Refresh.  $V_{\text{REF}}$  must be maintained during Self Refresh operation.
- 2) Deselect and NOP are functionally interchangeable.
- 3) BA0, BA1 provide bank address and A0 - Ai provide row address.
- 4) BA0, BA1 provide bank address; A0 - Ai provide column address; A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.
- 5) Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.
- 6) A10 LOW: BA0, BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care".
- 7) This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW
- 8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are "Don't Care" except for CKE.
- 9) BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0 - Ai provide the op-code to be written to the selected Mode Register.

**TABLE 14**  
Truth Table 2: DM Operation

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	

- 1) Used to mask write data; provided coincident with the corresponding data.



**TABLE 15**  
**Truth Table 3: Clock Enable (CKE)**

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	1)
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	2)
Power Down	L	L	X	Maintain Power-Down	–
Power Down	L	H	Deselect or NOP	Exit Power-Down	–
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	–
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	–
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	–
	H	H	See <b>Table 16</b>	–	–

- 1)  $V_{REF}$  must be maintained during Self Refresh operation
- 2) Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit ( $t_{XSNR}$ ) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

- 1. CKEn is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
- 2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
- 3. COMMAND n is the command registered at clock edge n, and ACTION n is a result of COMMAND n.
- 4. All states and sequences not shown are illegal or reserved.



**TABLE 16**

**Truth Table 4: Current State Bank n - Command to Bank n (same bank)**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1)2)3)4)5)6)
Idle	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	L	L	H	AUTO REFRESH	–	1)2)3)4)5)6)7)
	L	L	L	L	MODE REGISTER SET	–	1)2)3)4)5)6)7)
Row Active	L	H	L	H	Read	Select column and start Read burst	1)2)3)4)5)6)8)
	L	H	L	L	Write	Select column and start Write burst	1)2)3)4)5)6)8)
	L	L	H	L	Precharge	Deactivate row in bank(s)	1)2)3)4)5)6)9)
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1)2)3)4)5)6)8)
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1)2)3)4)5)6)9)
	L	H	H	L	BURST TERMINATE	BURST TERMINATE	1)2)3)4)5)6)10)
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1)2)3)4)5)6)8)11)
	L	H	L	L	Write	Select column and start Write burst	1)2)3)4)5)6)8)
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1)2)3)4)5)6)9)11)

- 1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 15** and after  $t_{XSNR}/t_{XSRD}$  has been met (if the previous state was self refresh).
- 2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
- 3) Current state definitions: Idle: The bank has been precharged, and  $t_{RP}$  has been met. Row Active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress. Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated. Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- 4) The following states must not be interrupted by a command issued to the same bank. Precharging: Starts with registration of a Precharge command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, the bank is in the idle state. Row Activating: Starts with registration of an Active command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the bank is in the “row active” state. Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank is in the idle state. Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank is in the idle state. Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 17**.
- 5) The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states. Refreshing: Starts with registration of an Auto Refresh command and ends when  $t_{RFC}$  is met. Once  $t_{RFC}$  is met, the DDR SDRAM is in the “all banks idle” state. Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when  $t_{MRD}$  has been met. Once  $t_{MRD}$  is met, the DDR SDRAM is in the “all banks idle” state. Precharging All: Starts with registration of a Precharge All command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, all banks is in the idle state.
- 6) All states and sequences not shown are illegal or reserved.
- 7) Not bank-specific; requires that all banks are idle.
- 8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
- 9) May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
- 10) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
- 11) Requires appropriate DM masking.



**TABLE 17**

**Truth Table 5: Current State Bank n - Command to Bank m (different bank)**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation	1)2)3)4)5)6)
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	–	1)2)3)4)5)6)
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	H	L	H	Read	Select column and start Read burst	1)2)3)4)5)6)7)
	L	H	L	L	Write	Select column and start Write burst	1)2)3)4)5)6)7)
	L	L	H	L	Precharge	–	1)2)3)4)5)6)
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	H	L	H	Read	Select column and start new Read burst	1)2)3)4)5)6)7)
	L	L	H	L	Precharge	–	1)2)3)4)5)6)
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	H	L	H	Read	Select column and start Read burst	1)2)3)4)5)6)7)8)
	L	H	L	L	Write	Select column and start new Write burst	1)2)3)4)5)6)7)
	L	L	H	L	Precharge	–	1)2)3)4)5)6)
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	H	L	H	Read	Select column and start new Read burst	1)2)3)4)5)6)7)9)
	L	H	L	L	Write	Select column and start Write burst	1)2)3)4)5)6)7)9)10)
	L	L	H	L	Precharge	–	1)2)3)4)5)6)
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1)2)3)4)5)6)
	L	H	L	H	Read	Select column and start Read burst	1)2)3)4)5)6)7)9)
	L	H	L	L	Write	Select column and start new Write burst	1)2)3)4)5)6)7)9)
	L	L	H	L	Precharge	–	1)2)3)4)5)6)

- 1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 15**: Clock Enable (CKE) and after  $t_{XSNR}/t_{XSRD}$  has been met, if the previous state was self refresh)
- 2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
- 3) Current state definitions: Idle: The bank has been precharged, and  $t_{RP}$  has been met. Row Active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress. Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated. Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- 4) AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.
- 5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
- 6) All states and sequences not shown are illegal or reserved.
- 7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
- 8) Requires appropriate DM masking.
- 9) **Concurrent Auto Precharge:** This device supports “Concurrent Auto Precharge”. When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data

HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The minimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in **Table 18**.

10) A Write command may be applied after the completion of data output.

**TABLE 18****Truth Table 6: Concurrent Auto Precharge**

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Unit
WRITE w/AP	Read or Read w/AP	$1 + (BL/2) + t_{WTR}$	$t_{CK}$
	Write to Write w/AP	$BL/2$	$t_{CK}$
	Precharge or Activate	1	$t_{CK}$
Read w/AP	Read or Read w/AP	$BL/2$	$t_{CK}$
	Write or Write w/AP	$CL \text{ (rounded up)} + BL/2$	$t_{CK}$
	Precharge or Activate	1	$t_{CK}$





## 5 Electrical Characteristics

This chapter describes the electrical characteristics.

### 5.1 Operating Conditions

This chapter contains the operating conditions tables.

**TABLE 19**  
Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	—	$V_{DDQ} + 0.5$	V	—
Voltage on inputs relative to $V_{SS}$	$V_{IN}$	-1	—	+3.6	V	—
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1	—	+3.6	V	—
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1	—	+3.6	V	—
Operating temperature (ambient)	$T_A$	0	—	+70	°C	for HYB...
		-40	—	+85	°C	for HYI...
Storage temperature (plastic)	$T_{STG}$	-55	—	+150	°C	—
Power dissipation (per SDRAM component)	$P_D$	—	1	—	W	—
Short circuit output current	$I_{OUT}$	—	50	—	mA	—

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**TABLE 20**  
**Input and Output Capacitances**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input Capacitance: CK, $\overline{\text{CK}}$	C <sub>I1</sub>	2.0	—	3.0	pF	TSOPII <sup>1)</sup>
		1.5	—	2.5	pF	TFBGA <sup>1)</sup>
Delta Input Capacitance	C <sub>dl1</sub>	—	—	0.25	pF	<sup>1)</sup>
Input Capacitance: All other input-only pins	C <sub>I2</sub>	1.5	—	2.5	pF	TFBGA <sup>1)</sup>
		2.0	—	3.0	pF	TSOPII <sup>1)</sup>
Delta Input Capacitance: All other input-only pins	C <sub>dIO</sub>	—	—	0.5	pF	<sup>1)</sup>
Input/Output Capacitance: DQ, DQS, DM	C <sub>IO</sub>	3.5	—	4.5	pF	TFBGA <sup>1)2)</sup>
		4.0	—	5.0	pF	TSOPII <sup>1)2)</sup>
Delta Input/Output Capacitance: DQ, DQS, DM	C <sub>dIO</sub>	—	—	0.5	pF	<sup>1)</sup>

- 1) These values are guaranteed by design and are tested on a sample base only.  $V_{DDQ} = V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $f = 100 \text{ MHz}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ ,  $V_{OUT(DC)} = V_{DDQ}/2$ ,  $V_{OUT}$  (Peak to Peak) 0.2 V. Unused pins are tied to ground.
- 2) DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.



**TABLE 21**  
**Electrical Characteristics and DC Operating Conditions**

Parameter	Symbol	Values			Unit	Note/Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
Device Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V	$f_{CK} \leq 200$ MHz
Output Supply Voltage	$V_{DDQ}$	2.3	2.5	2.7	V	$f_{CK} \leq 200$ MHz <sup>2)</sup>
Supply Voltage, I/O Supply Voltage	$V_{SS}, V_{SSQ}$	0		0	V	—
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	<sup>3)</sup>
I/O Termination Voltage (System)	$V_{TT}$	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	<sup>4)</sup>
Input High (Logic1) Voltage	$V_{IH,DC}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	<sup>5)</sup>
Input Low (Logic0) Voltage	$V_{IL,DC}$	-0.3		$V_{REF} - 0.15$	V	<sup>5)</sup>
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN,DC}$	-0.3		$V_{DDQ} + 0.3$	V	<sup>5)</sup>
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID,DC}$	0.36		$V_{DDQ} + 0.6$	V	<sup>5)6)</sup>
VI-Matching Pull-up Current to Pull-down Current	$V_{I,Ratio}$	0.71		1.4	—	<sup>7)</sup>
Input Leakage Current	$I_I$	-2		2	$\mu$ A	Any input $0 \text{ V} \leq V_{IN} \leq V_{DD}$ ; All other pins not under test = 0 V <sup>8)</sup>
Output Leakage Current	$I_{OZ}$	-5		5	$\mu$ A	DQs are disabled; $0 \text{ V} \leq V_{OUT} \leq V_{DDQ}$ <sup>8)</sup>
Output High Current, Normal Strength Driver	$I_{OH}$	—		-16.2	mA	$V_{OUT} = 1.95 \text{ V}$
Output Low Current, Normal Strength Driver	$I_{OL}$	16.2		—	mA	$V_{OUT} = 0.35 \text{ V}$

- 1)  $0 \text{ }^\circ\text{C} \leq T_A \leq 70 \text{ }^\circ\text{C}$ ;  $V_{DD} = V_{DDQ} = 2.5 \text{ V} \pm 0.2 \text{ V}$
- 2) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- 3) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF,DC}$ .  $V_{REF}$  is also expected to track noise variations in  $V_{DDQ}$ .
- 4)  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$ .
- 5) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 6)  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
- 7) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 8) Values are shown per pin.

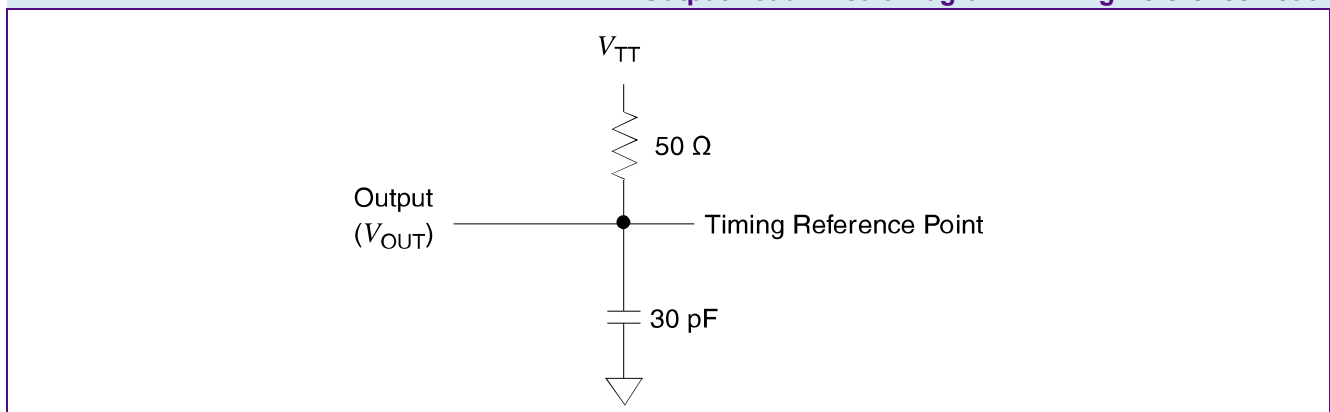


## 5.2 AC Characteristics

Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions,  $I_{DD}$  Specifications and Conditions, and Electrical Characteristics and AC Timing.

### Notes

1. All voltages referenced to  $V_{SS}$ .
2. Tests for AC timing,  $I_{DD}$ , and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. **Figure 5** represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).
4. AC timing and  $I_{DD}$  tests may use a  $V_{IL}$  to  $V_{IH}$  swing of up to 1.5 V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for CK,  $\overline{CK}$ ), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between  $V_{IL(AC)}$  and  $V_{IH(AC)}$ .
5. The AC and DC input level specifications are as defined in the SSTL\_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level).
6. For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating, DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp  $V-I$  characteristics see the latest Industry specification for DDR components.

**FIGURE 5****AC Output Load Circuit Diagram / Timing Reference Load**



**TABLE 22**  
**AC Operating Conditions**

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Input High (Logic 1) Voltage, DQ, DQS and DM Signals	$V_{IH.AC}$	$V_{REF} + 0.31$	—	V	1)2)3)
Input Low (Logic 0) Voltage, DQ, DQS and DM Signals	$V_{IL.AC}$	—	$V_{REF} - 0.31$	V	1)2)3)
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID.AC}$	0.7	$V_{DDQ} + 0.6$	V	1)2)3)4)
Input Closing Point Voltage, CK and $\overline{CK}$ Inputs	$V_{IX.AC}$	$0.5 \times V_{DDQ} - 0.2$	$0.5 \times V_{DDQ} + 0.2$	V	1)2)3)5)

- 1)  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ;  $V_{DD} = V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$
- 2) Input slew rate = 1 V/ns.
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 4)  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
- 5) The value of  $V_{IX}$  is expected to equal  $0.5 \times V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.

**TABLE 23**  
**AC Timing - Absolute Specifications**

Parameter	Symbol	-5		-6		Unit	Note/ Test Condition <sup>1)</sup>
		DDR400		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/ $\overline{CK}$	$t_{AC}$	-0.7	+0.7	-0.7	+0.7	ns	2)3)4)5)
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Clock cycle time	$t_{CK}$	5	12	6	12	ns	CL = 4.0 2)3)4)5)
		5	12	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Auto precharge write recovery + precharge time	$t_{DAL}$	Min. : $(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$ , Max. : —				$t_{CK}$	2)3)4)5)6)
DQ and DM input hold time	$t_{DH}$	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	$t_{DIPW}$	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/ $\overline{CK}$	$t_{DQSK}$	-0.6	+0.6	-0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{DQSQ}$	—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{DQSQ}$	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
Write command to 1 <sup>st</sup> DQS latching transition	$t_{DQSS}$	0.72	1.25	0.75	1.25	$t_{CK}$	2)3)4)5)



**HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM**

Parameter	Symbol	-5		-6		Unit	Note/ Test Condition <sup>1)</sup>
		DDR400		DDR333			
		Min.	Max.	Min.	Max.		
DQ and DM input setup time	$t_{DS}$	0.4	—	0.45	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
Clock Half Period	$t_{HP}$	min. ( $t_{CL}$ , $t_{CH}$ )	—	min. ( $t_{CL}$ , $t_{CH}$ )	—	ns	2)3)4)5)
Data-out high-impedance time from CK/ $\overline{CK}$	$t_{HZ}$	—	+0.7	—	+0.7	ns	2)3)4)5)7)
Address and control input hold time	$t_{IH}$	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	$t_{IPW}$	2.2	—	2.2	—	ns	2)3)4)5)9)
Address and control input setup time	$t_{IS}$	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Data-out low-impedance time from CK/ $\overline{CK}$	$t_{LZ}$	-0.7	+0.7	-0.7	+0.7	ns	2)3)4)5)7)
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	2)3)4)5)
DQ/DQS output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
Data hold skew factor	$t_{QHS}$	—	+0.50	—	+0.55	ns	TSOPII <sup>2)3)4)5)</sup>
Data hold skew factor	$t_{QHS}$	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
Active to Autoprecharge delay	$t_{RAP}$	$t_{RCD}$	—	$t_{RCD}$	—	ns	2)3)4)5)
Active to Precharge command	$t_{RAS}$	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	$t_{RC}$	55	—	60	—	ns	2)3)4)5)
Active to Read or Write delay	$t_{RCD}$	15	—	18	—	ns	2)3)4)5)
Average Periodic Refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu$ s	2)3)4)5)8)
Auto-refresh to Active/Auto-refresh command period	$t_{RFC}$	68	—	72	—	ns	2)3)4)5)
Precharge command period	$t_{RP}$	15	—	18	—	ns	2)3)4)5)
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	2)3)4)5)
Read postamble	$t_{RPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)
Active bank A to Active bank B command	$t_{RRD}$	10	—	12	—	ns	2)3)4)5)



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

Parameter	Symbol	-5		-6		Unit	Note/ Test Condition <sup>1)</sup>
		DDR400		DDR333			
		Min.	Max.	Min.	Max.		
Write preamble	$t_{WPRES}$	Max. (0.25 × $t_{CK}$ , 1.5 ns)	—	Max. (0.25 × $t_{CK}$ , 1.5 ns)	—	ns	2)3)4)5)
Write preamble setup time	$t_{WPRES}$	0	—	0	—	ns	2)3)4)5)10)
Write postamble	$t_{WPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)11)
Write recovery time	$t_{WR}$	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	$t_{WTR}$	2	—	1	—	$t_{CK}$	2)3)4)5)
Exit self-refresh to non-read command	$t_{XSNR}$	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	2)3)4)5)

- 1)  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$
- 2) Input slew rate  $\geq 1\text{ V/ns}$ .
- 3) The CK/ $\overline{\text{CK}}$  input reference level (for timing reference to CK/ $\overline{\text{CK}}$ ) is the point at which CK and  $\overline{\text{CK}}$  cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$ , is  $V_{REF}$ . CK/ $\overline{\text{CK}}$  slew rate are  $\geq 1.0\text{ V/ns}$ .
- 4) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is  $V_{TT}$ .
- 6) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  is equal to the actual system clock cycle time.
- 7)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) Fast slew rate  $\geq 1.0\text{ V/ns}$ , slow slew rate  $\geq 0.5\text{ V/ns}$  and  $< 1\text{ V/ns}$  for command/address and CK &  $\overline{\text{CK}}$  slew rate  $> 1.0\text{ V/ns}$ , measured between  $V_{IH,AC}$  and  $V_{IL,AC}$ .
- 9) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 10) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on  $t_{DQSS}$ .
- 11) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.



**TABLE 24**  
 **$I_{DD}$  Conditions**

Parameter	Symbol
<b>Operating Current:</b> one bank; active/ precharge; $t_{RC} = t_{RCMIN}$ ; $t_{CK} = t_{CKMIN}$ ; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	$I_{DD0}$
<b>Operating Current:</b> one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	$I_{DD1}$
<b>Precharge Power-Down Standby Current:</b> all banks idle; power-down mode; $CKE \leq V_{ILMAX}$ ; $t_{CK} = t_{CKMIN}$	$I_{DD2P}$
<b>Precharge Floating Standby Current:</b> $\overline{CS} \geq V_{IHMIN}$ , all banks idle; $CKE \geq V_{IHMIN}$ ; $t_{CK} = t_{CKMIN}$ , address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD2F}$
<b>Precharge Quiet Standby Current:</b> $\overline{CS} \geq V_{IHMIN}$ , all banks idle; $CKE \geq V_{IHMIN}$ ; $t_{CK} = t_{CKMIN}$ , address and other control inputs stable at $\geq V_{IHMIN}$ or $\leq V_{ILMAX}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD2Q}$
<b>Active Power-Down Standby Current:</b> one bank active; power-down mode; $CKE \leq V_{ILMAX}$ ; $t_{CK} = t_{CKMIN}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD3P}$
<b>Active Standby Current:</b> one bank active; $\overline{CS} \geq V_{IHMIN}$ ; $CKE \geq V_{IHMIN}$ ; $t_{RC} = t_{RASMAX}$ ; $t_{CK} = t_{CKMIN}$ ; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	$I_{DD3N}$
<b>Operating Current:</b> one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$ ; $I_{OUT} = 0$ mA	$I_{DD4R}$
<b>Operating Current:</b> one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$	$I_{DD4W}$
<b>Auto-Refresh Current:</b> $t_{RC} = t_{RFCMIN}$ , burst refresh	$I_{DD5}$
<b>Self-Refresh Current:</b> $CKE \leq 0.2$ V; external clock on; $t_{CK} = t_{CKMIN}$	$I_{DD6}$
<b>Operating Current:</b> four bank; four bank interleaving with BL = 4; Refer to the following page for detailed test conditions.	$I_{DD7}$





**TABLE 25**  
 **$I_{DD}$  Specification**

Symbol	-5	-6	Unit	Note <sup>1)</sup>
	DDR400B	DDR333B		
	Max.	Max.		
$I_{DD0}$	65	57	mA	$\times 4/\times 8$ <sup>2)3)</sup>
	69	60	mA	$\times 16$ <sup>3)</sup>
$I_{DD1}$	72	62	mA	$\times 4/\times 8$ <sup>3)</sup>
	78	68	mA	$\times 16$ <sup>3)</sup>
$I_{DD2P}$	4,6	4,6	mA	<sup>3)</sup>
$I_{DD2F}$	30	27	mA	<sup>3)</sup>
$I_{DD2Q}$	22	20	mA	<sup>3)</sup>
$I_{DD3P}$	14	14	mA	<sup>3)</sup>
$I_{DD3N}$	37	34	mA	$\times 4/\times 8$ <sup>3)</sup>
	37	34	mA	$\times 16$ <sup>3)</sup>
$I_{DD4R}$	69	64	mA	$\times 4/\times 8$ <sup>3)</sup>
	88	77	mA	$\times 16$ <sup>3)</sup>
$I_{DD4W}$	69	64	mA	$\times 4/\times 8$ <sup>3)</sup>
	85	74	mA	$\times 16$ <sup>3)</sup>
$I_{DD5}$	146	126	mA	<sup>3)</sup>
$I_{DD6}$	5	5	mA	<sup>4)</sup>
$I_{DD6\_low\ power}$	2,5	2,5	mA	Low power
$I_{DD7}$	198	178	mA	$\times 4/\times 8$ <sup>3)</sup>
	213	167	mA	$\times 16$ <sup>3)</sup>

- 1) Test conditions :  $V_{DD} = 2.7\text{ V}$ ,  $T_A = 10\text{ °C}$ .
- 2)  $I_{DD}$  specifications are tested after the device is properly initialized and measured at 200 MHz.
- 3) Input slew rate = 1 V/ns.
- 4) Enables on-chip refresh and address counters.

HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

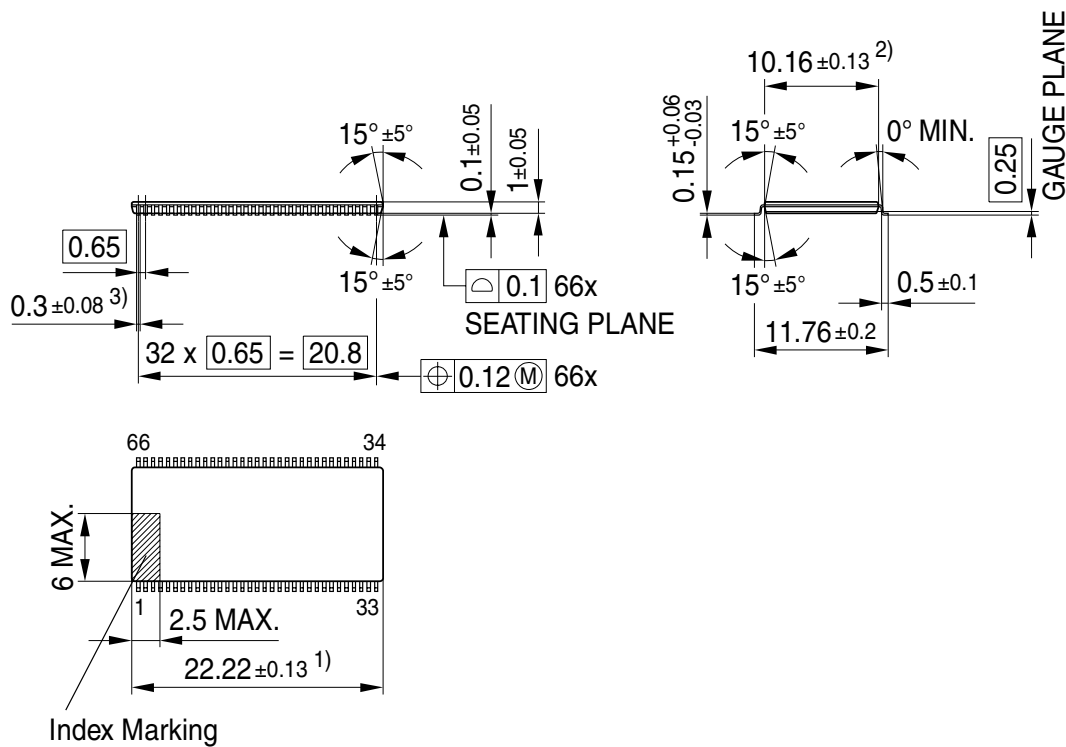
## 6 Package Outlines

The package used for this product family.

### Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances  $\pm 0.15$

**FIGURE 6**  
Package Outline P(G)-TSOPII-66



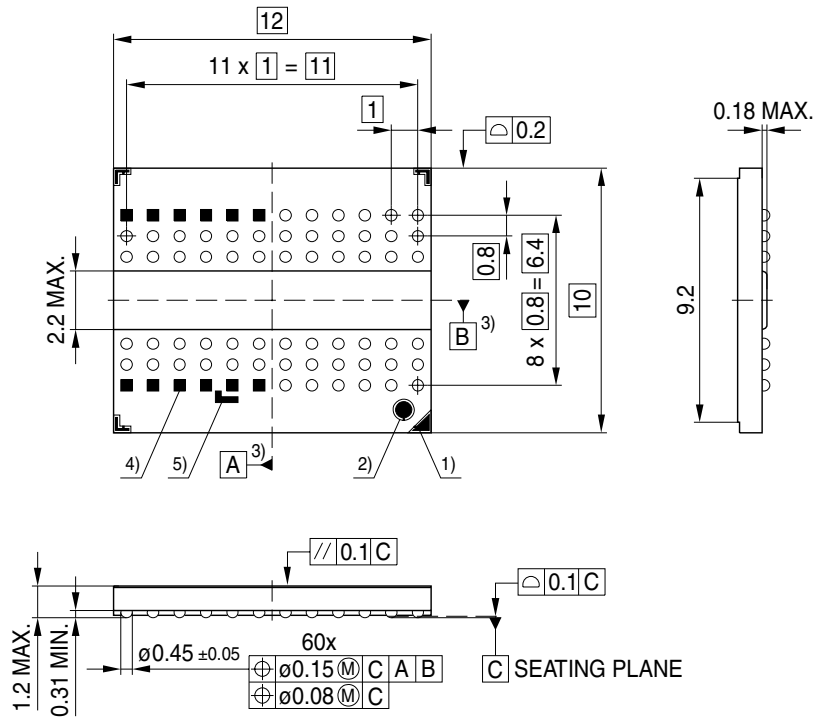
- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include plastic protrusion of 0.25 max. per side
- 3) Does not include dambar protrusion of 0.13 max.

FPO\_P\_-TSOPII\_-066-001



HY[B/I]25D512[40/80/16]0D[C/E/F/T](L)  
512-Mbit Double-Data-Rate SDRAM

**FIGURE 7**  
Package Outline PG-TFBGA-60



Lead free solder balls (green solder balls)

- 1) Package orientation mark A1
- 2) Bad unit marking (BUM) (light = good)
- 3) Middle of packages edges
- 4) Dummy pads without ball ■
- 5) SBA fiducial (solder ball attach)

FPO\_PG-TFBGA\_\_060-062



# 7 Product Nomenclature

For reference the Qimonda SDRAM component nomenclature is enclosed in this chapter.

**TABLE 26**  
Example for Nomenclature Fields

Example for	Field Number									
	1	2	3	4	5	6	7	8	9	10
DDR SDRAM	HYB	25	D	512	80	0	D	E		-5

**TABLE 27**  
DDR Memory Components

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Memory components
		HYI	Memory components, industrial temperature range (-40°C – +85 °C)
2	Interface Voltage [V]	25	2.5 V
3	DRAM Technology	D	Double Data Rate SDRAM
4	Component Density [Mbit]	64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		512	512 Mbit
5	Number of I/Os	40	×4
		80	×8
		16	×16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
		D	Fourth
8	Package, Lead-Free Status	C	FBGA, lead containing
		E	TSOP, lead- and halogen-free
		F	FBGA, lead- and halogen-free
		T	TSOP, lead containing
9	Power	–	Standard power product
10	Speed Grade	–4	DDR500B
		–4A	DDR500A
		–5	DDR400B
		–5A	DDR400A
		–6	DDR333B



# List of Illustrations

Figure 1	Configuration for x4 Organization, TFBGA-60, Top View . . . . .	10
Figure 2	Configuration for x8 Organization, TFBGA-60, Top View . . . . .	11
Figure 3	Configuration for x16 Organization, TFBGA-60, Top View . . . . .	12
Figure 4	Configuration TSOP168, Top View . . . . .	16
Figure 5	AC Output Load Circuit Diagram / Timing Reference Load . . . . .	28
Figure 6	Package Outline P(G)-TSOP168 . . . . .	34
Figure 7	Package Outline PG-TFBGA-60 . . . . .	35



# List of Tables

Table 1	Performance . . . . .	3
Table 2	Ordering Information for RoHS Compliant Products . . . . .	5
Table 3	Ordering Information for Lead-Containing Products . . . . .	6
Table 4	Configuration . . . . .	7
Table 5	Abbreviations for Ball Type . . . . .	9
Table 6	Abbreviations for Buffer Type . . . . .	10
Table 7	Configuration . . . . .	13
Table 8	Abbreviations for Pin Type . . . . .	15
Table 9	Abbreviations for Buffer Type . . . . .	15
Table 10	Mode Register Definition . . . . .	17
Table 11	Burst Definition . . . . .	18
Table 12	Extended Mode Register . . . . .	19
Table 13	Truth Table 1: Commands . . . . .	20
Table 14	Truth Table 2: DM Operation . . . . .	20
Table 15	Truth Table 3: Clock Enable (CKE) . . . . .	21
Table 16	Truth Table 4: Current State Bank n - Command to Bank n (same bank) . . . . .	22
Table 17	Truth Table 5: Current State Bank n - Command to Bank m (different bank) . . . . .	23
Table 18	Truth Table 6: Concurrent Auto Precharge . . . . .	24
Table 19	Absolute Maximum Ratings . . . . .	25
Table 20	Input and Output Capacitances . . . . .	26
Table 21	Electrical Characteristics and DC Operating Conditions . . . . .	27
Table 22	AC Operating Conditions . . . . .	29
Table 23	AC Timing - Absolute Specifications . . . . .	29
Table 24	I <sub>DD</sub> Conditions . . . . .	32
Table 25	I <sub>DD</sub> Specification . . . . .	33
Table 26	Example for Nomenclature Fields . . . . .	36
Table 27	DDR Memory Components . . . . .	36



# Contents

<b>1</b>	<b>Overview</b> .....	<b>3</b>
1.1	Features .....	3
1.2	Description .....	4
<b>2</b>	<b>Configuration</b> .....	<b>7</b>
2.1	Configuration for TFBGA-60 .....	7
2.2	Configuration for TSOPII-66 .....	13
<b>3</b>	<b>Functional Description</b> .....	<b>17</b>
3.1	Mode Register Definition .....	17
3.1.1	Burst Type .....	18
3.2	Extended Mode Register .....	19
<b>4</b>	<b>Truth Tables</b> .....	<b>20</b>
<b>5</b>	<b>Electrical Characteristics</b> .....	<b>25</b>
5.1	Operating Conditions .....	25
5.2	AC Characteristics .....	28
<b>6</b>	<b>Package Outlines</b> .....	<b>34</b>
<b>7</b>	<b>Product Nomenclature</b> .....	<b>36</b>

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