FAIRCHILD
A Schlumberger Company

F100165
Universal Priority Encoder

F100K ECL Product

Description

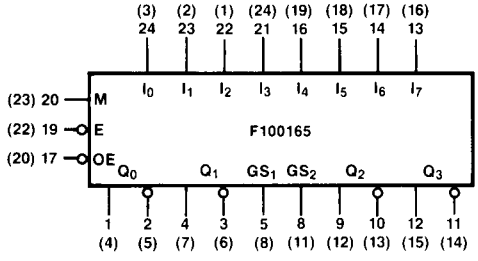
The F100165 contains eight input latches with a common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a signal 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0-I_3. Q_2, Q_3 and GS_2 operate with I_4-I_7. A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

Pin Names

I_0-I_7	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
M	Mode Control Input
GS_1-GS_2	Group Signal Outputs
Q_0-Q_3	Data Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Data Outputs

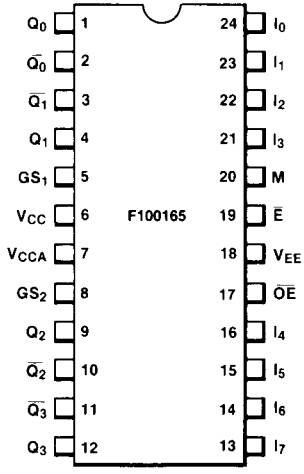
Logic Symbol



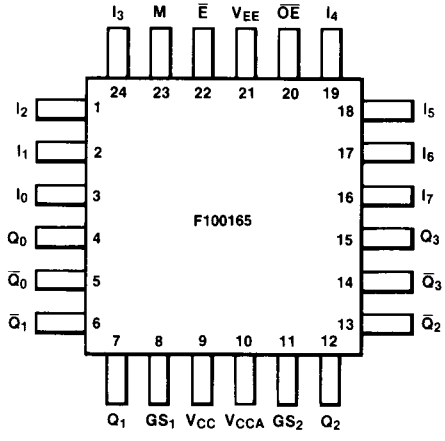
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



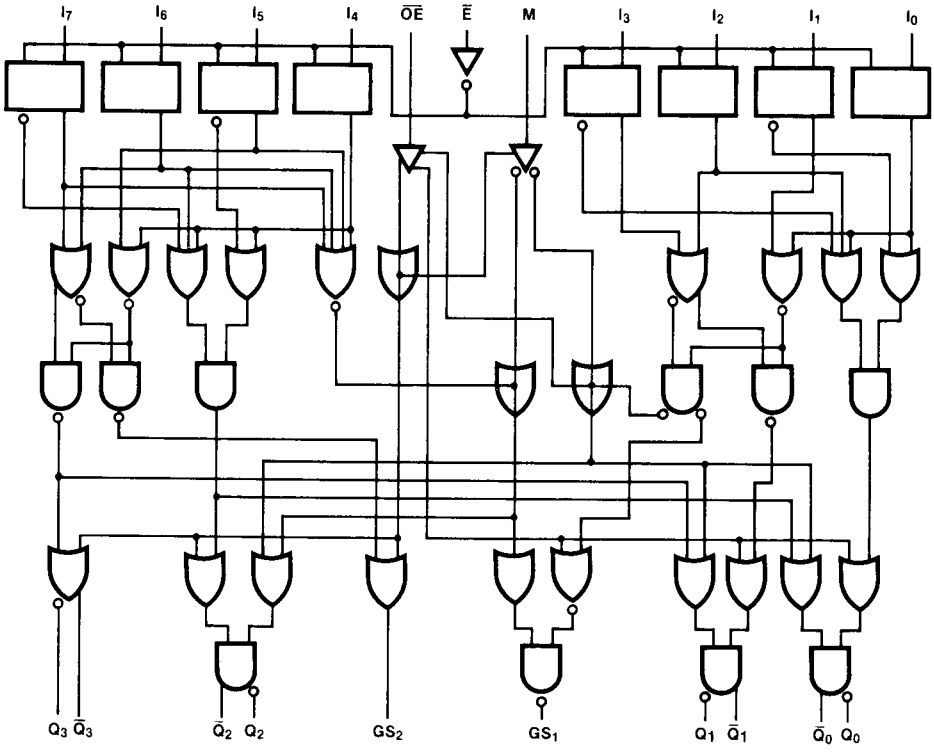
24-Pin Flatpak (Top View)



Ordering Information

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Truth Table

Inputs											Outputs					
$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0-I_7 when $\overline{E}$ was LOW and M = L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0-I_7 when $\overline{E}$ was LOW and M = H					

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			230	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−200	−140	−77	mA	Inputs Open

*See Family Characteristics for other dc specifications.

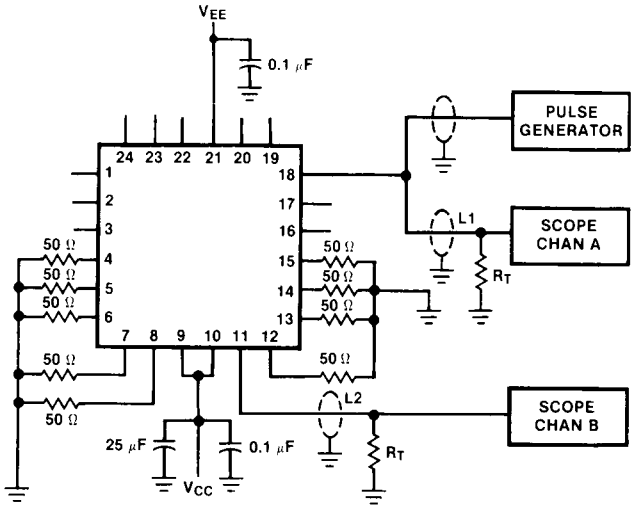
Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to Q_0-Q_3, $\overline{Q_0}$-$\overline{Q_3}$ (Transparent Mode)	1.10	4.10	1.10	4.10	1.10	4.60	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode)	1.30	3.90	1.30	3.90	1.30	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0-Q_3, $\overline{Q_0}$-$\overline{Q_3}$	1.00	3.00	1.00	3.00	1.10	3.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1-GS_2	1.10	2.60	1.10	2.60	1.20	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0-Q_3, $\overline{Q_0}$-$\overline{Q_3}$	0.90	3.60	1.00	3.60	1.00	3.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0-Q_3, $\overline{Q_0}$-$\overline{Q_3}$	1.50	4.70	1.50	4.60	1.50	5.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 1, 2* and *3*
t_s	Setup Time I_0-I_7	1.00		0.90		1.00		ns	*Figure 4*
t_h	Hold Time I_0-I_7	1.20		1.20		1.20		ns	
$t_{pw(L)}$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$ (Transparent Mode)	1.10	3.90	1.10	3.90	1.10	4.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode)	1.30	3.70	1.30	3.70	1.30	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.00	2.80	1.00	2.80	1.10	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1-GS_2	1.10	2.40	1.10	2.40	1.20	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	0.90	3.40	1.00	3.40	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.50	4.50	1.50	4.40	1.50	4.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1*, *2* and *3*
t_s	Setup Time I_0-I_7	0.90		0.80		0.90		ns	*Figure 4*
t_h	Hold Time I_0-I_7	1.10		1.10		1.10		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay (M, $\overline{OE}$) and Transition Times

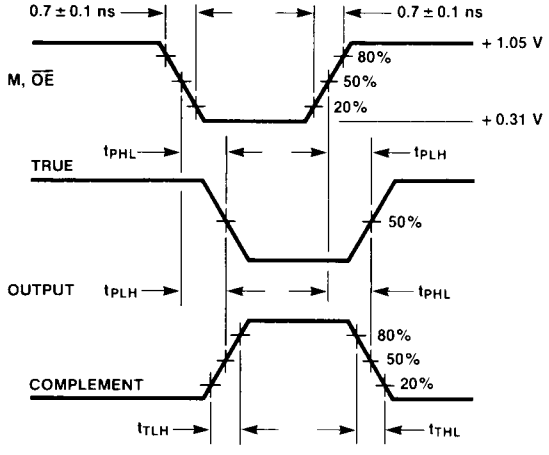


Fig. 3 Enable Timing

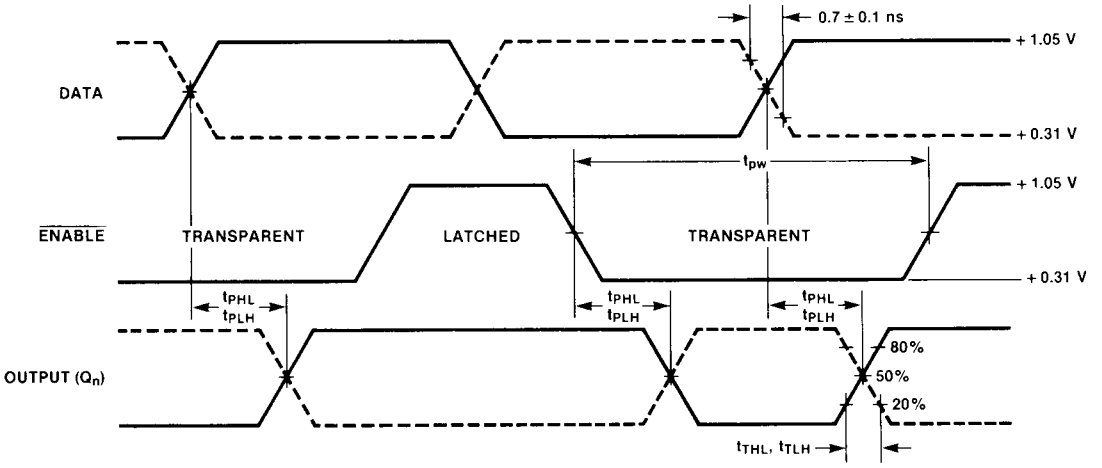
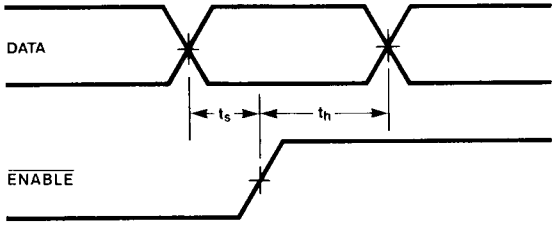


Fig. 4 Setup and Hold Times



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input