a8255

Programmable Peripheral Interface Adapter

September 1996, ver. 1

Features

- a8255 MegaCore function implementing a programmable peripheral interface adapter
- Optimized for FLEX® and MAX® architectures
- 24 programmable inputs/outputs
- Static read/write or handshaking modes
- Direct bit set/reset capability
- Synchronous design
- Uses approximately 194 FLEX logic elements (LEs)
- Functionally based on the Intel 8255A and Harris 82C55A devices, except as noted in the "Variations & Clarifications" section on page 56

General Description

The a8255 MegaCore function implements a programmable peripheral interface adapter (see Figure 1). The a8255 has 24 I/O signals that can be programmed in two groups of 12. This MegaCore function operates in the following three modes:

- *Mode 0: Basic Input/Output*—Port A, port B, and port C (upper and lower) can be independently configured as inputs or outputs to read or hold static data. Outputs are registered; inputs are not registered.
- *Mode 1: Strobed Input/Output*—Port A and port B can be independently configured as strobed input or output buses. Signals from port C are dedicated as control signals for data handshaking.
- *Mode 2: Bidirectional Bus*—Port A can be configured as a bidirectional bus with the majority of port C providing the control signals. In this configuration, port B can still implement mode 0 or mode 1.

Figure 1. a8255 Symbol

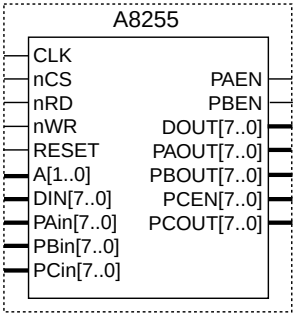


Table 1 describes the input and output ports of the a8255.

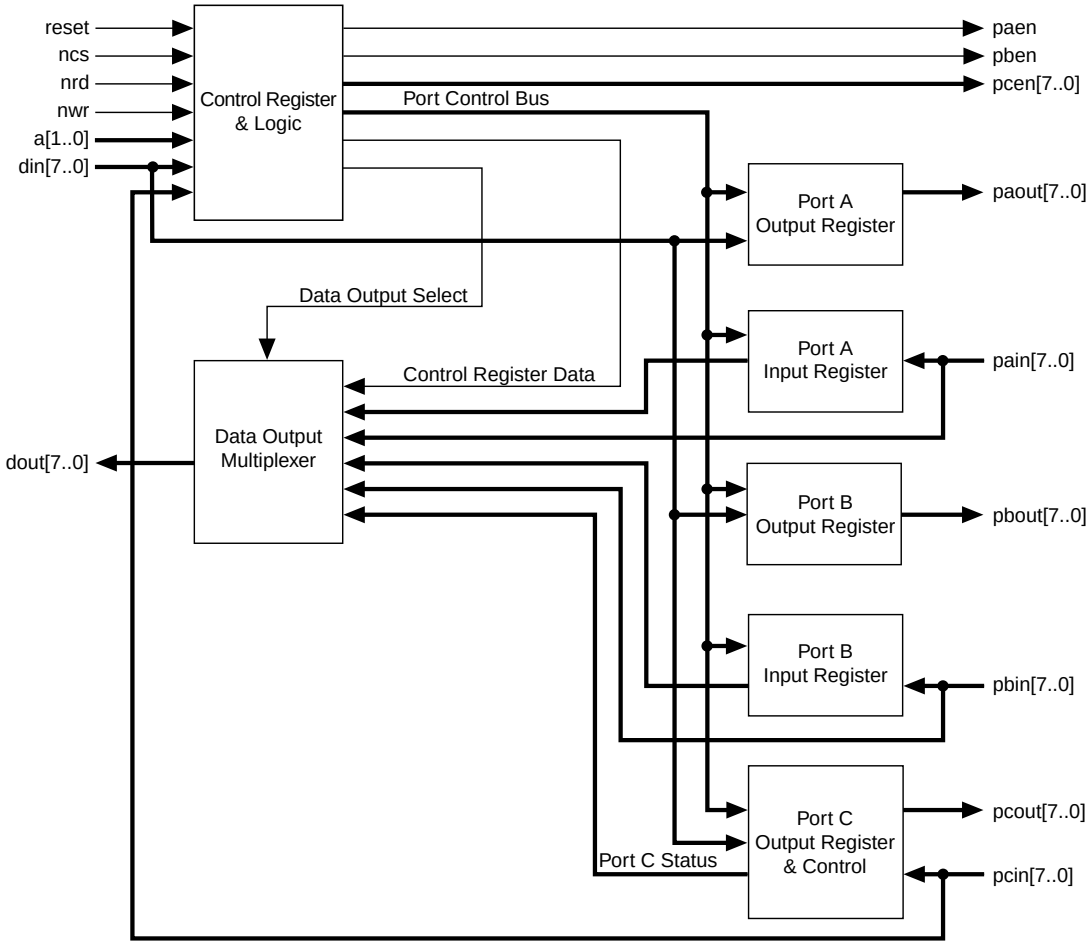
Table 1. a8255 Ports

Name	Type	Polarity	Description
clk	Input	–	Clock.
ncs	Input	Low	Chip select. When ncs is asserted, the a8255 is selected and read and write transactions to internal registers are possible.
nrd	Input	Low	Read control. When nrd is asserted and the a8255 is selected, read transactions from internal registers are possible.
nwr	Input	Low	Write control. When nwr is asserted and the a8255 is selected, write transactions to internal registers are possible.
reset	Input	High	Reset. Initializes the control and port C output registers, and sets the port A, B, and C registers to input mode.
a[1..0]	Input	High	Register address bus. This bus selects one of the internal registers.
din[7..0]	Input	High	Data input bus. The CPU writes data to the internal control, port A, port B, or port C register via the din[7..0] bus.
pain[7..0]	Input	High	Port A input data bus.
pbin[7..0]	Input	High	Port B input data bus.
pcin[7..0]	Input	High	Port C input data bus.
paen	Output	High	Port A data enable. Output enable for the port A output data bus.
pben	Output	High	Port B data enable. Output enable for the port B output data bus.
dout[7..0]	Output	High	Data output bus. The CPU reads data from the internal control, port A, port B, or port C register via the dout[7..0] bus.
paout[7..0]	Output	High	Port A output data bus.
pbout[7..0]	Output	High	Port B output data bus.
pcen[7..0]	Output	High	Port C data enable bus. Output enable for each bit of the port C output data bus.
pcout[7..0]	Output	High	Port C output data bus.

Functional Description

Figure 2 shows a block diagram of the a8255.

Figure 2. a8255 Block Diagram



Register Address Map

Table 2 shows the register address map for the a8255.

Table 2. Register Address Map

a1	a0	Register
0	0	Port A data (all modes)
0	1	Port B data (all modes)
1	0	Port C data (mode 0) and status (modes 1 and 2)
1	1	Control register mode definition and port C bit set/reset

Registers

This section describes the following a8255 registers:

- Control
- Port A, B & C

Control Register

The control register sets the mode and signal direction for the three 8-bit I/O ports. Control of the I/O ports is split into two groups. Group A consists of port A and the upper four bits of port C; group B consists of port B and the lower four bits of port C. Group A can be set to mode 0, mode 1, or mode 2, but group B can be set to only mode 0 or mode 1.

Writing to the control register address with bit 7 set is the mode definition format, which allows control of the mode and direction of the three I/O ports (see Table 3). Writing to the control register address with bit 7 reset is the port C bit set/reset format, which allows single-bit control of port C (see Table 4). The CPU reads the control register using the mode definition format.

Table 3. Control Register Mode Definition Format	
Bit	**Description**
0	Port C (lower) I/O direction: 1 = input 0 = output
1	Port B I/O direction: 1 = input 0 = output
2	Group B mode select: 1 = mode 1 0 = mode 0
3	Port C (upper) I/O direction: 1 = input 0 = output
4	Port A I/O direction: 1 = input 0 = output
6..5	Group A mode select: 00 = mode 0 01 = mode 1 1X = mode 2, *Note (1)*
7	1 when writing = mode definition format Always 1 when reading the control register

Note:
(1) The X indicates "don't care."

Table 4. Port C Bit Set/Reset Format *Note (1)*	
Bit	**Description**
0	Bit set/reset: 1 = set 0 = reset
3..1	Bit select address
6..4	XXX, *Note (2)*
7	0 when writing = port C bit set/reset format

Notes:
(1) For example, to reset bit 3 of port C, bit 7 is reset to indicate that the write is in the port C bit set/reset format. Bits 6 through 4 are "don't care." Bits 3 through 1 are 011 to address bit 3, and bit 0 is 0 to indicate a reset operation. The complete data word is 0XXX0110.
(2) The X indicates "don't care."

Port A, B & C Registers

Depending on the configured input and output directions that are set in the control register, the microprocessor either reads or writes data to/from the port A, B, or C registers. Ports A and B have separate input and output registers.

In mode 0, the port C register functions identically to the port A and B registers. In modes 1 and 2, the port C register has a specialized role; a write to port C has no effect—the register bits must be altered individually using the port C bit set/reset format. Reading the port C status bits in modes 1 or 2 provides the CPU with the status of the control signals and flags, as shown in Tables 5 through 7. However, the modes and port directions can be mixed in more combinations than these tables illustrate.

Table 5. Port C Status Bits with Ports A & B in Mode 1 Input *Note (1)*

Bit	Signal	Description
0	intrb	Port B interrupt request
1	ibfb	Port B input buffer full flag
2	inteb	Port B interrupt enable
3	intra	Port A interrupt request
4	intea	Port A interrupt enable
5	ibfa	Port A input buffer full flag
6	I/O	*Note (2)*
7	I/O	*Note (2)*

Notes:
(1) These bits are defined in Table 9.
(2) Bits 6 and 7 effectively operate in mode 0. The I/O direction is dependent on bit 3 of the control register.

Table 6. Port C Status Bits with Ports A & B in Mode 1 Output *Note (1)*		
Bit	**Signal**	**Description**
0	intrb	Port B interrupt request
1	nobfb	Port B output buffer full flag
2	inteb	Port B interrupt enable
3	intra	Port A interrupt request
4	I/O	*Note (2)*
5	I/O	*Note (2)*
6	intea	Port A interrupt enable
7	nobfa	Port A output buffer full flag

Notes:
(1) These bits are defined in Table 9.
(2) Bits 4 and 5 effectively operate in mode 0. The I/O direction is dependent on bit 3 of the control register.

Table 7. Port C Status Bits with Port A in Mode 2 *Note (1)*		
Bit	**Signal**	**Description**
0	–	*Note (2)*
1	–	*Note (2)*
2	–	*Note (2)*
3	intra	Port A interrupt request
4	inte2	Interrupt enable 2
5	ibfa	Port A input buffer full flag
6	inte1	Interrupt enable 1
7	nobfa	Port A output buffer full flag

Notes:
(1) These bits are defined in Table 11.
(2) Depending on the lower three bits of the control register, bits 0 through 2 either operate in mode 0 or function as status bits for port B in mode 1.

Operation

The a8255 operates in the following three modes:

- Mode 0: basic input/output
- Mode 1: strobed input/output
- Mode 2: strobed bidirectional bus

Mode 0: Basic Input/Output

Mode 0 is used to perform simple reads or writes of relatively static signals, such as switches or status displays. Port A, port B, port C (upper), and port C (lower) can be independently configured as inputs or outputs without requiring handshake signals. Data written by the CPU to a port configured as an output is registered; data read by the CPU from a port configured as an input is not registered.

Mode 1: Strobed Input/Output

Mode 1 is used to perform reads or writes of data controlled by handshake signals. Ports A and B are the data ports, configured independently as either inputs or outputs. Port C provides the three handshaking signals for each of the data ports. Both input and output data are registered.

Table 8 shows how the handshaking signals are configured for mode 1 input.

Table 8. Handshaking Signal Configuration (Mode 1 Input)

Name	Signal Type	Description
nstb	Input	Strobe. Enable for input register.
ibf	Output	Input buffer full flag. When set, indicates that data has been loaded into the input register. Set by nstb going low, and reset by the rising edge of the nrd input.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU. Set on the rising edge of nstb when inte is high. Reset by the falling edge of nrd.
inte	Internal control bit	Interrupt enable. Set by bit set to PC4 for port A and PC2 for port B.

Table 9 shows how the handshaking signals are configured for mode 1 output.

Table 9. Handshaking Signal Configuration (Mode 1 Output)

Name	Signal Type	Description
nobf	Output	Output buffer full flag. Indicates that data has been written to the port. Goes low on the rising edge of nwr, and returns high when nack is asserted. The rising edge of nobf should be used to latch data into the peripheral.
nack	Input	Acknowledge. Indicates the peripheral is ready to latch the output data.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU, which indicates that the peripheral device has latched the data. Reset on the falling edge of nwr; set on the rising edge of nack when inte is high.
inte	Internal control bit	Interrupt enable. Set by bit set to PC6 for port A and PC2 for port B.

Table 10 summarizes the configuration of port C when both port A and port B are configured as mode 1.

Table 10. Port C with Port A & Port B Both Configured as Mode 1 *Note (1)*

Bit	Mode 1 Input	Mode 1 Output	Description
PC0	intrb	intrb	Always output.
PC1	ibfb	nobfb	Always output.
PC2	nstbb	nackb	Always input.
PC3	intra	intra	Always output.
PC4	nstba	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC5	ibfa	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC6	I/O	nacka	I/O direction configured by bit 3 of the control register in “mode 1 input.”
PC7	I/O	nobfa	I/O direction configured by bit 3 of the control register in “mode 1 input.”

Note:
(1) The interrupt enable control bits (intea and inteb) are stored in the output register bits PC2, PC4, and PC6.

Mode 2: Strobed Bidirectional Bus

Mode 2 is used to perform reads and writes of data over a bidirectional bus controlled by handshake signals. Port A is the only data port capable of mode 2 operation, while port C provides the five control signals for this data port. Both input and output data are registered. Table 11 shows the configuration for the bidirectional bus.

Table 11. Bidirectional Bus Configuration

Name	Signal Type	Description
nstb	Input	Strobe. Enable for input register.
nack	Input	Acknowledge. Indicates that the peripheral is ready to latch the output data. Acts as the tri-state enable for port A.
ibf	Output	Input buffer full flag. When set, indicates data has been loaded into the input register. Set by nstb going low, and reset by the rising edge of the nrd input.
nobf	Output	Output buffer full flag. Indicates that data has been written to port A. Reset on the rising edge of nwr, and set when nack goes low.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU that indicates the peripheral has latched the data. Reset on the falling edge of nwr or falling edge of nrd. Set on the rising edge of nack when inte1 is high, or on the rising edge of nstb when inte2 is high.
inte1	Internal control bit	Interrupt enable 1. Set by bit set to PC6.
inte2	Internal control bit	Interrupt enable 2. Set by bit set to PC4.

Table 12 summarizes the configuration of port C in mode 2.

Table 12. Port C Configuration in Mode 2

I/O	Mode 2	Description
PC0	I/O	Dependent on group B configuration
PC1	I/O	Dependent on group B configuration
PC2	I/O	Dependent on group B configuration
PC3	intra	Output
PC4	nstba	Input
PC5	ibfa	Output
PC6	nacka	Input
PC7	nobfa	Output

Timing Waveforms

Figures 3 and 4 shows the functional timing waveforms for the a8255.

Figure 3. a8255 Mode 0 and Mode 1 Functional Timing Waveforms

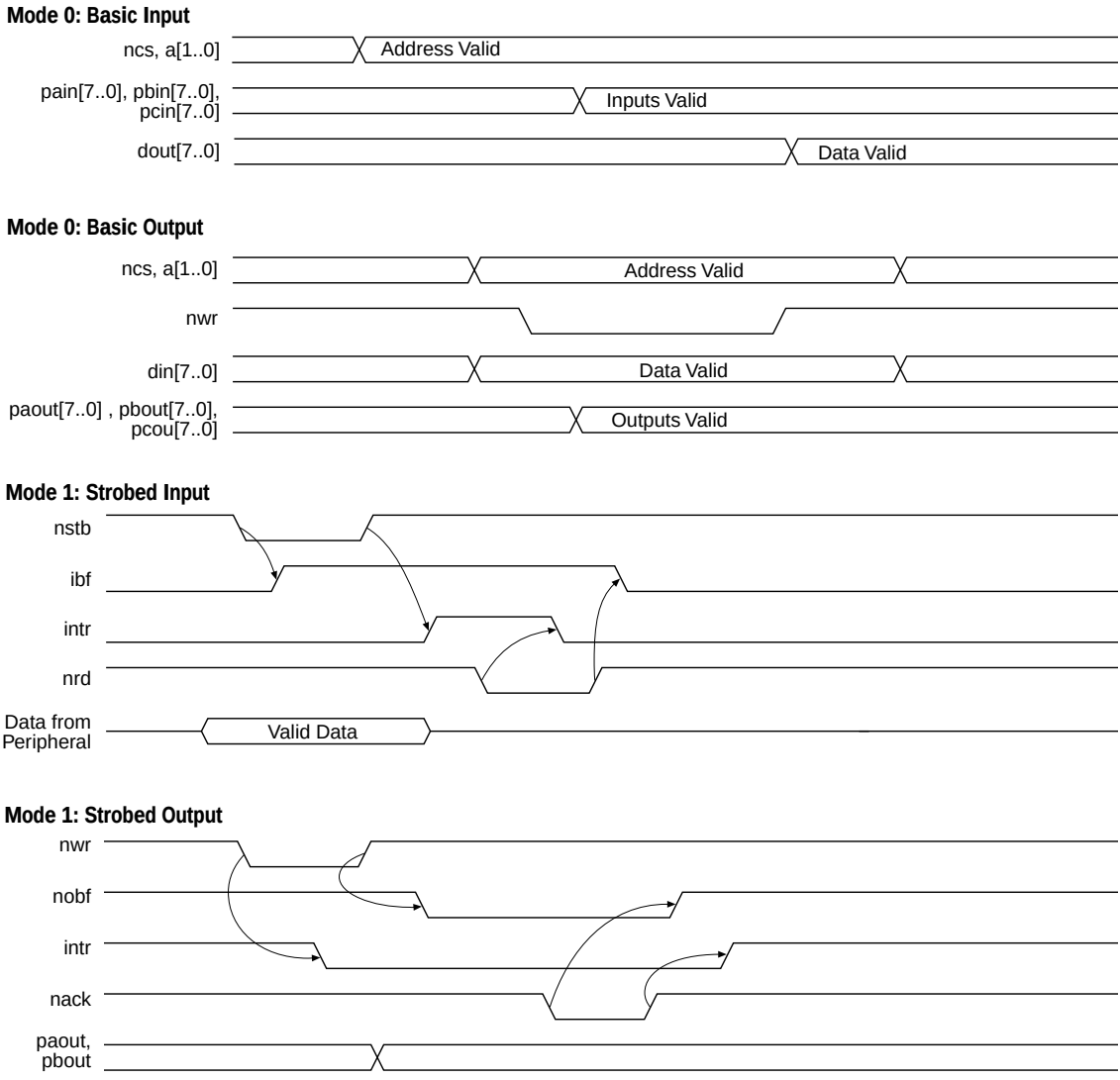
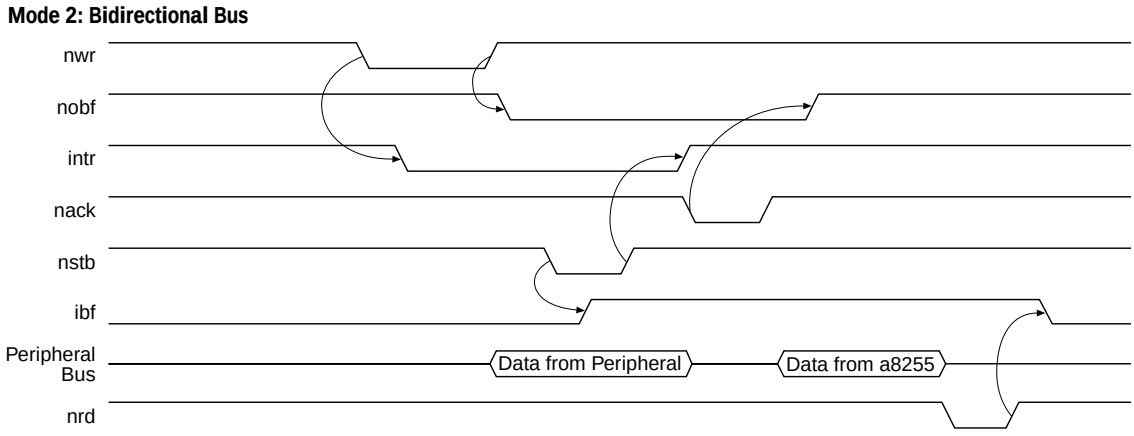


Figure 4. a8255 Mode 2 Functional Timing Waveforms



Variations & Clarifications

The following characteristics distinguish the Altera a8255 from the Intel 8255A and Harris 82C55A devices:

- To allow synchronous design, a clk input was added as a system clock to the a8255. This capability requires that all strobes (nrd, nwr, nstb, and nack) have a minimum pulse width of one clk cycle.
- In the a8255, the reset input resets the port A, B, and C registers. In the Intel 8255A and Harris 82C55A devices, the port A, B, and C registers are unaffected by the reset input.
- The bidirectional buses in the Intel 8255A and Harris 82C55A devices (d, pa, pb, and pc) are split into input, output, and enable signals in the Altera a8255.
- The a8255 has no "bus hold" passive pull-ups on port signals. Because the port I/O signal is usually tied to the I/O of the Altera device, pull-ups or pull-downs can be added.
- In the a8255, the control register can be read. The control register can be read on the Harris 82C55A device, but the Intel 8255A device does not have this capability.
- In the a8255, the reset signal initializes the control register such that all ports are set to mode 0 inputs. Reading the control register after initialization will return the value of 9B in hexadecimal.
- After initialization in mode 1, the pertinent control signals in the port C register should be configured via the port C bit set/reset commands.
- In mode 2, every read or write of port A resets the intra interrupt signal.
- The Intel and Harris data sheets state that output registers and status flipflops should be reset in the event of a mode change. This feature was not included in the a8255.