



P-Channel 60-V (D-S) 175°C MOSFET

CHARACTERISTICS

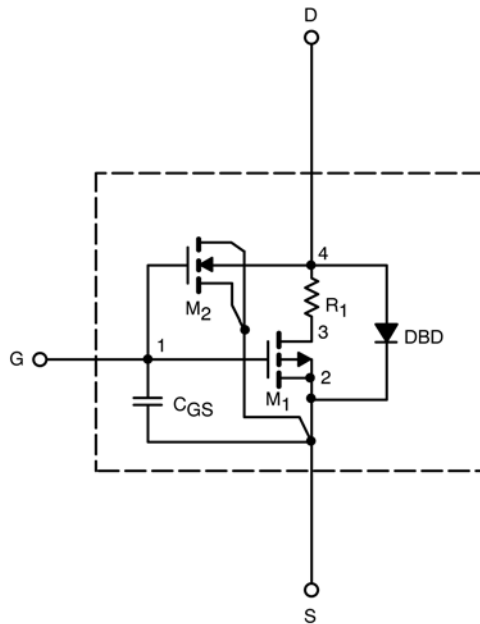
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model SUD19P06-60L

Vishay Siliconix



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	2		V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	104		A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	0.047	0.047	Ω
		$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}, T_J = 125^\circ\text{C}$	0.083		
		$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}, T_J = 175^\circ\text{C}$	0.102		
		$V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$	0.060	0.061	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -10 \text{ A}$	20	22	S
Diode Forward Voltage ^a	V_{SD}	$I_S = -10 \text{ A}, V_{GS} = 0 \text{ V}$	-0.87	-1	V
Dynamic ^b					
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$	1430	1140	pF
Output Capacitance	C_{oss}		130	130	
Reverse Transfer Capacitance	C_{rss}		84	90	
Total Gate Charge ^c	Q_g	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	25	26	nC
Gate-Source Charge ^c	Q_{gs}		4.5	4.5	
Gate-Drain Charge ^c	Q_{gd}		7	7	

Notes

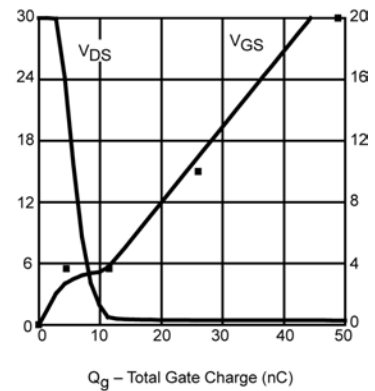
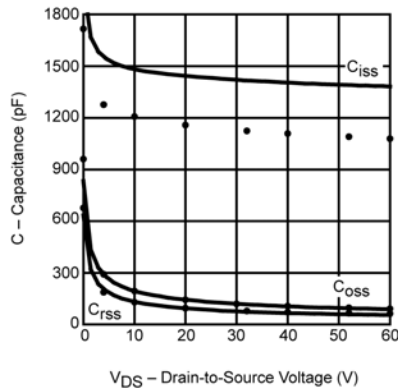
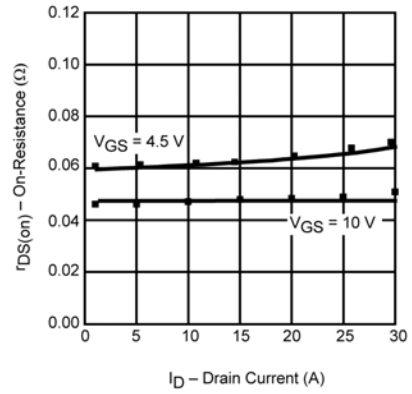
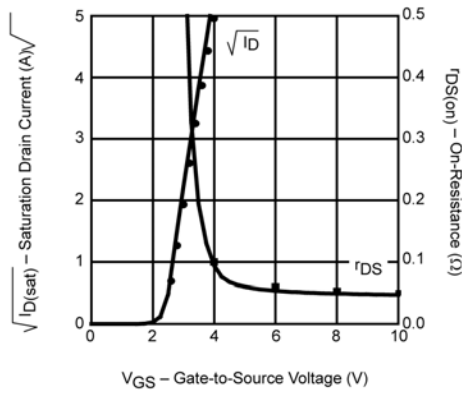
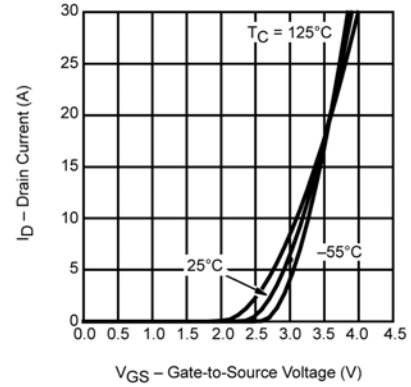
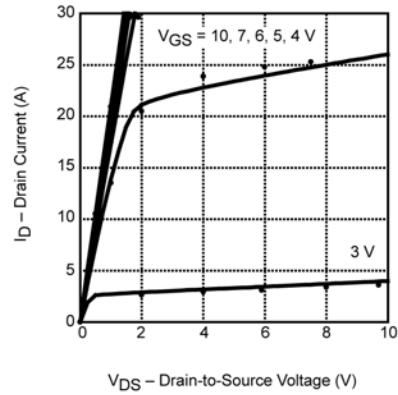
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.