

Low Charge Injection 8-Channel High Voltage Analog Switches with Bleed Resistors

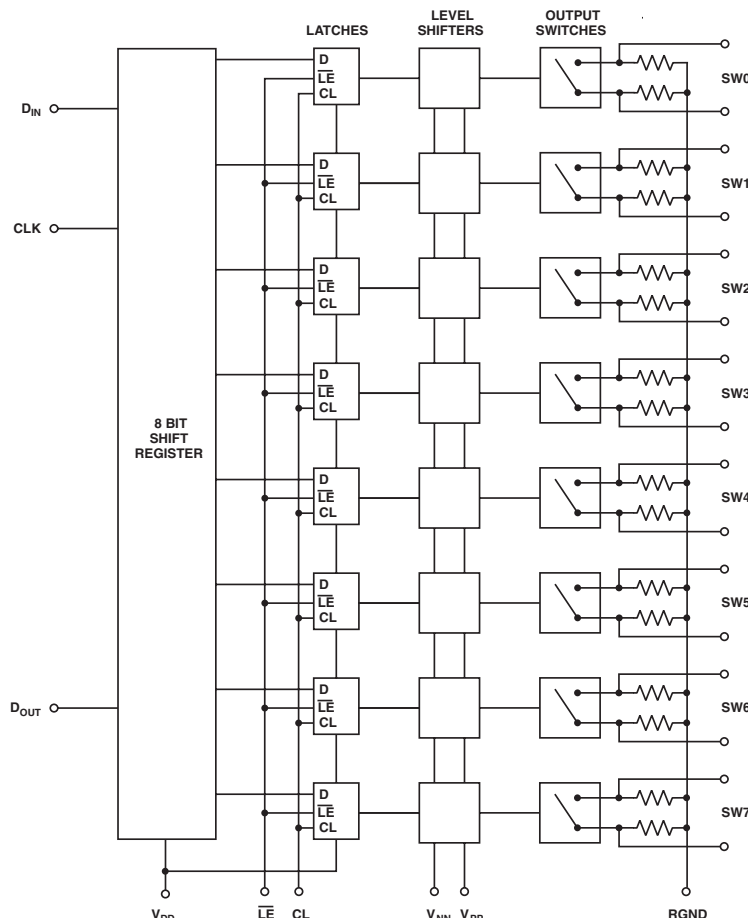
Features

- ❑ HVCMOS® technology for high performance
- ❑ Very low quiescent power dissipation – 10µA
- ❑ Output On-resistance typically 22 ohms
- ❑ Integrated bleed resistors on the outputs
- ❑ Low parasitic capacitances
- ❑ DC to 10MHz analog signal frequency
- ❑ -60dB typical output off isolation at 5MHz
- ❑ CMOS logic circuitry for low power
- ❑ Excellent noise immunity
- ❑ On-chip shift register, latch and clear logic circuitry
- ❑ Flexible high voltage supplies

Applications

- ❑ Medical ultrasound imaging
- ❑ Piezoelectric transducer drivers

Block Diagram



General Description

The Supertex HV230 and HV232 are low charge injection 8-channel high-voltage analog switch integrated circuits (ICs) with bleed resistors. These devices can be used in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar (\overline{LE}) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

These ICs are suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/-150V, or +100V/-100V.

Absolute Maximum Ratings*

| | |
|---------------------------------------|--------------------------|
| V_{DD} Logic power supply voltage | -0.5V to +15V |
| $V_{PP} - V_{NN}$ Supply voltage | 220V |
| V_{PP} Positive high voltage supply | -0.5V to $V_{NN} + 200V$ |
| V_{NN} Negative high voltage supply | +0.5V to -200V |
| Logic input voltages | -0.5V to $V_{DD} + 0.3V$ |
| Analog Signal Range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 3.0A |
| Storage temperature | -65°C to +150°C |
| Power dissipation: | |
| 28-lead PLCC | 1.2W |
| 48-lead TQFP | 1.0W |
| 26-lead TAPP | 1.0W |
| 26-lead μ -BGA | 1.0W |

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Operating Conditions*

| Symbol | Parameter | Value |
|-----------|--|---|
| V_{DD} | Logic power supply voltage ^{1, 3} | 4.5V to 13.2V |
| V_{PP} | Positive high voltage supply ^{1, 3} | 40V to $V_{NN} + 200V$ |
| V_{NN} | Negative high voltage supply ^{1, 3} | -40V to -160V |
| V_{IH} | High-level input voltage | $V_{DD} - 1.5V$ to V_{DD} |
| V_{IL} | Low-level input voltage | 0V to 1.5V |
| V_{SIG} | Analog signal voltage peak to peak | $V_{NN} + 10V$ to $V_{PP} - 10V$ ² |
| T_A | Operating free air-temperature | 0°C to 70°C |

Notes:

- 1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- 2 V_{SIG} must be $V_{NN} - V_{SIG} - V_{PP}$ or floating during power up/down transition.
- 3 Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.

Ordering Information

| Package Options | | | | | $V_{PP} - V_{NN}$ |
|------------------------------|--------------|--------------|--------------------|--------|-------------------|
| 28-Lead plastic chip carrier | 48-Lead TQFP | 26-lead TAPP | 26-lead μ -BGA | Die | |
| HV232PJ | HV232FG | - | HV232GA | HV232X | 200V |
| - | - | HV230TA | - | - | 200V |

Truth Table

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | \overline{LE} | CL | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
|----|----|----|----|----|----|----|----|-----------------|----|-----|---------------------|-----|-----|-----|-----|-----|-----|
| L | | | | | | | | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | | | | | | ON | | |
| | | | | | | L | | L | L | | | | | | | OFF | |
| | | | | | | H | | L | L | | | | | | | ON | |
| X | X | X | X | X | X | X | X | X | H | L | HOLD PREVIOUS STATE | | | | | | |
| X | X | X | X | X | X | X | X | X | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flows through the latch.
4. D_{OUT} is high when data in shift register 7 is high.
5. Shift register clocking has no effect on the switch states if \overline{LE} is H.
6. The clear input overrides all other inputs.

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)

| Characteristics | Sym | 0°C | | +25°C | | | +70°C | | Units | Test Conditions | |
|--|-------------------|------|-----|-------|------|-----|-------|-----|-------|---|--|
| | | min | max | min | typ* | max | min | max | | | |
| Small Signal Switch (ON) Resistance | R _{ONS} | | 30 | | 26 | 38 | | 48 | Ω | I _{SIG} = 5mA | V _{PP} = 40V, V _{NN} = -160V |
| | | | 25 | | 22 | 27 | | 32 | | I _{SIG} = 200mA | V _{NN} = -100V |
| | | | 25 | | 22 | 27 | | 30 | | I _{SIG} = 5mA | V _{PP} = 100V, V _{NN} = -100V |
| | | | 18 | | 18 | 24 | | 27 | | I _{SIG} = 200mA | V _{NN} = -100V |
| | | | 23 | | 20 | 25 | | 30 | | I _{SIG} = 5mA | V _{PP} = 160V, V _{NN} = -40V |
| | | | 22 | | 16 | 25 | | 27 | | I _{SIG} = 200mA | V _{NN} = -40V |
| Small Signal Switch (ON) Resistance Matching | ΔR _{ONS} | | 20 | | 5.0 | 20 | | 20 | % | I _{SW} = 5mA, V _{PP} = 100V, V _{NN} = -100V | |
| Large Signal Switch (ON) Resistance | R _{ONL} | | | | 15 | | | | Ω | V _{SIG} = V _{PP} - 10V, I _{SIG} = 1A | |
| Output Switch Shunt Resistance | R _{INT} | | | 20 | 35 | 50 | | | KΩ | Output switch to R _{GND} I _{RINT} = 0.5mA | |
| Switch Off Leakage Per Switch | I _{SOL} | | 5.0 | | 1.0 | 10 | | 15 | μA | V _{SIG} = V _{PP} - 10V | |
| DC Offset Switch Off | | | 300 | | 100 | 300 | | 300 | mV | No Load | |
| DC Offset Switch On | | | 500 | | 100 | 500 | | 500 | mV | No Load | |
| Pos. HV Supply Current | I _{PPQ} | | | | 10 | 50 | | | μA | ALL SWs OFF | |
| Neg. HV Supply Current | I _{NNQ} | | | | -10 | -50 | | | μA | ALL SWs OFF | |
| Pos. HV Supply Current | I _{PPQ} | | | | 10 | 50 | | | μA | ALL SWs ON, I _{SW} = 5mA | |
| Neg. HV Supply Current | I _{NNQ} | | | | -10 | -50 | | | μA | ALL SWs ON, I _{SW} = 5mA | |
| Switch Output Peak Current | | | 3.0 | | 3.0 | 2.0 | | 2.0 | A | V _{SIG} duty cycle - 0.1% | |
| Output Switch Frequency | f _{SW} | | | | | 50 | | | KHz | Duty Cycle = 50% | |
| I _{PP} Supply Current | I _{PP} | | 6.5 | | | 7.0 | | 8.0 | mA | V _{PP} = 40V, V _{NN} = -160V | 50KHz Output Switching Frequency with no load |
| | | | 4.0 | | | 5.0 | | 5.5 | | V _{PP} = 100V, V _{NN} = -100V | |
| | | | 4.0 | | | 5.0 | | 5.5 | | V _{PP} = 160V, V _{NN} = -40V | |
| I _{NN} Supply Current | I _{NN} | | 6.5 | | | 7.0 | | 8.0 | mA | V _{PP} = 40V, V _{NN} = -160V | |
| | | | 4.0 | | | 5.0 | | 5.5 | | V _{PP} = 100V, V _{NN} = -100V | |
| | | | 4.0 | | | 5.0 | | 5.5 | | V _{PP} = 160V, V _{NN} = -40V | |
| Logic Supply Average Current | I _{DD} | | 4.0 | | | 4.0 | | 4.0 | mA | f _{CLK} = 5MHz, V _{DD} = 5.0V | |
| Logic Supply Quiescent Current | I _{DDQ} | | 10 | | | 10 | | 10 | μA | | |
| Data Out Source Current | I _{SOR} | 0.45 | | 0.45 | 0.70 | | 0.40 | | mA | V _{OUT} = V _{DD} - 0.7V | |
| Data Out Sink Current | I _{SINK} | 0.45 | | 0.45 | 0.70 | | 0.40 | | mA | V _{OUT} = 0.7V | |
| Logic Input Capacitance | C _{IN} | | 10 | | | 10 | | 10 | pF | | |

*Typical values only for HV232

Electrical Characteristics

AC Characteristics (over operating conditions $V_{DD} = 5V$, unless otherwise noted)

| Characteristics | Sym | 0°C | | +25°C | | | +70°C | | Units | Test Conditions |
|--|---------------|-----|-----|-------|------|-----|-------|-----|---------|---|
| | | min | max | min | typ* | max | min | max | | |
| Set Up Time Before \overline{LE} Rises | t_{SD} | 150 | | 150 | | | 150 | | ns | |
| Time Width of \overline{LE} | t_{WLE} | 150 | | 150 | | | 150 | | ns | |
| Clock Delay Time to Data Out | t_{DO} | 55 | 150 | 60 | | 150 | 70 | 150 | ns | |
| Time Width of CL | t_{WCL} | 150 | | 150 | | | 150 | | ns | |
| Set Up Time Data to Clock | t_{SU} | 15 | | 15 | 8.0 | | 20 | | ns | |
| Hold Time Data from Clock | t_h | 35 | | 35 | | | 35 | | ns | |
| Clock Freq | f_{CLK} | | 5.0 | | | 5.0 | | 5.0 | MHz | 50% duty cycle $f_{DATA} = f_{CLK}/2$ |
| Clock Rise and Fall Times | t_r, t_f | | 1.0 | | | 1.0 | | 1.0 | μs | |
| Turn On Time | t_{ON} | | 5.0 | | | 5.0 | | 5.0 | μs | $V_{SIG} = V_{PP} - 10V$, $R_L = 10K\Omega$ |
| Turn Off Time | t_{OFF} | | 5.0 | | | 5.0 | | 5.0 | μs | $V_{SIG} = V_{PP} - 10V$, $R_L = 10K\Omega$ |
| Maximum V_{SIG} Slew Rate | dv/dt | | 20 | | | 20 | | 20 | V/ns | $V_{PP} = 160V$, $V_{NN} = -40V$ |
| | | | 20 | | | 20 | | 20 | | $V_{PP} = 100V$, $V_{NN} = -100V$ |
| | | | 20 | | | 20 | | 20 | | $V_{PP} = 40V$, $V_{NN} = -160V$ |
| Off Isolation | KO | -30 | | -30 | -33 | | -30 | | dB | f = 5MHz, 1K Ω /15pF load |
| | | -58 | | -58 | | | -58 | | | f = 5MHz, 50 Ω load |
| Switch Crosstalk | K_{CR} | -60 | | -60 | -70 | | -60 | | dB | f = 5MHz, 50 Ω load |
| Output Switch Isolation Diode Current | I_{ID} | | 300 | | | 300 | | 300 | | mA |
| Off Capacitance SW to GND | $C_{SG(OFF)}$ | 5.0 | 17 | 5.0 | 12 | 17 | 5.0 | 17 | pF | 0V, 1MHz |
| On Capacitance SW to GND | $C_{SG(ON)}$ | 25 | 50 | 25 | 38 | 50 | 25 | 50 | pF | 0V, 1MHz |

*Typical values only for HV232

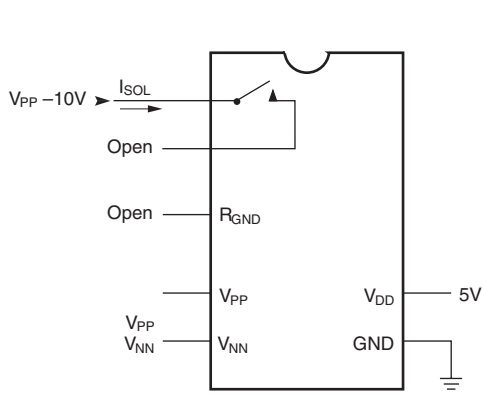
Electrical Characteristics

AC Characteristics (over operating conditions $V_{DD} = 5V$, unless otherwise noted)

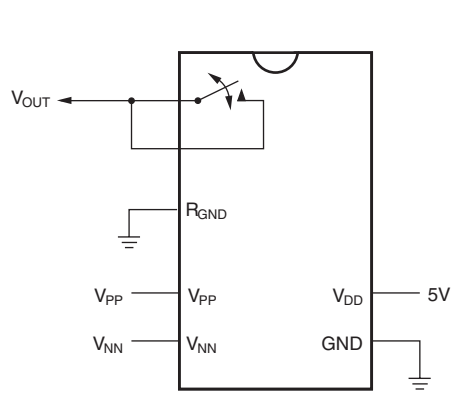
| Characteristics | Sym | +25°C | | | Units | Test Conditions |
|----------------------|------------|-------|------|-----|-------|---|
| | | min | typ* | max | | |
| Output Voltage Spike | $+V_{SPK}$ | | | 150 | mV | $V_{PP} = 40V, V_{NN} = -160V, R_L = 50\Omega$ |
| | $-V_{SPK}$ | | | 150 | | |
| | $+V_{SPK}$ | | | 150 | | $V_{PP} = 100V, V_{NN} = -100V, R_L = 50\Omega$ |
| | $-V_{SPK}$ | | | 150 | | |
| | $+V_{SPK}$ | | | 150 | | $V_{PP} = 160V, V_{NN} = -40V, R_L = 50\Omega$ |
| | $-V_{SPK}$ | | | 150 | | |

*Typical values only for HV232

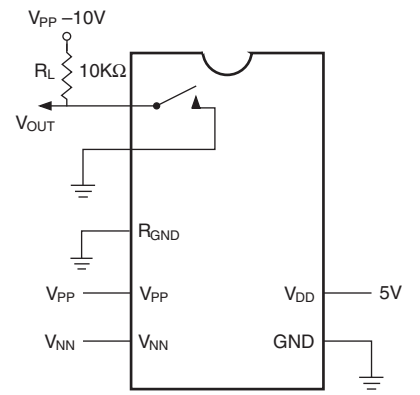
Test Circuits



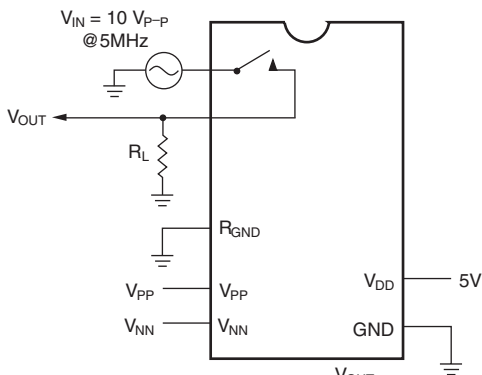
Switch OFF Leakage



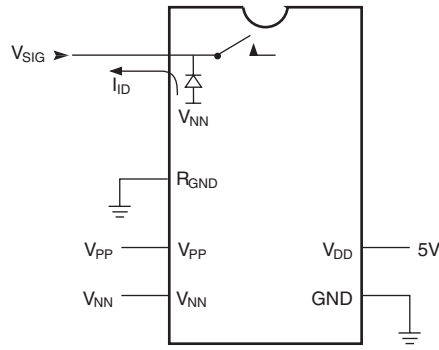
DC Offset ON/OFF



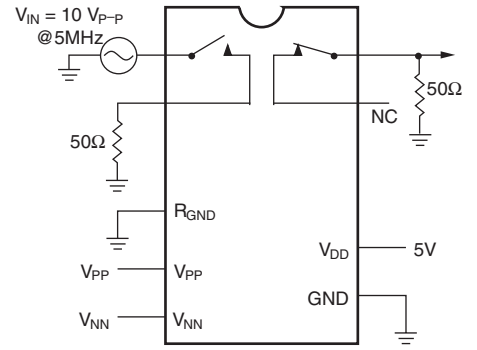
T_{ON}/T_{OFF} Test Circuit



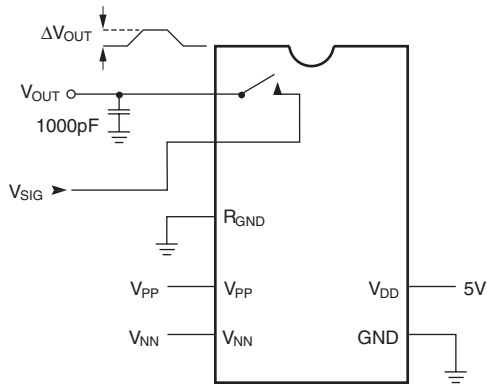
$K_O = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$
OFF Isolation



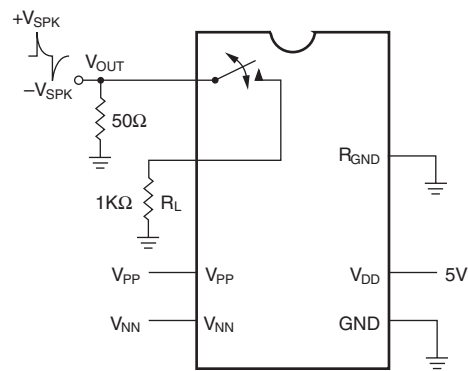
Isolation Diode Current



$K_{CR} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$
Crosstalk

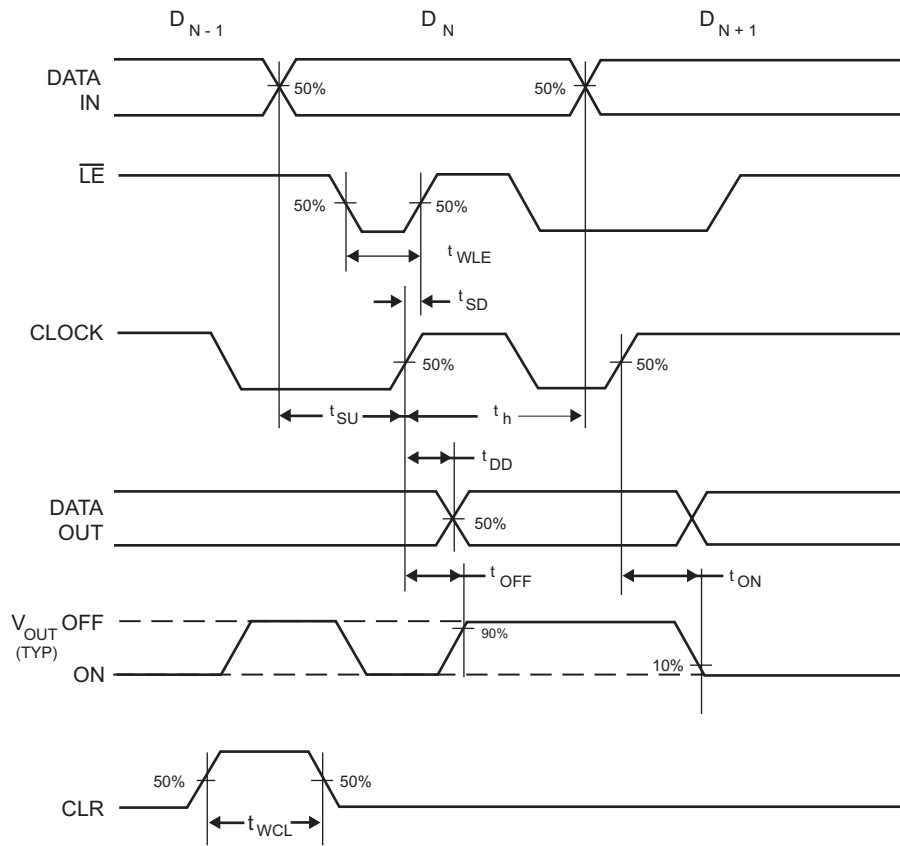


$Q = 1000 \text{pF} \times \Delta V_{OUT}$
Charge Injection

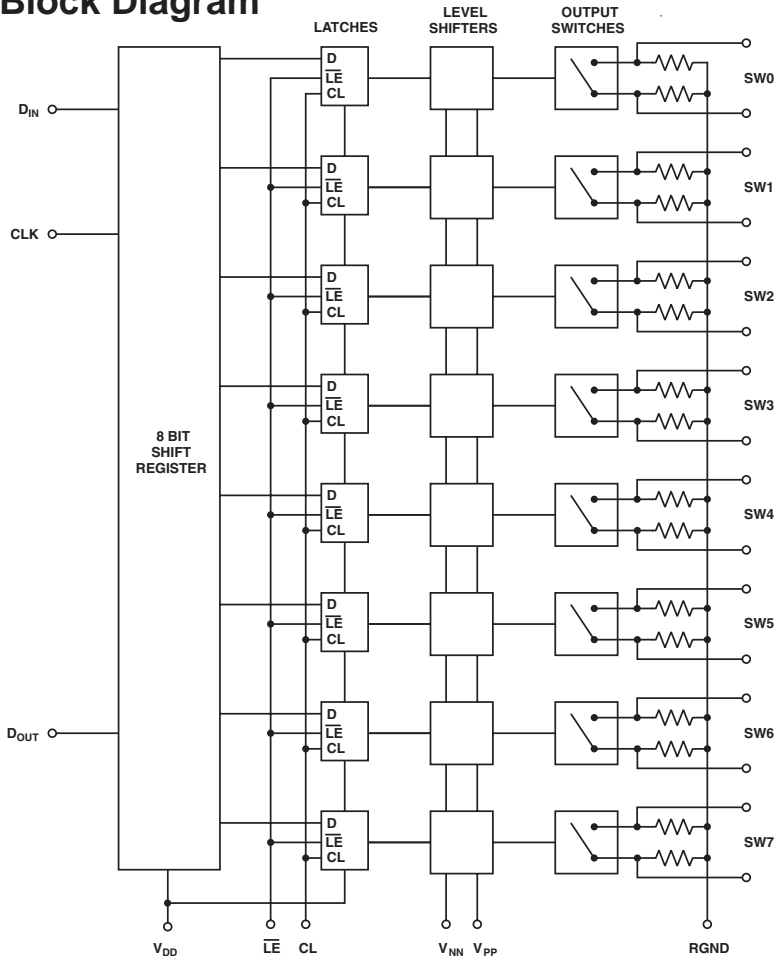


Output Voltage Spike

Logic Timing Waveforms



Block Diagram

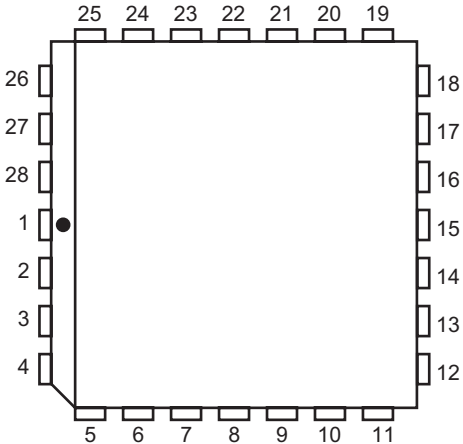


Pin Configurations

Package Outlines

HV232 28-Pin J-Lead

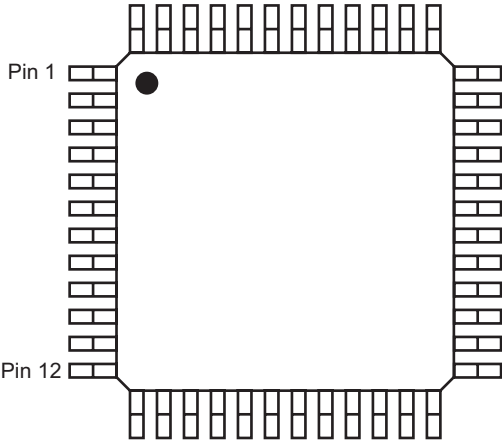
| Pin | Function | Pin | Function |
|-----|------------------|-----|------------------|
| 1 | SW3 | 15 | N/C |
| 2 | SW3 | 16 | D _{IN} |
| 3 | SW2 | 17 | CLK |
| 4 | SW2 | 18 | LE |
| 5 | SW1 | 19 | CL |
| 6 | SW1 | 20 | D _{OUT} |
| 7 | SW0 | 21 | SW7 |
| 8 | SW0 | 22 | SW7 |
| 9 | N/C | 23 | SW6 |
| 10 | V _{PP} | 24 | SW6 |
| 11 | R _{GND} | 25 | SW5 |
| 12 | V _{NN} | 26 | SW5 |
| 13 | GND | 27 | SW4 |
| 14 | V _{DD} | 28 | SW4 |



Top View
28-Pin J-Lead Package

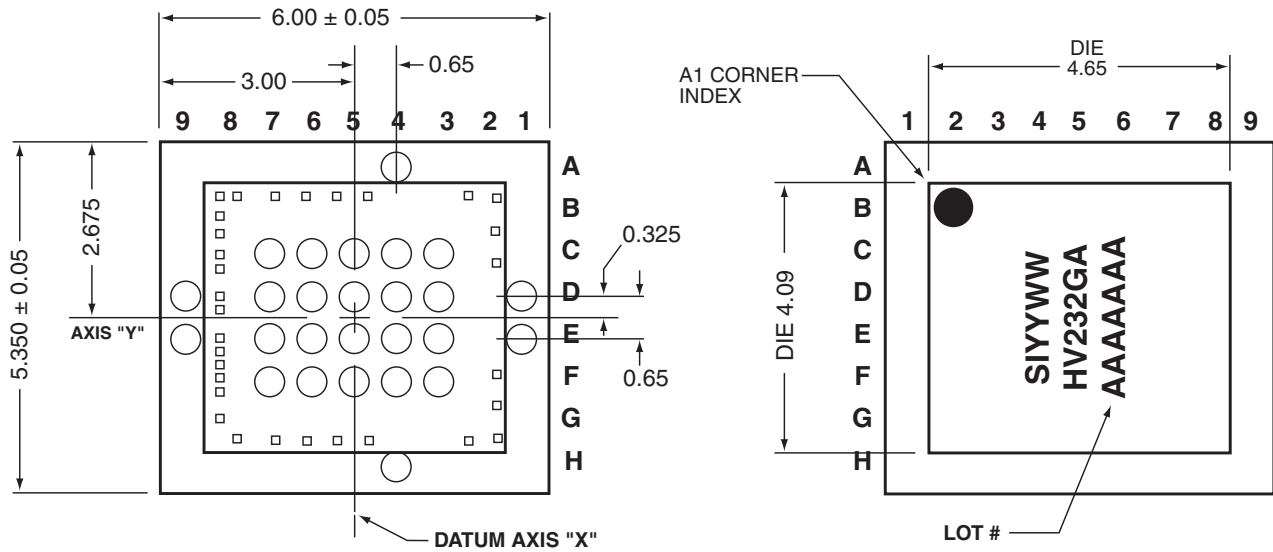
HV232 48-Pin TQFP

| Pin | Function | Pin | Function |
|-----|-----------------|-----|------------------|
| 1 | SW5 | 25 | V _{NN} |
| 2 | N/C | 26 | N/C |
| 3 | SW4 | 27 | R _{GND} |
| 4 | N/C | 28 | GND |
| 5 | SW4 | 29 | V _{DD} |
| 6 | N/C | 30 | N/C |
| 7 | N/C | 31 | N/C |
| 8 | SW3 | 32 | N/C |
| 9 | N/C | 33 | D _{IN} |
| 10 | SW3 | 34 | CLK |
| 11 | N/C | 35 | LE |
| 12 | SW2 | 36 | CLR |
| 13 | N/C | 37 | D _{OUT} |
| 14 | SW2 | 38 | N/C |
| 15 | N/C | 39 | SW7 |
| 16 | SW1 | 40 | N/C |
| 17 | N/C | 41 | SW7 |
| 18 | SW1 | 42 | N/C |
| 19 | N/C | 43 | SW6 |
| 20 | SW0 | 44 | N/C |
| 21 | N/C | 45 | SW6 |
| 22 | SW0 | 46 | N/C |
| 23 | N/C | 47 | SW5 |
| 24 | V _{PP} | 48 | N/C |



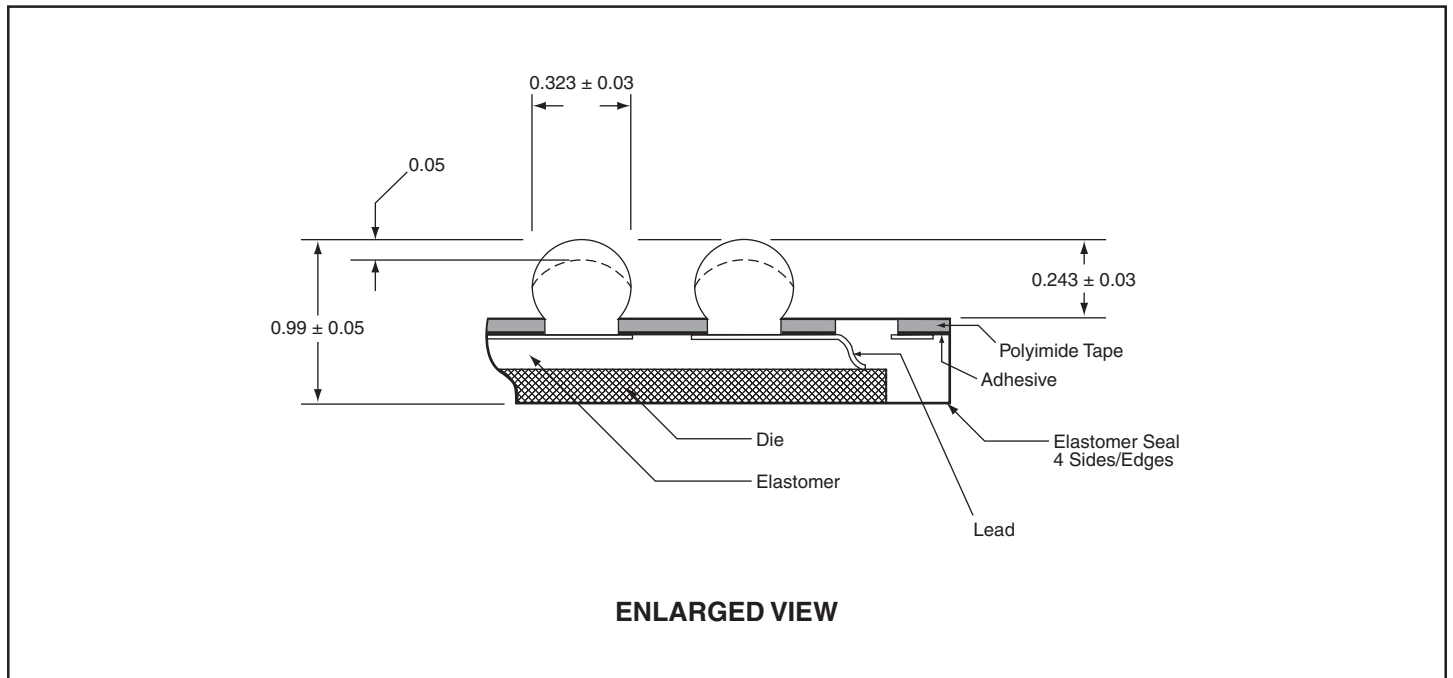
Top View
48-Pin TQFP

HV232GA Package Outline (μ-BGA)



Notes:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Do not subject part to ultrasonic cleaning or intense UV.
3. Contact ball position per JESD 95-1, SPP-010.
4. Units are in millimeters.



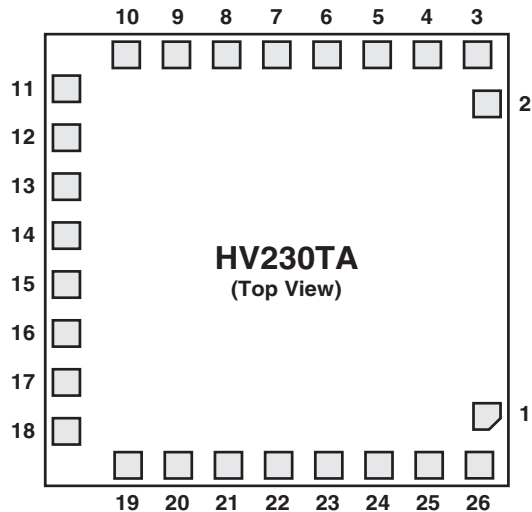
μ-BGA Function Table

| Ball Location | Function |
|----------------------|------------------------|
| A4 | SW1 |
| C3 | SW2 |
| C4 | SW1 |
| C5 | SW0 |
| C6 | V _{PP} |
| C7 | V _{NN} |
| D1 | SW3 |
| D3 | SW3 |
| D4 | SW2 |
| D5 | SW0 |
| D6 | R _{GND} |
| D7 | GND |
| D9 | V _{DD} |
| E1 | SW4 |
| E3 | SW4 |
| E4 | SW5 |
| E5 | SW7 |
| E6 | $\overline{\text{LE}}$ |
| E7 | CLK |
| E9 | D _{IN} |
| F3 | SW5 |
| F4 | SW6 |
| F5 | SW7 |
| F6 | D _{OUT} |
| F7 | CLR |
| H4 | SW6 |

Pin Configuration

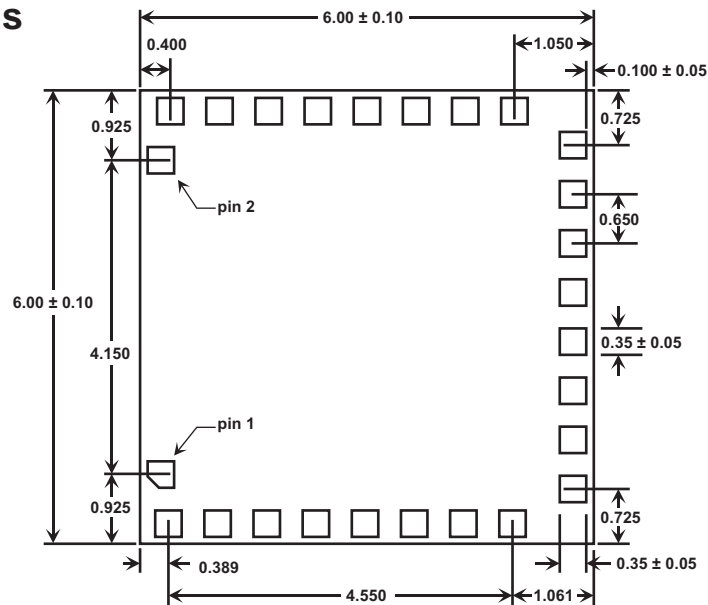
| Pin # | Function | Pin # | Function |
|-------|------------------|-------|------------------|
| 1 | SW4 | 14 | V _{DD} |
| 2 | SW3 | 15 | D _{IN} |
| 3 | SW3 | 16 | CLK |
| 4 | SW2 | 17 | LE bar |
| 5 | SW2 | 18 | CLR |
| 6 | SW1 | 19 | D _{OUT} |
| 7 | SW1 | 20 | SW7 |
| 8 | SW0 | 21 | SW7 |
| 9 | SW0 | 22 | SW6 |
| 10 | V _{PP} | 23 | SW6 |
| 11 | V _{NN} | 24 | SW5 |
| 12 | R _{GND} | 25 | SW5 |
| 13 | GND | 26 | SW4 |

Pad Diagram



Pad connections are on the backside of the package

Package Dimensions



Bottom View
Dimensions are in mm



Side View
Dimensions are in mm

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