AGD8136A / AGD8236A

High Voltage 3-Phase Gate Driver IC

General Description

The AGD8136A / AGD8236A are 600V 6-channel gate driver ICs to control IGBTs and power MOS-transistors in 3-phase inverter systems. Due to specially designed common mode filter, it has an excellent ruggedness on transient voltage variation.

SOP-28L

(Body: 18 x 7.5 x 2.5 mm)

Green

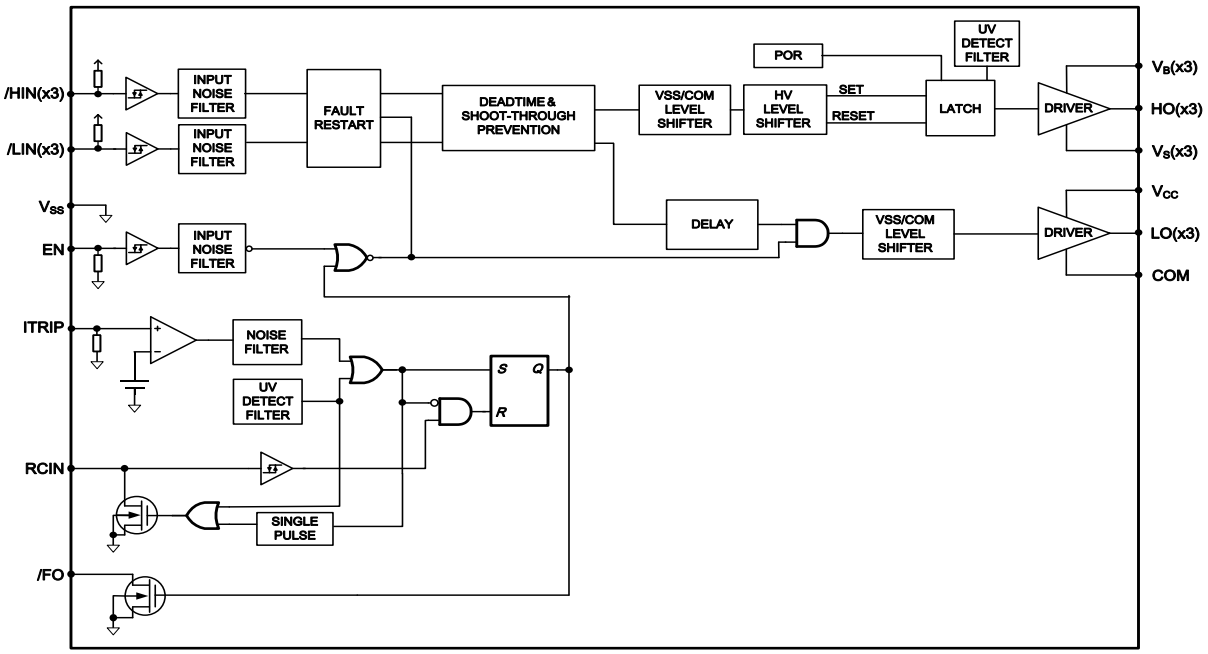
Features

- Maximum blocking voltage +600V
- Output current: +200mA / -350mA (Typ.)
- Matched propagation delay for all channels
- Shoot-through (cross-conduction) protection
- Under-voltage lockout protection (UVLO)
- Over-current protection (OCP)
- Fault output corresponding to UV (Vcc supply) and OCP
- Shut-down of all channels during fault conditions
- Adjustable fault output duration time
- 3.3V / 5V CMOS and TTL input logic compatible
- Input logic: Schmitt trigger receiver circuit (Active Low)

Applications

- 3-phase motor drives
- Home appliances
- IGBT and power MOS gate drivers for general purpose

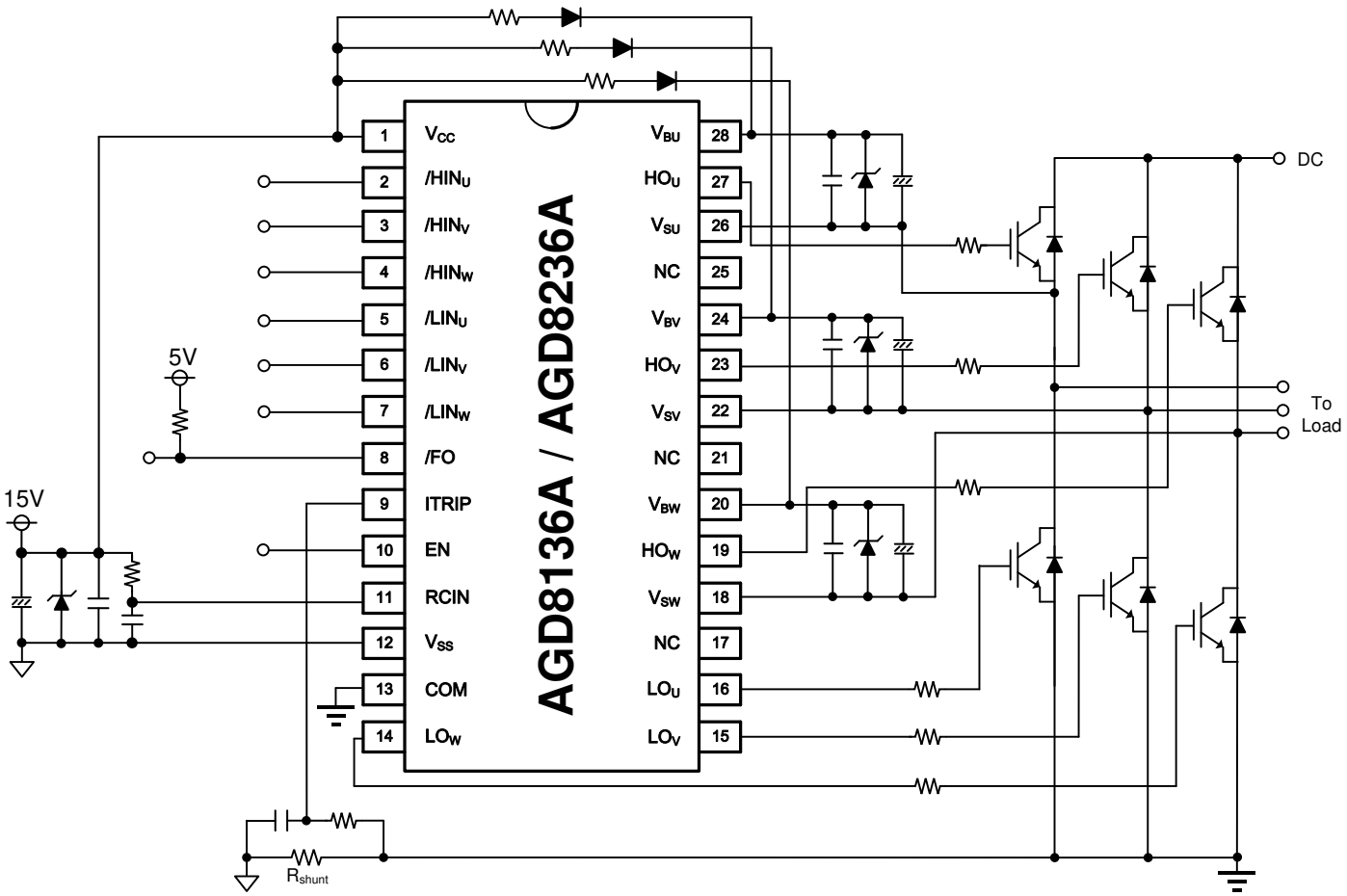
Internal Block Diagram



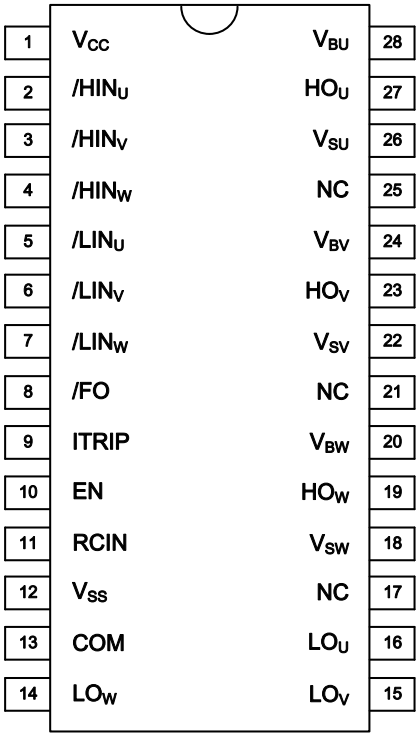
Ordering Information

Part Number	Temperature Range	Package
AGD8136A	-40°C to 125°C	SOP-28L
AGD8236A	-40°C to 125°C	SOP-28L

Typical Application Circuit



Pin Configuration



SOP-28L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	V_{CC}	Low-Side Supply Voltage
2	$/HIN_U$	High-Side Logic Input (U-Phase)
3	$/HIN_V$	High-Side Logic Input (V-Phase)
4	$/HIN_W$	High-Side Logic Input (W-Phase)
5	$/LIN_U$	Low-Side Logic Input (U-Phase)
6	$/LIN_V$	Low-Side Logic Input (V-Phase)
7	$/LIN_W$	Low-Side Logic Input (W-Phase)
8	/FO	Fault Output with Open Drain (Indicates Over-Current and V_{CC} UVLO)
9	ITRIP	Analog Input for Over-Current Shutdown
10	EN	Enable I/O Functionality (Positive Logic)
11	RCIN	External RC-Network Input used to define Fault Output Duration Time
12	V_{SS}	Logic Ground
13	COM	Power Ground
14	LO_W	Low-Side Driver Output (W-Phase)
15	LO_V	Low-Side Driver Output (V-Phase)
16	LO_U	Low-Side Driver Output (U-Phase)

Pin Description *(continued)*

Pin Number	Pin Name	Pin Function
17	NC	No Connection
18	V_{SW}	High-Side Floating Supply Offset Voltage (W-Phase)
19	HO_W	High-Side Driver Output (W-Phase)
20	V_{BW}	High-Side Floating Supply Voltage (W-Phase)
21	NC	No Connection
22	V_{SV}	High-Side Floating Supply Offset Voltage (V-Phase)
23	HO_V	High-Side Driver Output (V-Phase)
24	V_{BV}	High-Side Floating Supply Voltage (V-Phase)
25	NC	No Connection
26	V_{SU}	High-Side Floating Supply Offset Voltage (U-Phase)
27	HO_U	High-Side Driver Output (U-Phase)
28	V_{BU}	High-Side Floating Supply Voltage (U-Phase)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute values referenced to V_{SS} unless otherwise stated in the table.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Low-Side Supply Voltage	-0.3	20 (1)	V
V_{IN}	Logic Input Voltage (/LIN, /HIN)	V_{SS}-0.3	V_{SS}+5.2	
V_{ITRIP}	ITRIP Input Voltage	V_{SS}-0.3	V_{SS}+5.2	
V_{EN}	Enable Input Voltage	V_{SS}-0.3	V_{SS}+5.2	
V_{RCIN}	RCIN Input Voltage	V_{SS}-0.3	V_{CC}+0.3	
V_B	High-Side Floating Supply Voltage	-0.3	620	
V_S	High-Side Floating Supply Offset Voltage	V_B-20 (1)	V_B+0.3	
V_{HO}	High-Side Driver Output Voltage	V_S-0.3	V_B+0.3	
V_{LO}	Low-Side Driver Output Voltage	COM-0.3	V_{CC}+0.3	
V_{FO}	Fault Output Voltage	V_{SS}-0.3	V_{CC}+0.3	
COM	Power Ground	V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Vs Offset Voltage Slew Rate (2)	-	50	V/ns
PW_{HIN}	High-Side Input Pulse Width	500	-	ns
P_D	Package Power Dissipation @ $T_A \le 25°C$	-	1.6	W
$R_{th(j-a)}$	Thermal Resistance, Junction to Ambient	-	78	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	-	300	
ESD	Human Body Model	2		kV

Note:

1. An internal 20V zener diode is integrated to clamp each supply voltage.
2. Not subject of production test, verified by characterization.

Recommended Operation Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise specified. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15 V.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Low-Side Supply Voltage	AGD8136A	10	20	V
		AGD8236A	13.2	20	
V_{IN}	Logic Input Voltage (/LIN, /HIN)		V_{SS}	V_{SS}+5	
V_{EN}	Enable Input Voltage		V_{SS}	V_{SS}+5	
V_B	High-Side Floating Supply Voltage	AGD8136A	V_S+10	V_S+20	
		AGD8236A	V_S+13.2	V_S+20	
V_S	High-Side Floating Supply Offset Voltage (3)		COM-6	600	
$V_S(t)$	Transient High-Side Floating Supply Voltage (4)		-50	600	
V_{HO}	High-Side Driver Output Voltage		V_S	V_B	
V_{LO}	Low-Side Driver Output Voltage		COM	V_{CC}	
COM	Power Ground		-5	5	
V_{FO}	Fault Output Voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN Input Voltage		V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP Input Voltage		V_{SS}	V_{SS}+5	
T_A	Ambient Temperature		-40	125	°C

Note:

3. Logic operation for V_S of -6V to 600V. Logic state held for V_S of -6V to -V_{BS}.
4. Operational for transient negative V_S of V_{SS}-50V with a 50ns pulse width, which is guaranteed by design.

Static Electrical Characteristics

V_{CC} = V_{BS} = 15V. T_A = 25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
UV_{CC+}	V_{CC} Under-Voltage Positive Going Threshold	AGD8136A		8.0	8.9	9.8	V
		AGD8236A		10.8	11.9	13.0	
UV_{CC-}	V_{CC} Under-Voltage Negative Going Threshold	AGD8136A		7.4	8.2	9.0	
		AGD8236A		10.3	11.4	12.5	
UV_{CChys}	V_{CC} Under-Voltage Hysteresis	AGD8136A		-	0.7	-	
		AGD8236A		-	0.5	-	
UV_{BS+}	V_{BS} Under-Voltage Positive Going Threshold	AGD8136A		8.0	8.9	9.8	
		AGD8236A		10.0	11.0	12.0	
UV_{BS-}	V_{BS} Under-Voltage Negative Going Threshold	AGD8136A		7.4	8.2	9.0	
		AGD8236A		9.0	10.0	11.0	
UV_{BShys}	V_{BS} Under-Voltage Hysteresis	AGD8136A		-	0.7	-	
		AGD8236A		-	1.0	-	
I_{LK}	High-Side Floating Supply Leakage Current (per 1-Phase)		V_B=V_S=600V	-	-	50	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{QBS}	Quiescent V_{BS} Supply Current (per 1-Phase)	V_{IN}=5V (all inputs are in the off state)	-	70	120	
I_{QCC}	Quiescent V_{CC} Supply Current (per 1-Phase)		-	1	2	mA
V_{OH}	High Level Output Voltage Drop, V_{BIAS} - V_O	I_O=20mA, V_{IN}=0V	-	0.9	1.4	V
V_{OL}	Low Level Output Voltage Drop, V_O	I_O=20mA, V_{IN}=5V	-	0.4	0.6	
I_{O+}	Output High Current with Capacitive Load	C_L=10nF	120	200	-	mA
I_{Opk+}	Peak Output High Short Circuit Pulsed Current	V_O=0V, PW≤10μs (Single Pulse)	-	220	-	
I_{O-}	Output Low Current with Capacitive Load	C_L=10nF	220	350	-	
I_{Opk-}	Peak Output Low Short Circuit Pulsed Current	V_O=15V, PW≤10μs (Single Pulse)	-	375	-	
V_{IH}	High Level Input Voltage		2.5	-	-	V
V_{IL}	Low Level Input Voltage		-	-	0.8	
V_{CLAMP}	Input Clamp Voltage (/LIN, /HIN, ITRIP, EN)	I_{IN}=100μA	5.2	5.6	5.9	
I_{HIN+}	Input Bias Current	V_{HIN}=5V	-	110	150	μA
I_{HIN-}	Input Bias Current	V_{HIN}=0V	-	150	200	
I_{LIN+}	Input Bias Current	V_{LIN}=5V	-	110	150	
I_{LIN-}	Input Bias Current	V_{LIN}=0V	-	150	200	
$V_{RCIN,TH}$	RCIN Positive Going Threshold		-	8	-	V
I_{RCIN}	RCIN Input Bias Current	V_{RCIN}=0V or 15V	-	-	1	μA
$R_{RCIN,ON}$	RCIN Low On-Resistance	I=1.5mA	-	50	100	Ω
$V_{IT,TH+}$	ITRIP Positive Going Threshold		0.42	0.46	0.5	V
$V_{IT,TH-}$	ITRIP Negative Going Threshold		-	0.4	-	
$V_{IT,Hys}$	ITRIP Hysteresis		-	0.06	-	
I_{ITRIP+}	High ITRIP Input Bias Current	V_{ITRIP}=4V	-	5	40	μA
I_{ITRIP-}	Low ITRIP Input Bias Current	V_{ITRIP}=0V	-	-	1	
$V_{EN,TH+}$	EN Positive Going Threshold		-	-	2.5	V
$V_{EN,TH-}$	EN Negative Going Threshold		0.8	-	-	
I_{EN+}	High EN Input Bias Current	V_{EN}=5V	-	5	40	μA
I_{EN-}	Low EN Input Bias Current	V_{EN}=0V	-	-	1	
$R_{FO,ON}$	Fault Low On-Resistance	I=1.5mA	-	50	100	Ω

Dynamic Electrical Characteristics

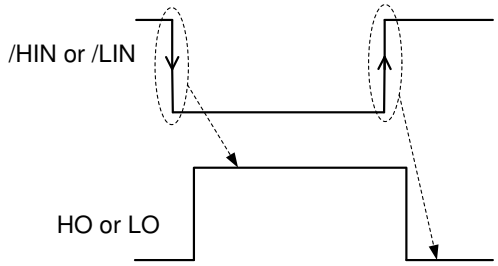
V_{BIAS} (V_{CC} or V_{BS}) = 15V, C_L = 1000pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
t_{ON}	Turn-On Propagation Delay		V_{IN}=0V or 5V	400	530	750	ns
t_{OFF}	Turn-Off Propagation Delay			400	530	750	
t_R	Turn-On Rise Time			-	125	190	
t_F	Turn-Off Fall Time			-	50	75	
$t_{IN,FLT}$	Input Filter Time (/LIN, /HIN) (5)			200	350	510	
t_{EN}	EN Low to Output Shutdown Propagation Delay		V_{IN}=0V V_{EN}=5V → 0V	250	460	650	
$t_{EN,FLT}$	EN Input Filter Time			100	200	-	
t_{FOd}	Fault Output Duration Time (RCIN: C = 1nF, R = 2MΩ)		V_{ITRIP}=1V	1.3	1.65	-	ms
t_{ITRIP}	ITRIP to Output Shutdown Propagation Delay	Low Side	V_{ITRIP}=5V, V_{IN}=0V, V_{FO}=5V (10kΩ pull-up)	420	620	970	ns
		High Side		600	800	1150	
$t_{IT,FLT}$	ITRIP Filter Time			-	400	-	
t_{FO}	ITRIP to FO Propagation Delay			400	600	950	
DT	Dead Time (6)		V_{IN}=0V or 5V without External Dead Time	100	275	420	
MT	Matching Delay Time (t_{ON}, t_{OFF}) (7)		$\lvert t_{ON(HO)} - t_{ON(LO)} \rvert$ or $\lvert t_{OFF(HO)} - t_{OFF(LO)} \rvert$	-	-	100	
PM	Output Pulse Width Matching (8)		Input Pulse Width=10µs	-	-	150	

Note:

5. The minimum width of the input pulse is recommended to exceed 500ns to ensure the filtering time of the input filter.
6. Please refer to 'Dead Time' definition of 'Function Diagram'.
7. This parameter, MT and MDT applies to all of the channels.
8. PM is defined as |(input pulse width) – (output pulse width)|.

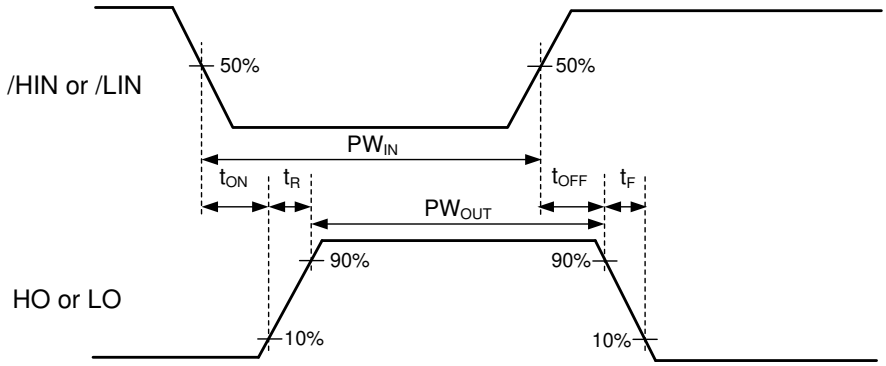
Output Activation



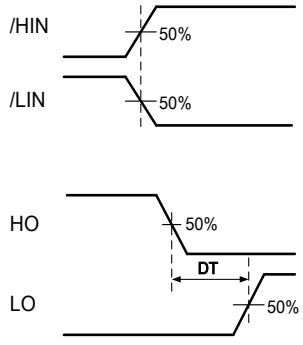
EN	/HIN	/LIN	HO	LO
L	L or H	L or H	L	L
H	H	L	L	H
	L	H	H	L

Note: Output signal (HO or LO) is triggered by the edge of input signal.

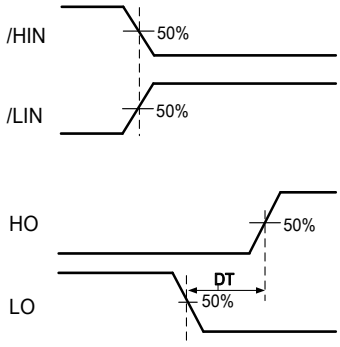
Input / Output Timing Diagram



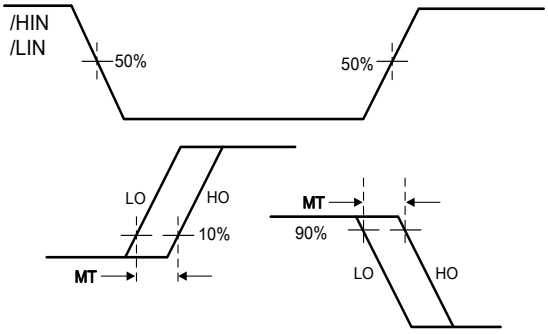
Dead Time Activation



</HIN off and /LIN on>



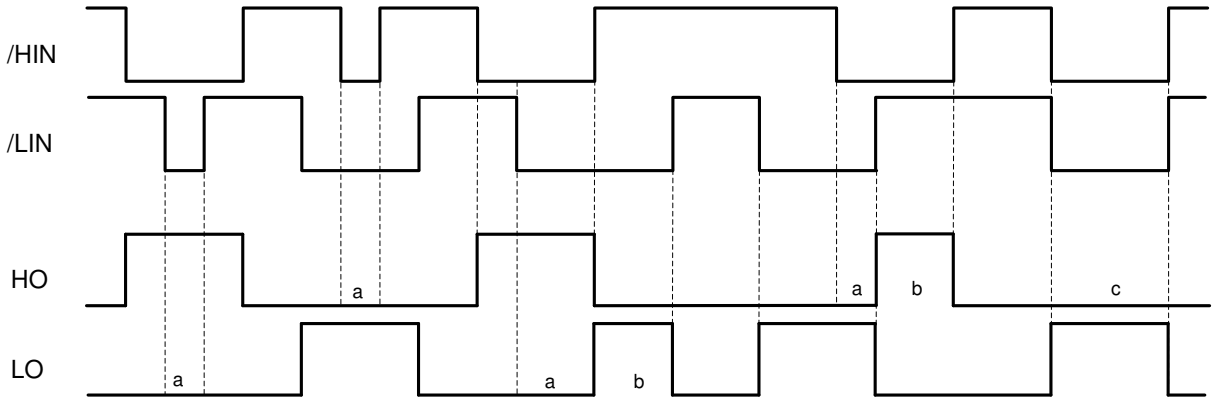
</HIN on and /LIN off>



<Delay Matching Waveform Definition>

Function Timing Diagram

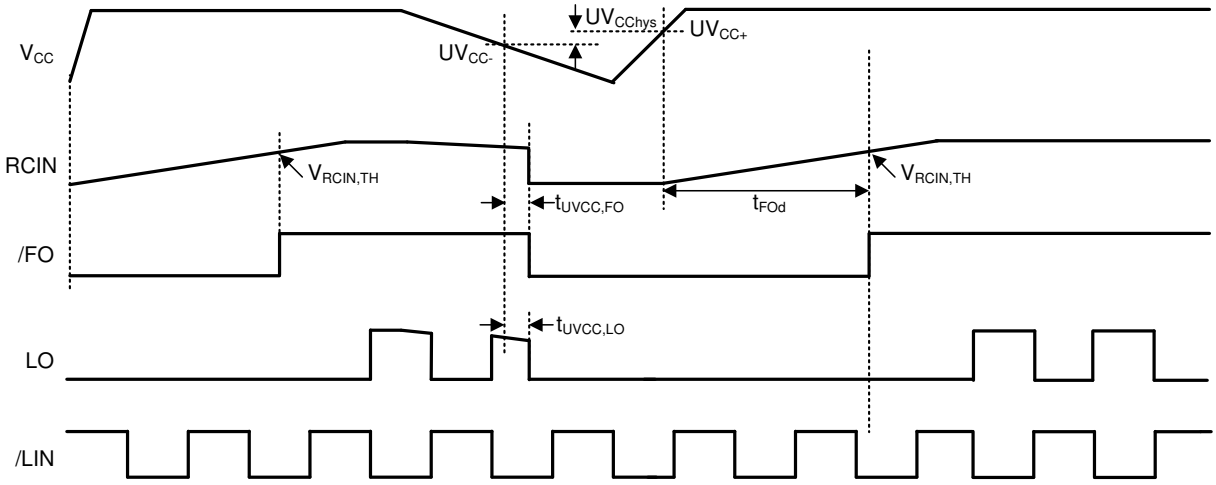
A. Illustration of Shoot-Through (Cross-Conduction) Protection Logic



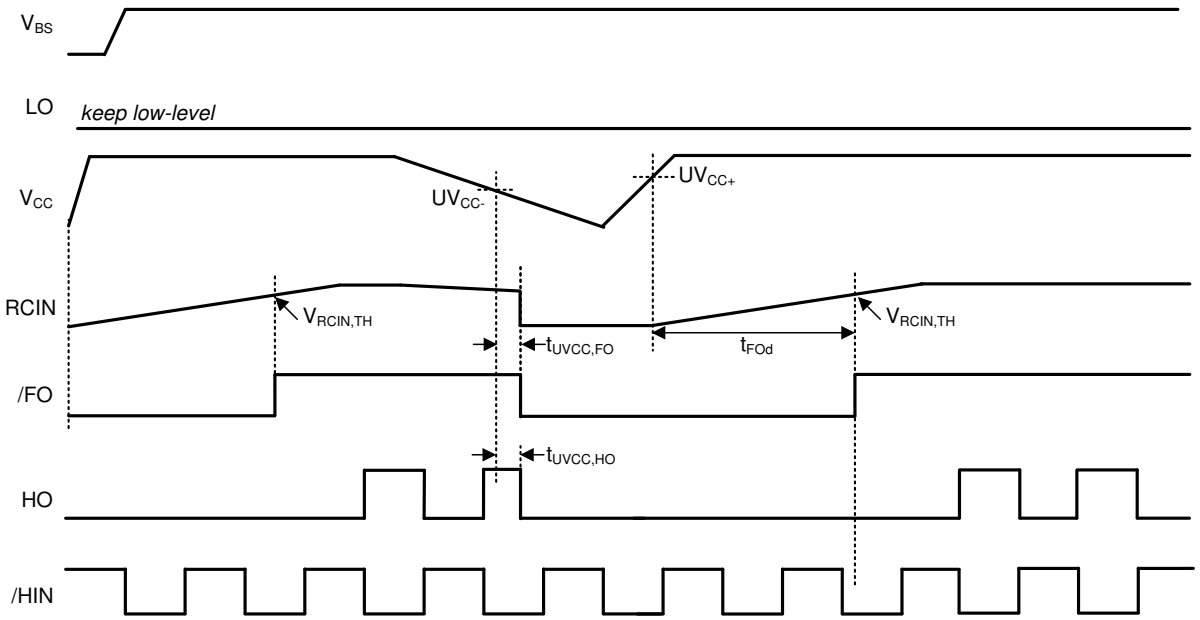
Note:
a. When one output (high or low side) is turned on, the other side turn-on input is ignored.
b. If both outputs are changed simultaneously, the turn-on activation is done by the internal dead time of 275ns typ. (For more information, please refer to below 'Dead Time' section.)
c. When high-side (/HIN) and low-side (/LIN) have turn-on inputs at the same time, low-side (/LIN) has the priority.

B. V_{CC} (V_{BS}) Supply Under-Voltage (UV) Lockout Timing Diagram

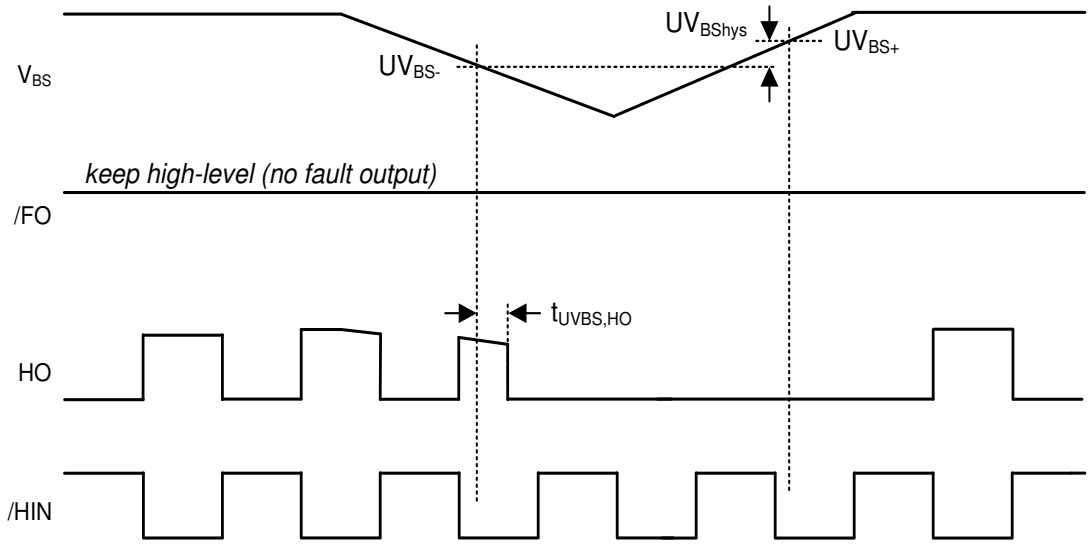
a. LO operation by V_{CC} under-voltage protection



b. HO operation by V_{CC} under-voltage protection

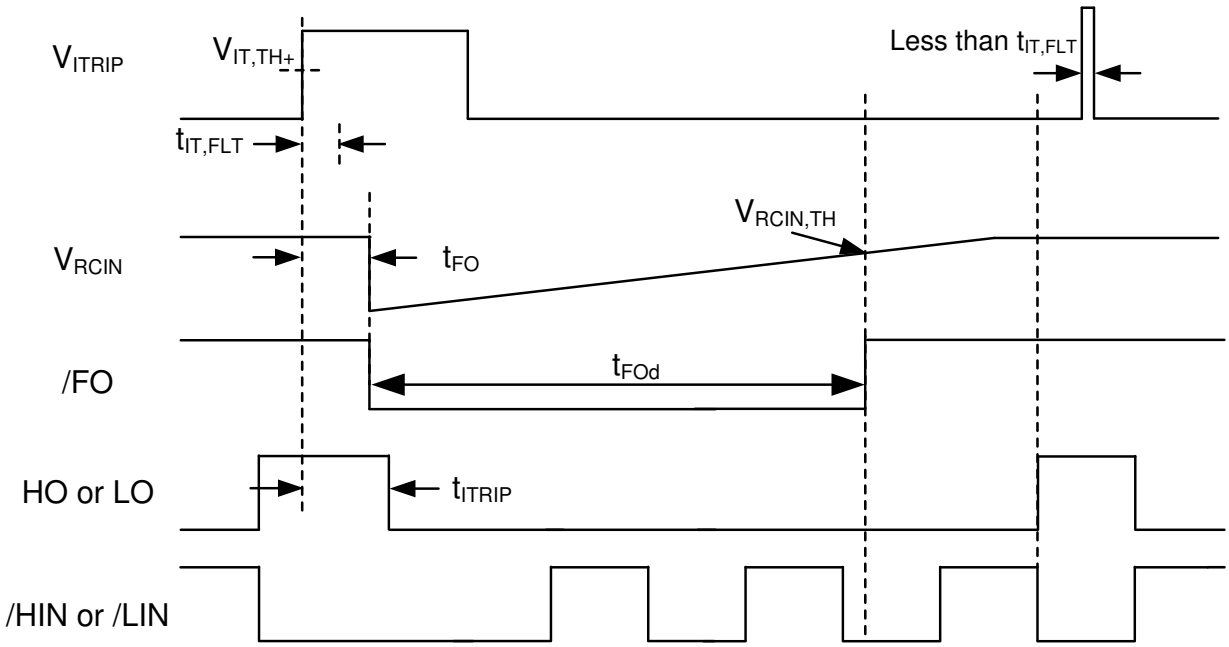


c. V_{BS} supply under-voltage (UV) lockout timing diagram

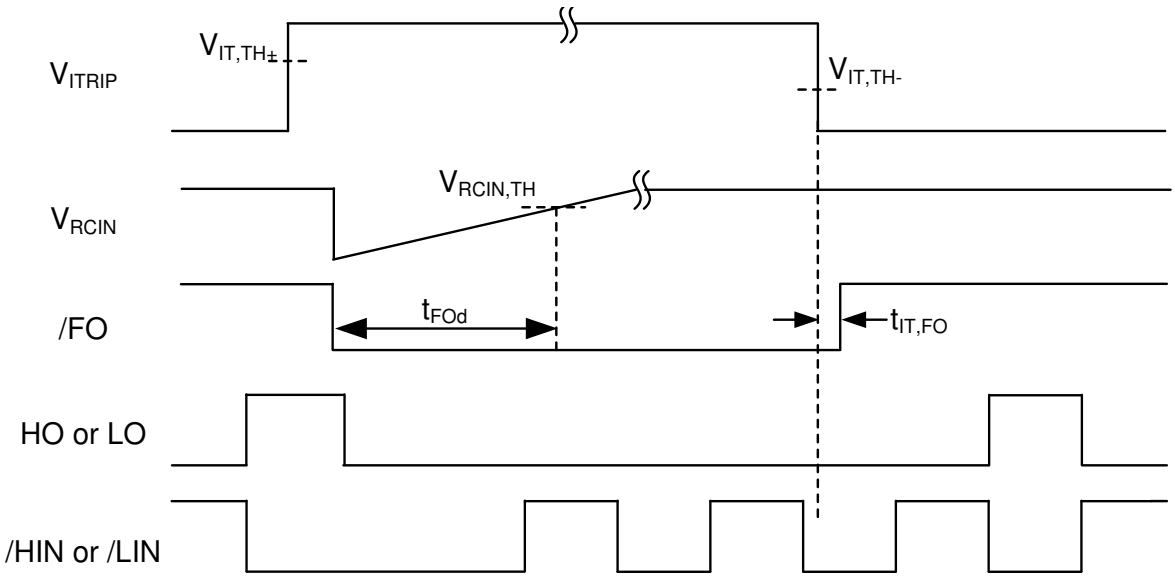


C. Over-Current Protection

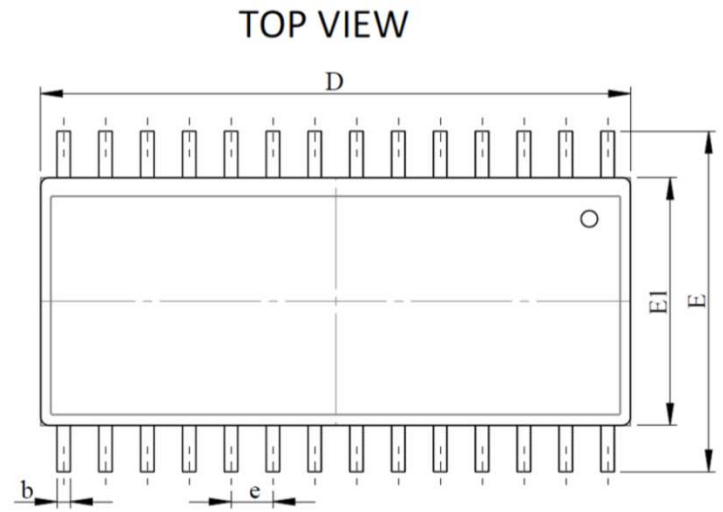
a. When ITRIP voltage rises higher than positive going threshold for t < t_{FOd}

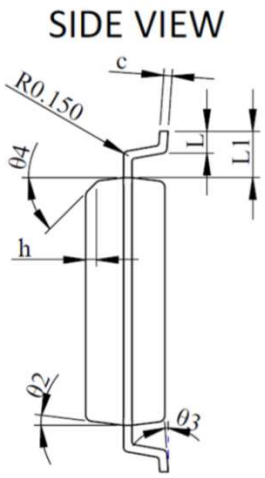


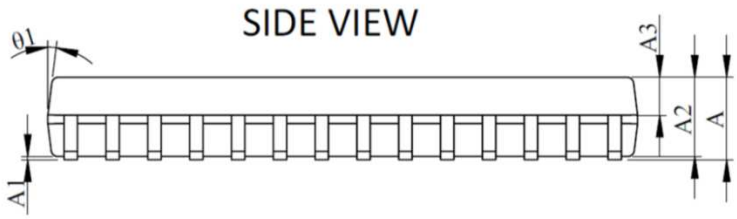
b. When ITRIP voltage keeps longer than t_{FOd}

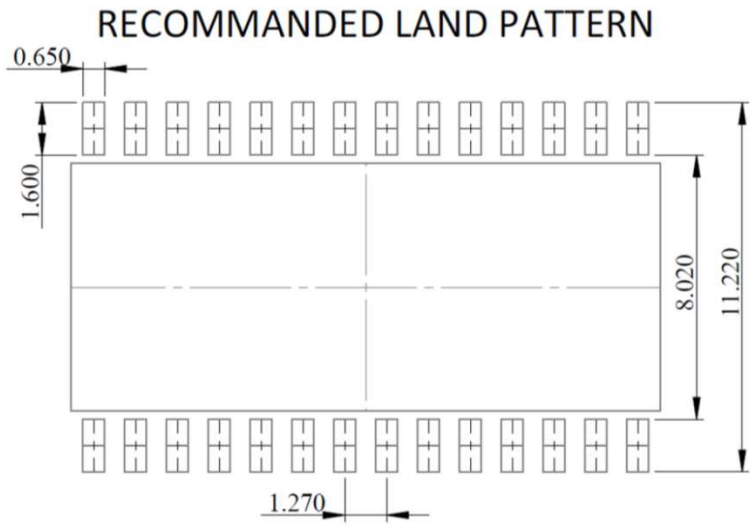


Package Dimensions, SOP-28L









SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	2.354	---	2.654
A1	0.1	---	0.3
A2	2.254	---	2.554
A3	1	---	1.3
D	17.8	17.9	18
E	10.1	10.34	10.58
E1	7.42	7.52	7.57
L	0.405	0.705	0.905
L1	1.21	1.41	1.61
e	1.27TYP.		
b	0.41TYP.		
c	0.254TYP.		
θ1	7°TYP.		
θ2	7°TYP.		
θ3	0°	---	8°
θ4	45°TYP.		
h	0.381TYP.		

NOTES
1. CONTROLLING DIMENSION : MM.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.

LEGAL DISCLAIMER

Alpha and Omega Semiconductor makes no representations or warranties with respect to the accuracy or completeness of the information provided herein and takes no liabilities for the consequences of use of such information or any product described herein. Alpha and Omega Semiconductor reserves the right to make changes to such information at any time without further notice. This document does not constitute the grant of any intellectual property rights or representation of non-infringement of any third party's intellectual property rights.

LIFE SUPPORT POLICY

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.