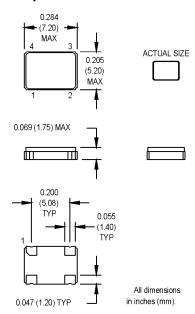
M1 Series 5.0 X 7.0 X 1.75 mm HCMOS/TTL **Compatible 5.0 Volt Surface Mount Oscillators**

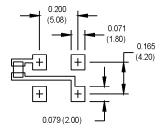




Low Profile, High Performance HCMOS/TTL **Compatible 5.0 Volt Surface Mount Oscillators**



SUGGESTED SOLDER PAD LAYOUT



NOTE: A capacitor of value 0.01 μF or greater between Vdd and Ground is recommended.

Pin Connections

PIN	FUNCTION			
1	N/C or Tri-state			
2	Ground			
3	Output			
4	+Vdd			

Tri-state Control Logic

Pin 1 high or floating: clock signal output. Pin 1 low: output disabled to high impedance.

Ordering Information 00.0000 M1 MHz Product Series Temperature Range 1: 0°C to +70°C 2: -40°C to +85°C 6: -20°C to +70°C Stability 3: ±100 ppm 4: ±50 ppm **5**: ±35 ppm 6: ±25 ppm 8: ±20 ppm **Output Type** F: Fixed T: Tristate Symmetry/Logic Compatibility A: 40/60 TTL/HCMOS (50.000 MHz and below) C: 45/55 HCMOS G: 40/60 HCMOS (50.001 to 125.000 MHz) Package/Lead Configurations N: Leadless Frequency (customer specified)

Electrical Specifications

Standard Operating Conditions • 0°C to +70°C; Vdd = 5.0 ±10% VDC							
	A & C SYMMETRY/LOGIC						
	TTL Load		HCMOS Load				
PARAMETERS	MIN.	MAX.	MIN.	MAX.	UNITS		
Frequency Range ¹	1.500	50.000	1.500	50.000	MHz		
Output Load ²		10		50	TTL/pF		
Symmetry ³	40/60	60/40	40/60	60/40	%		
Logic "0" Level		0.5		10% Vdd	V		
Logic "1" Level	Vdd-0.5		90% Vdd		V		
Rise/Fall Time 4		10		10	ns		
Supply Current							
1.500 to 20.000 MHz		20		20	mA		
20.001 to 50.000 MHz		35		45	mA		
Frequency Range ¹			50.001	125.000	MHz		
Output Load ²							
50.001 to 67.000 MHz				50	pF		
67.001 to 125.000 MHz				15	pF		
Symmetry ³			40/60	60/40	%		
Logic "0" Level				10% Vdd	V		
Logic "1" Level			90% Vdd		V		
Rise/Fall Time 4							
50.001 to 67.000 MHz				10	ns		
67.001 to 125.000 MHz				3	ns		
Supply Current				65	mA		

¹ Because this product is based on AT-strip technology, not all frequencies in the range stated are available.

Contact the factory for availability of specific frequencies.

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TTL load - See load circuit diagram #1 on page 113. HCMOS load - See load circuit diagram #2 on page 113. ³ Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.

⁴ Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load. See page 112, Figure "2" for suggested solder profile.