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CORPORATION

N-Channel Enhancement-Mode MOS Transistor

2N7000 / BS170L

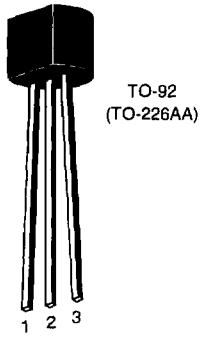
DESCRIPTION

The 2N7000 utilizes Calogic's vertical DMOS technology. The device is well suited for switching applications where B_V of 60V and low on resistance (under 5 ohms) are required. The 2N7000 is housed in a plastic TO-92 package.

ORDERING INFORMATION

Part	Package	Temperature Range
2N7000	Plastic TO-92	-55°C to +150°C
BS170L	Plastic TO-92	-55°C to +150°C
X2N7000	Sorted Chips in Carriers	-55°C to +150°C

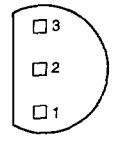
PIN CONFIGURATION



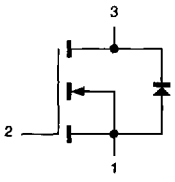
TO-92
(TO-226AA)

2N7000

1 SOURCE
2 GATE
3 DRAIN

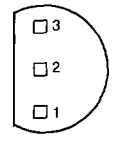


BOTTOM VIEW



BS170L

1 DRAIN
2 GATE
3 SOURCE



BOTTOM VIEW

CD5

PRODUCT SUMMARY

P/N	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
2N7000	60	5	0.2
BS170	60	5	0.5

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETERS	LIMITS	UNITS	TEST CONDITIONS
V_{DS}	Drain-Source Voltage	60	V	
V_{GS}	Gate-Source Voltage	±40		
I_D	Continuous Drain Current	0.2	A	T_A = 25°C
		0.13		T_A = 100°C
I_{DM}	Pulsed Drain Current[1]	0.5		
P_D	Power Dissipation[1]	0.4	W	T_A = 25°C
		0.16		T_A = 100°C
T_J	Operating Junction Temperature Range	-55 to 150	°C	
T_{stg}	Storage Temperature Range	-55 to 150		
T_L	Lead Temperature (1/16" from case for 10 sec.)	300		

THERMAL RESISTANCE RATINGS

SYMBOL	THERMAL RESISTANCE	LIMITS	UNITS
R_{thJA}	Junction-to-Ambient	312.5	K/W

NOTE: 1. Pulse width limited by maximum junction temperature.

SPECIFICATIONS[1]

SYMBOL	PARAMETER	MIN	TYP[2]	MAX	UNIT	TEST CONDITIONS
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	70		V	I_D = 10µA, V_{GS} = 0V
$V_{GS(th)}$	Gate-Threshold Voltage	0.8	1.9	3		V_{DS} = V_{GS}, I_D = 1mA
I_{GSS}	Gate-Body Leakage			±10	nA	V_{GS} = ±15V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			1	µA	V_{DS} = 48V, V_{GS} = 0V
				1000		T_C = 125°C
$I_{D(ON)}$	On-State Drain Current[3]	75	210		mA	V_{DS} = 10V, V_{GS} = 4.5V
$r_{DS(ON)}$	Drain-Source On-Resistance[3]		4.8	5.3	Ω	[4]V_{GS} = 4.5V, I_D = 75mA
			2.5	5		V_{GS} = 10V, I_D = 0.5A
			4.4	9		T_C = 125°C
$V_{DS(ON)}$	Drain-Source On-Voltage[3]		0.36	0.4	V	[4]V_{GS} = 4.5V, I_D = 75mA
			1.25	2.5		V_{GS} = 10V, I_D = 0.5A
			2.2	4.5		T_C = 125°C[4]
g_{FS}	Forward Transconductance[3]	100	170		mS	V_{DS} = 10V, I_D = 0.2A
g_{OS}	Common Source Output Conductance[3, 4]		500		µS	V_{DS} = 5V, I_D = 50mA
DYNAMIC						
C_{iss}	Input Capacitance		16	60	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz
C_{oss}	Output Capacitance[4]		11	25		
C_{rss}	Reverse Transfer Capacitance		2	5		
SWITCHING						
t_{ON}	Turn-On Time		7	10	nS	V_{DD} = 15V, R_L = 25Ω, I_D = 0.5A V_{GEN} = 10V, R_G = 25Ω (Switching time is essentially independent of operating temperature)
t_{OFF}	Turn-Off Time		7	10		

NOTES: 1. T_A = 25°C unless otherwise specified.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = ≤300µS, duty cycle ≤3%.
4. This parameter not registered with JEDEC.