LOGIC DEVICES INCORPORATED

L29C524/525
Dual Pipeline Register

T-46-09-09

FEATURES

- Pipeline Registers — Dual 7-Deep (L29C524) or Dual 8-Deep (L29C525)
- Configurable to Single 14-Deep and Single 16-Deep
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD AM29524 and AM29525
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin CerDIP
  - 28-pin Plastic LCC
  - 28-pin Ceramic Flatpack

DESCRIPTION

The Logic Devices **L29C524** and **L29C525** are high performance, low power CMOS pipeline registers. They are pin-for-pin compatible with the Advanced Micro Devices Am29524 and Am29525. The products can be configured as two independent, 7-level (or 8-level) pipelines or as single 14-level (or 16-level) pipelines. The configuration implemented is determined by the instruction code (I_1,I_0) as shown in Table 2.

The I_1,I_0 instruction code controls the internal routing of data and loading of each register. For instruction I_1,I_0 = 00 (Push A & B), data applied at the D_7–D_0 inputs is loaded into register A_0 at the rising edge of the Clock. The contents of A_0 simultaneously moves to register A_1, A_1 moves to A_2, and so on. The contents of the last register on the "A" side (A_6 for the L29C524, A_7 for the L29C525) are wrapped back to register B_0. The registers on the B side are similarly shifted, with the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) lost.

Instruction I_1,I_0 = 01 (Push B) acts similarly to the Push A & B instruction, except that only the B side registers are shifted. The input data is applied to register B_0, and the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) are lost. The contents of the A side registers are unaffected. Instruction I_1,I_0 = 10 (Push A) is identical to the Push B instruction, except that A side registers are shifted and B side registers are unaffected.

Instruction I_1,I_0 = 11 (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_3–S_0 control inputs. On the L29C524, the input pins D_7–D_0 may also be selected to drive the output, and all output pins may be forced to zero. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_3–S_0 controls is given in Table 3.

L29C524/525 Block Diagram

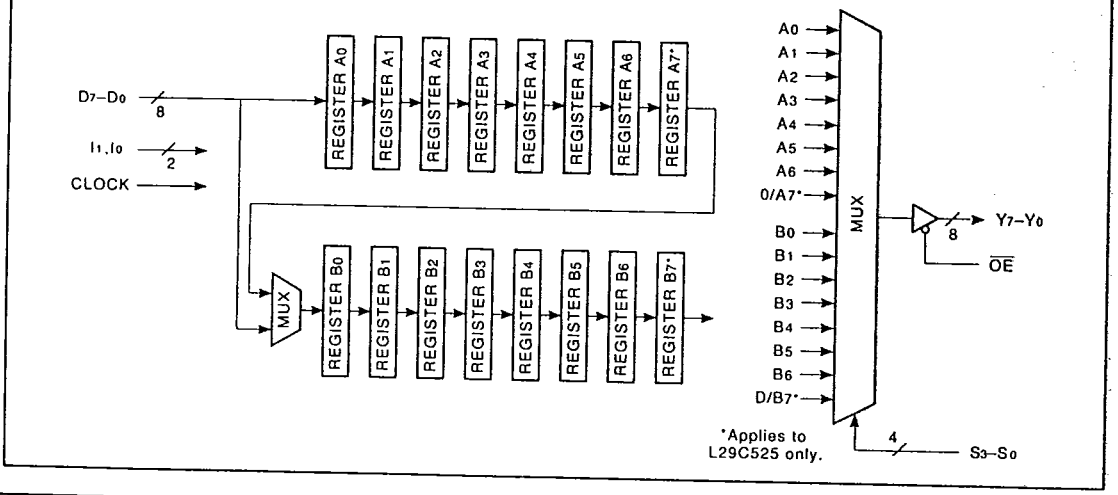
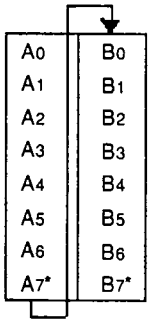
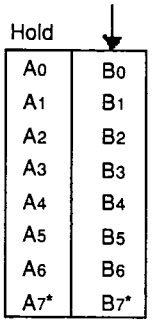
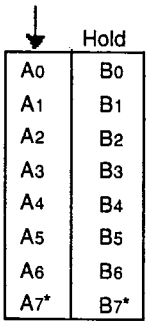
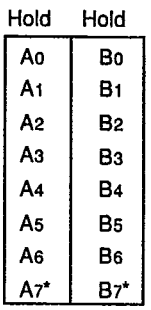


TABLE 1. REGISTER LOAD OPERATIONS *(See Table 2 for Instruction Codes.)*

Single 14/16 Level	Dual 7/8 Level		
Push A & B	**Push B**	**Push A**	**No-Op**
			

* A7 and B7 registers apply only to L29C525

TABLE 2. INSTRUCTION SET DESCRIPTIONS

Mnemonic	Inputs I_1	Inputs I_0	Description
Shift	0	0	Push A & B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	No-Op

TABLE 3. SELECT OPERATION DESCRIPTIONS

S_3	S_2	S_1	S_0	Y_7–Y_0
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	0 (L29C524) A7 (L29C525)
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	D7–D0 (L29C524) B7 (L29C525)

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
Vcc supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc (Note12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc (Note12)			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, Vcc = Max (Notes 4, 8)			−250	mA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		10	35	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

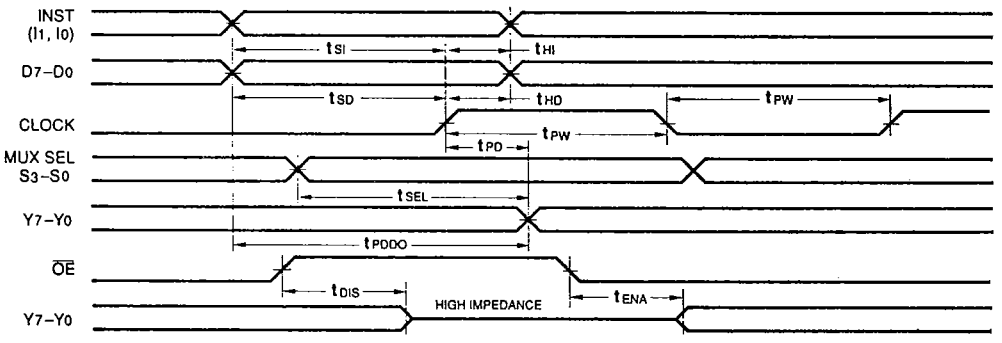
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C524/525- 20 Min	20 Max	15 Min	15 Max
t_{PD}	CLK to Y_7–Y_0		20		15
t_{SEL}	S_3–S_0 to Y_7–Y_0		20		15
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)		20		15
t_{SD}	D_7–D_0 to CLK Setup	7		5	
t_{HD}	CLK to D_7–D_0 Hold	0		0	
t_{SI}	I_1,I_0 to CLK Setup	7		5	
t_{HI}	CLK to I_1,I_0 Hold	2		2	
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)		13		13
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)		15		15
t_{PW}	Clock Pulse Width	12		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C524/525- 25 Min	25 Max	20 Min	20 Max
t_{PD}	CLK to Y_7–Y_0		25		20
t_{SEL}	S_3–S_0 to Y_7–Y_0		25		20
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)		25		20
t_{SD}	D_7–D_0 to CLK Setup	7		7	
t_{HD}	CLK to D_7–D_0 Hold	2		2	
t_{SI}	I_1,I_0 to CLK Setup	7		7	
t_{HI}	CLK to I_1,I_0 Hold	2		2	
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)		13		13
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)		15		15
t_{PW}	Clock Pulse Width	12		12	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at GND – 0.6 V.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

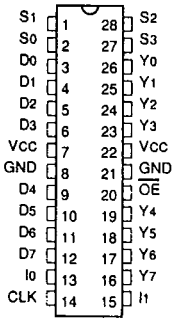
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

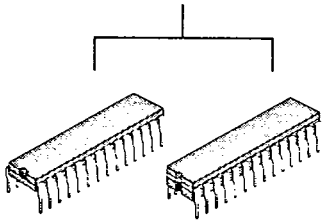
LOGIC DEVICES INCORPORATED

Dual Pipeline Register

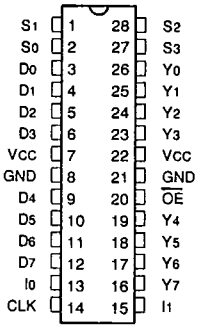
ORDERING INFORMATION

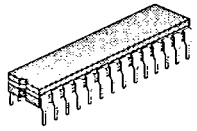
28-pin* (0.3" wide)



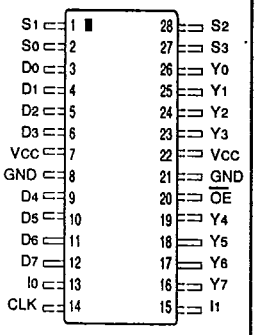


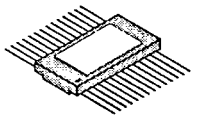
28-pin* (0.4" wide)



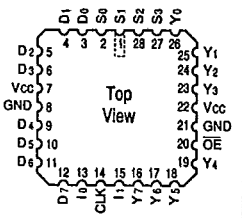


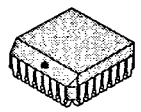
28-pin Flatpack





28-pin





Speed	Plastic DIP* (P10)	CerDIP (C5)	CerDIP* (C10)	Ceramic Flatpack (F2)	Plastic Leaded Chip Carrier (J4)
	0°C to +70°C — Commercial Screening				
20 ns 15 ns	L29C524PC20 " " 15 or L29C525PC20 " " 15	L29C524CC20 " " 15 or L29C525CC20 " " 15	L29C524IC20 " " 15 or L29C525IC20 " " 15	L29C524FC20 " " 15 or L29C525FC20 " " 15	L29C524JC20 " " 15 or L29C525JC20 " " 15
	−55°C to +125°C — Commercial Screening				
25 ns 20 ns		L29C524CM25 " " 20 or L29C525CM25 " " 20	L29C524IM25 " " 20 or L29C525IM25 " " 20	L29C524FM25 " " 20 or L29C525FM25 " " 20	
	−55°C to +125°C — Extended Screening				
25 ns 20 ns		L29C524CME25 " " 20 or L29C525CME25 " " 20	L29C524IME25 " " 20 or L29C525IME25 " " 20	L29C524FME25 " " 20 or L29C525FME25 " " 20	
	−55°C to +125°C — MIL-STD-883 Compliant				
25 ns 20 ns		L29C524CMB25 " " 20 or L29C525CMB25 " " 20	L29C524IMB25 " " 20 or L29C525IMB25 " " 20	L29C524FMB25 " " 20 or L29C525FMB25 " " 20	

***Also available in 0.4" wide Plastic DIP Package (P11). Use part number L29C52xNCxx.**

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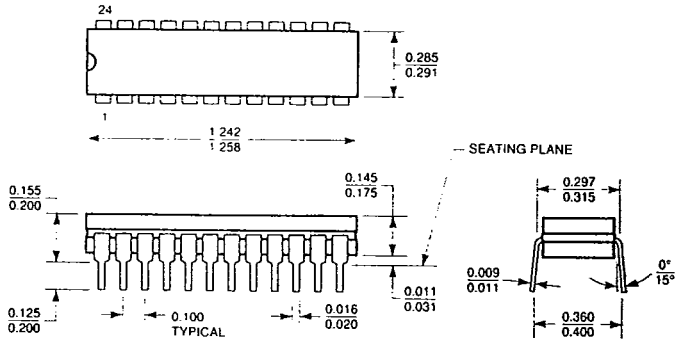
Mechanical Drawings

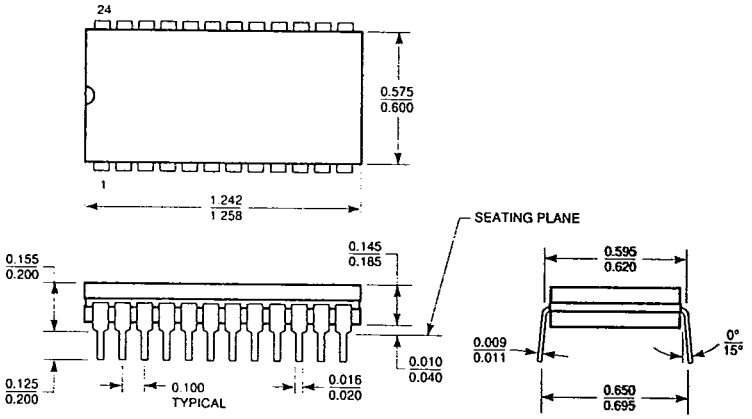
CerDIP — Type C

T-90-20

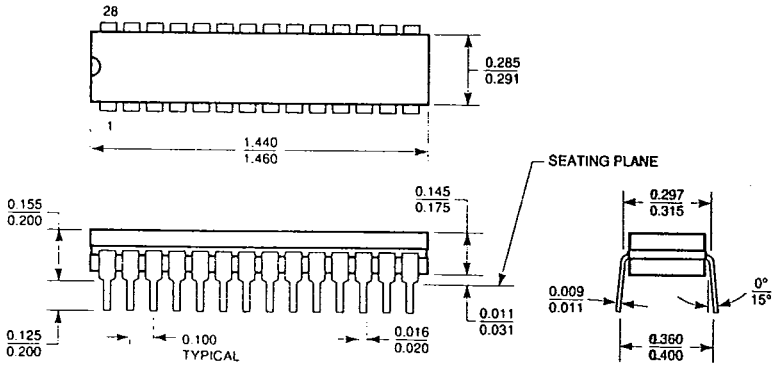
C1 — 24-pin CerDIP (0.3" Wide)



C4 — 24-pin CerDIP (0.6" Wide)



C5 — 28-pin CerDIP (0.3" Wide)



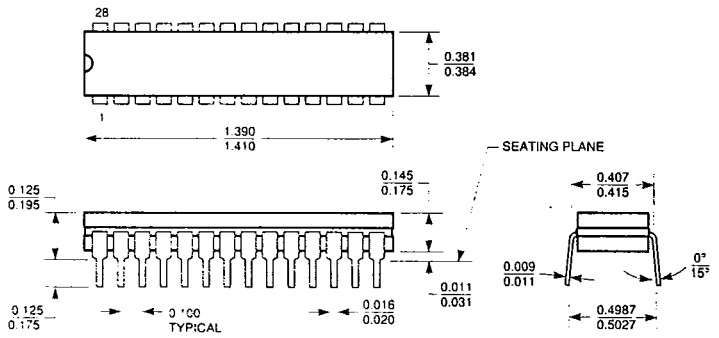
LOGIC DEVICES INCORPORATED

Mechanical Drawings

T-90-20

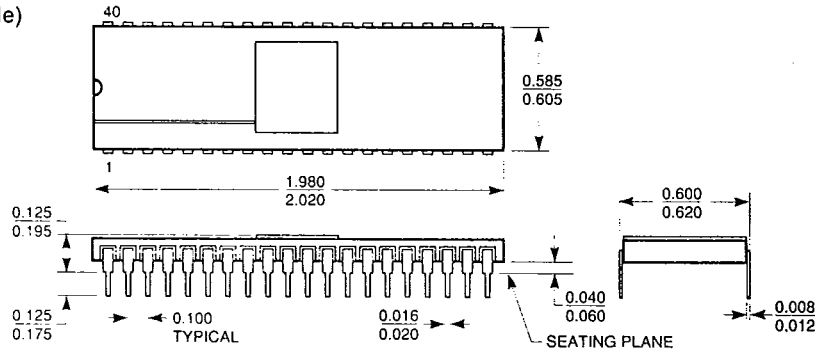
CerDIP — Type C

C10 — 28-pin CerDIP (0.4" Wide)



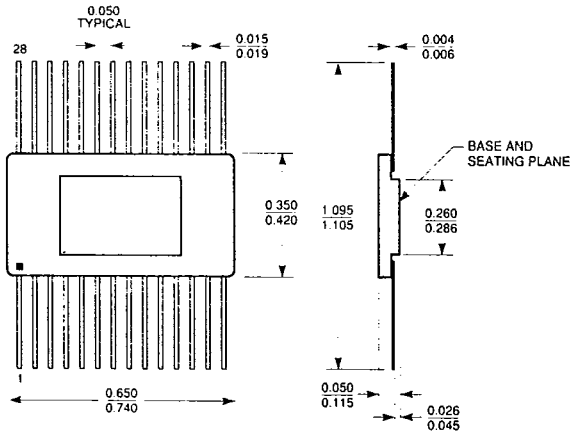
Sidebraze, Hermetic DIP — Type D

D3 — 40-pin Hermetic DIP (0.6" Wide)



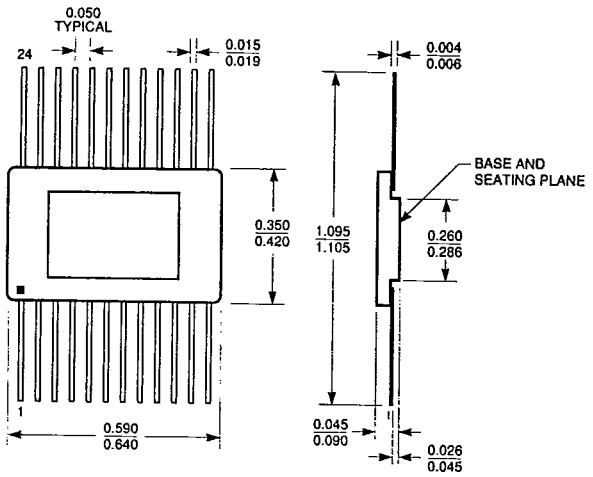
Ceramic Flat Pack — Type F

F1 — 24-pin Ceramic Flat Pack



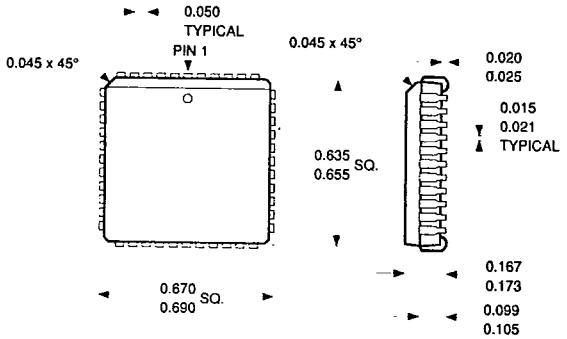
Ceramic Flat Pack — Type F

F2 — 28-pin Ceramic Flat Pack

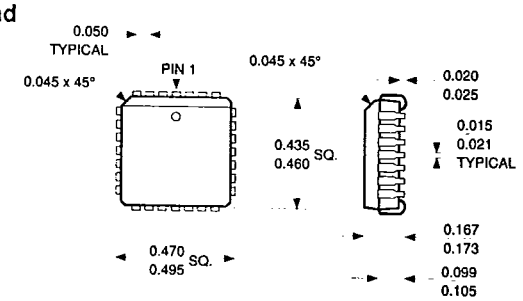


Plastic J-Lead Chip Carrier — Type J

J1 — 44-pin Plastic J-Lead (0.690" x 0.690")



J4 — 28-pin Plastic J-Lead (0.490" x 0.490")



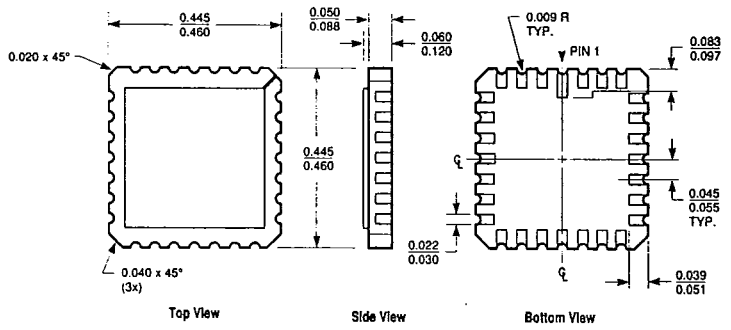
LOGIC DEVICES INCORPORATED

Mechanical Drawings

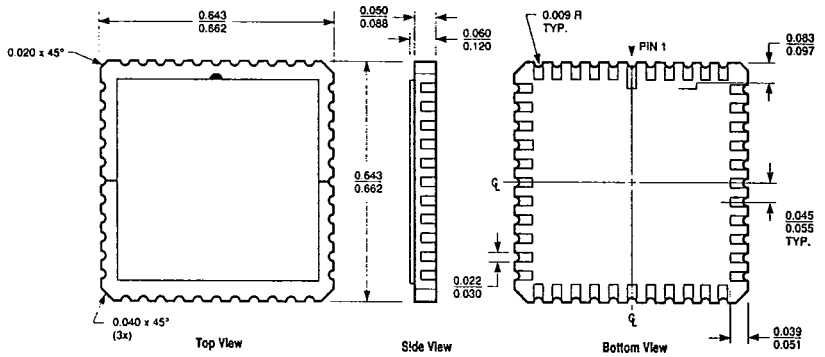
T-90-20

Ceramic Leadless Chip Carrier — Type K

K1 — 28-pin Ceramic LCC (0.450" x 0.450")

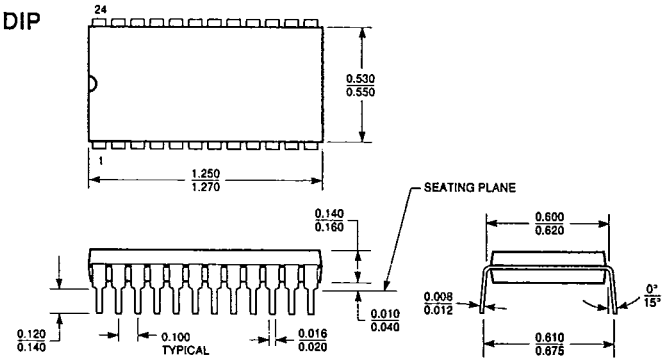


K2 — 44-pin Ceramic LCC (0.650" x 0.650")



Plastic DIP — Type P

P1 — 24-pin Plastic DIP (0.6" Wide)



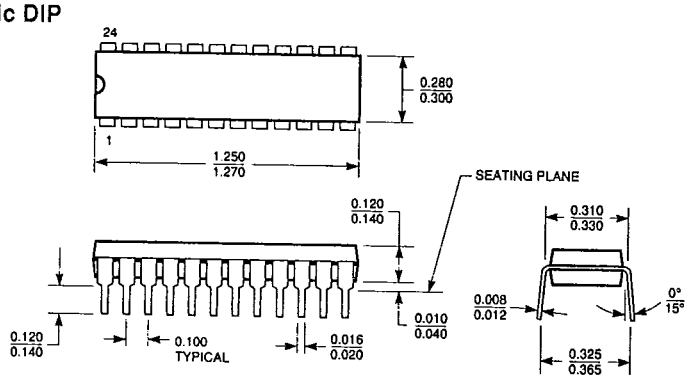
LOGIC DEVICES INCORPORATED

Mechanical Drawings

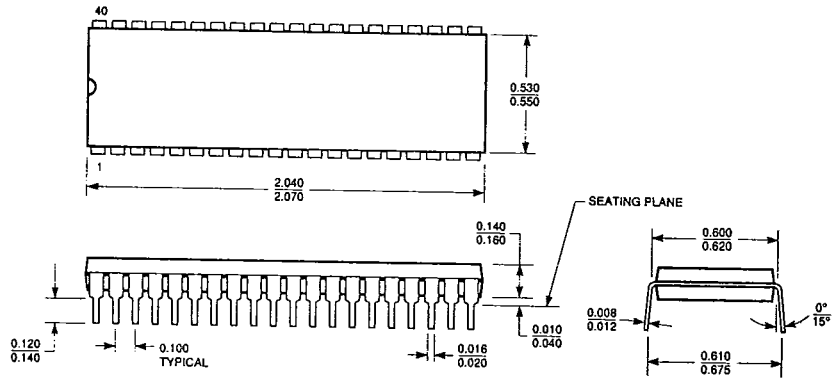
T-90-20

Plastic DIP — Type P

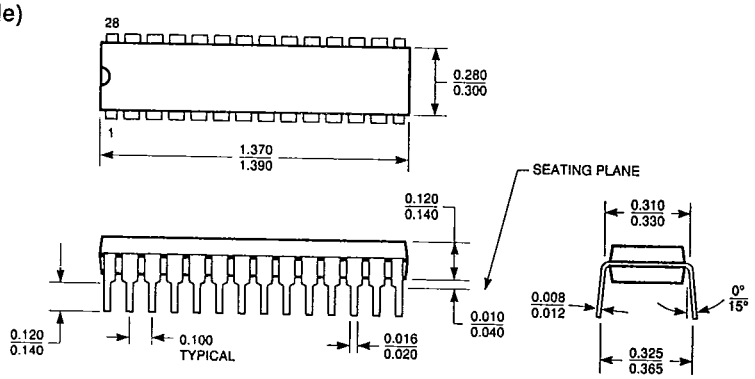
P2 — 24-pin Plastic DIP (0.3" Wide)



P3 — 40-pin Plastic DIP (0.6" Wide)



P10 — 28-pin Plastic DIP (0.3" Wide)



Plastic DIP — Type P

P11 — 28-pin Plastic DIP (0.4" wide)