

37-40GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

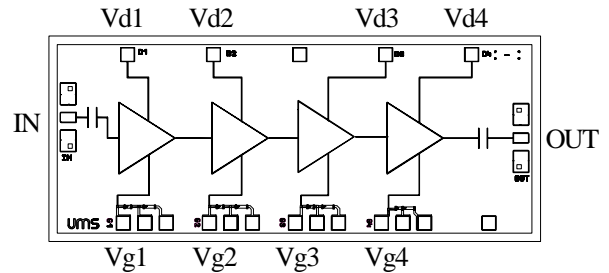
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Description

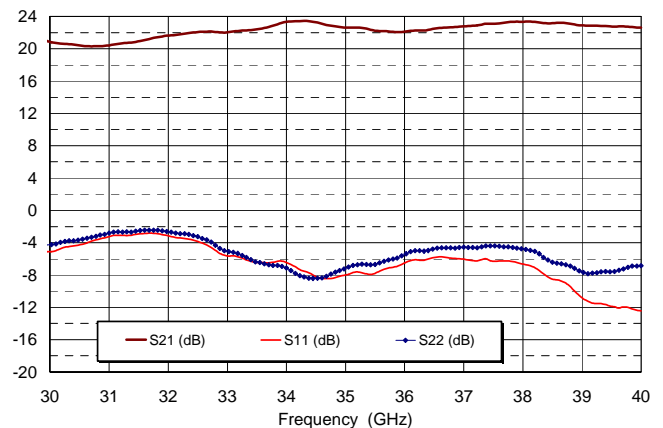
The CHA5292a is a high gain four-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.15 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on jig Measurements



Main Features

- Performances : 37-40GHz
- 24dBm output power @ 1dB comp. gain
- 24 dB \pm 1dB gain
- DC power consumption, 500mA @ 3.5V
- Chip size : 3.43 x 1.44 x 0.07 mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	37		40	GHz
G	Small signal gain		24		dB
P1dB	Output power at 1dB gain compression		24		dBm
Id	Bias current		500		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics

Tamb = +25°C, Vd = 3.5V Id = 500mA

preliminary

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	37		40	GHz
G	Small signal gain (1)		24		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation		35		dB
P1dB	Pulsed output power at 1dB compression (1)		24		dBm
P03	Output power at 3dB gain compression (1)		26		dBm
VSWRin	Input VSWR (2)		3:1		
VSWRout	Output VSWR (2)		3.5:1		
Tj	Junction temperature for 80°C backside		160		°C
Id	Bias current @ small signal		500	650	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) Value representative for CW on jig measurement.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage with Pin max=0dBm	+4.0	V
Id	Drain bias current	750	mA
Vg	Gate bias voltage	-2 to +0.4	V
Ig	Gate bias current	-1.8 to +1.8	mA
Vdg	Maximum drain to gate voltage (Vd - Vg)	+6.0	V
Pin	Maximum input power overdrive (2)	+3.0	dBm
Tch	Maximum channel temperature	+175	°C
Ta	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

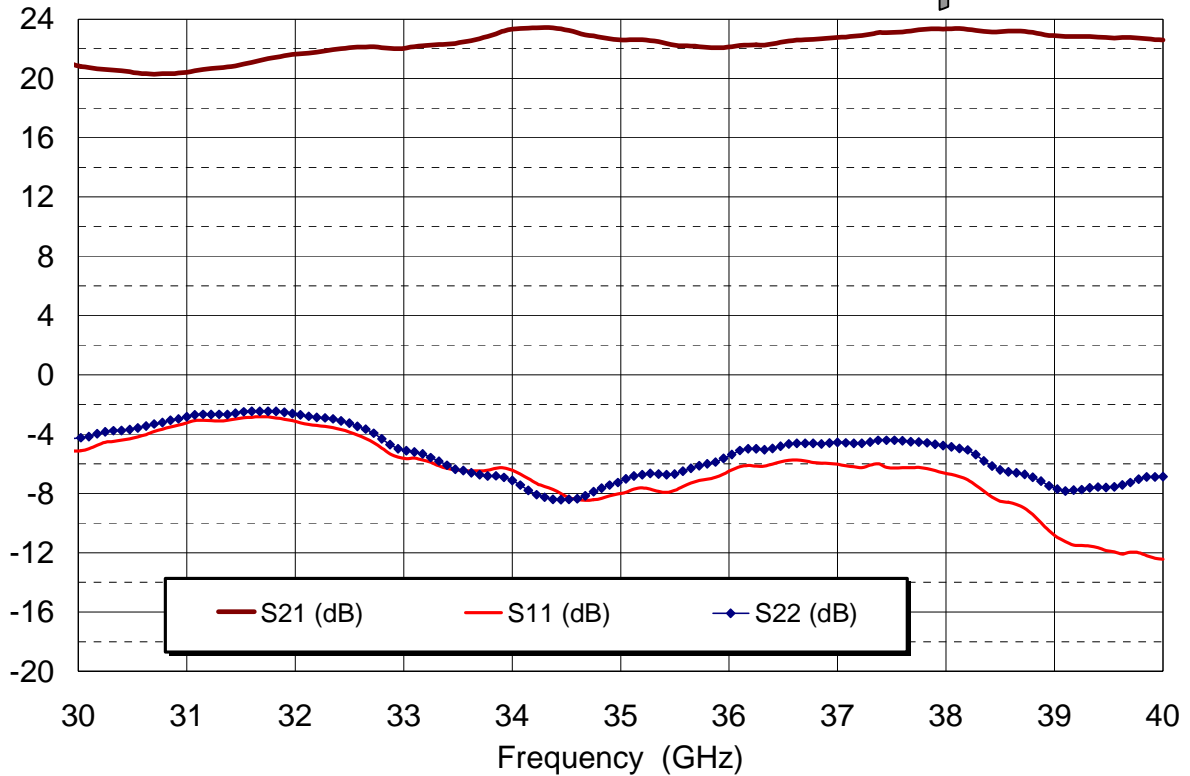
(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s.

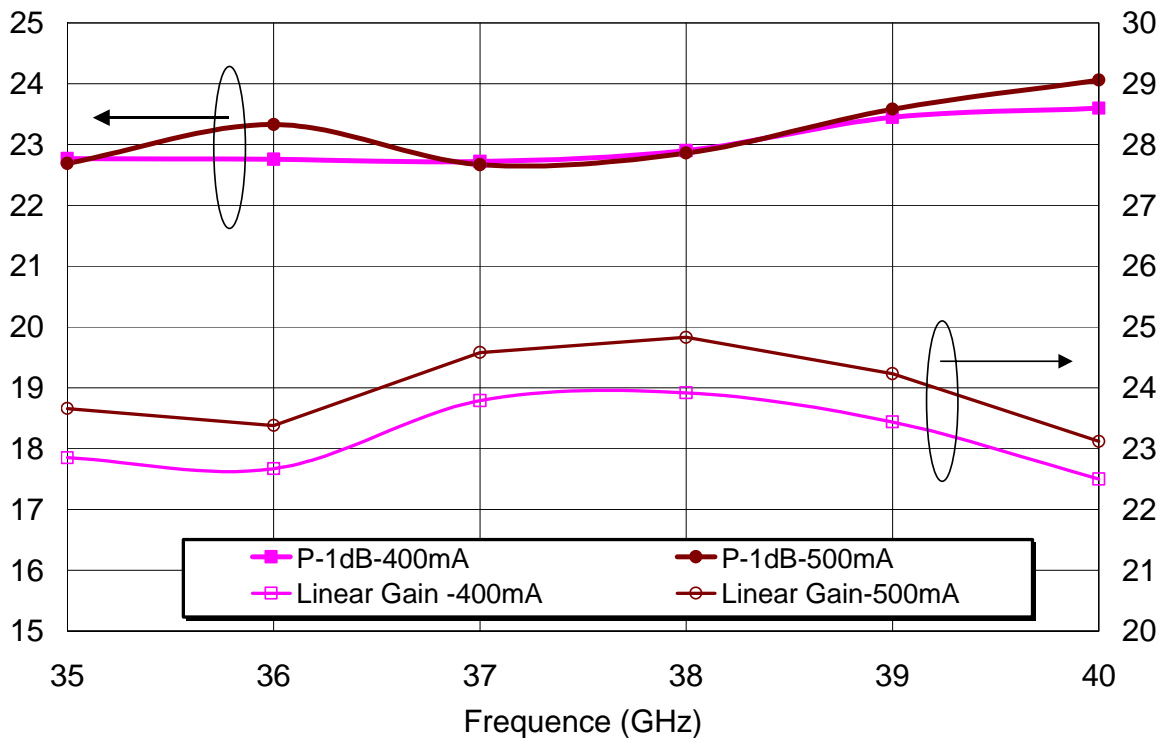
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Typical on Jig Measurements

Bias conditions: $V_d=3.5V$, V_g tuned for $I_d = 500mA$

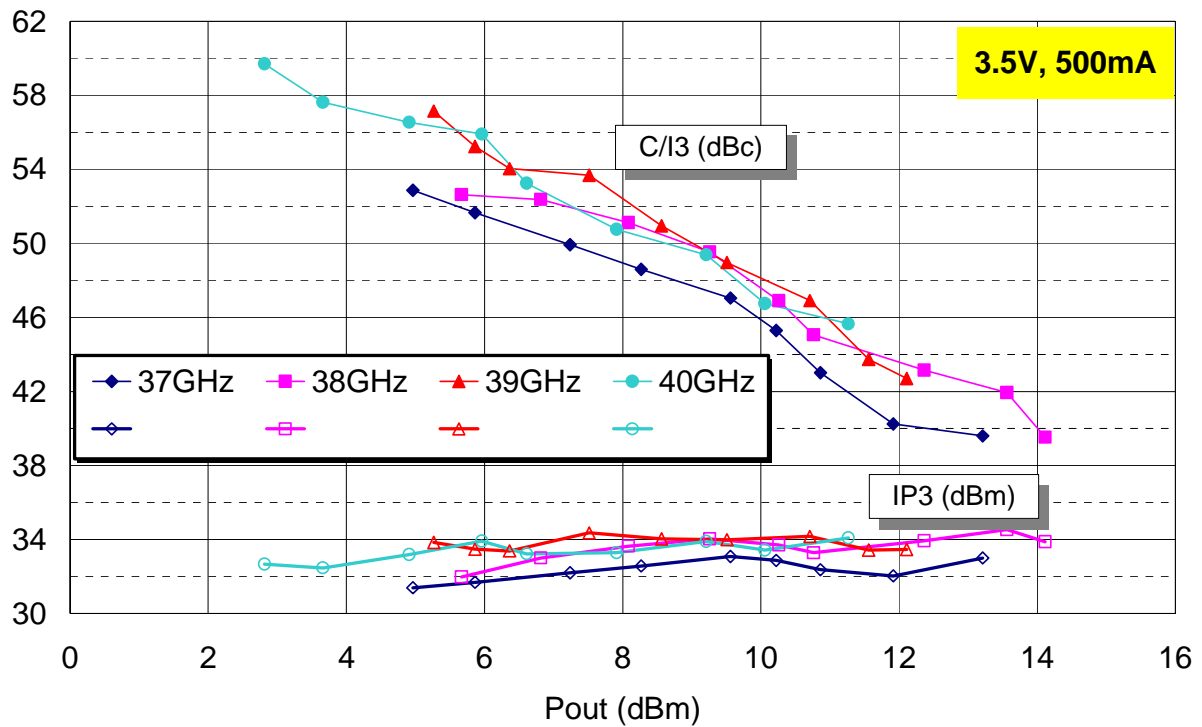
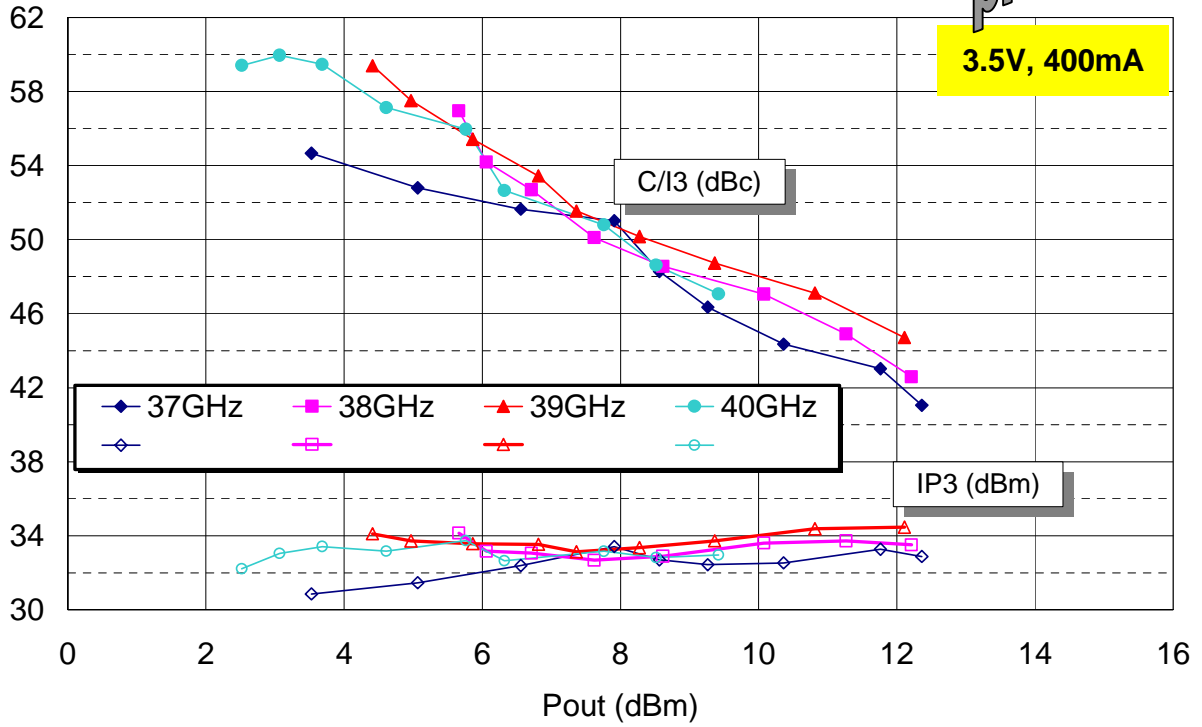


Linear Gain & Return Losses versus frequency (including 1dB losses)



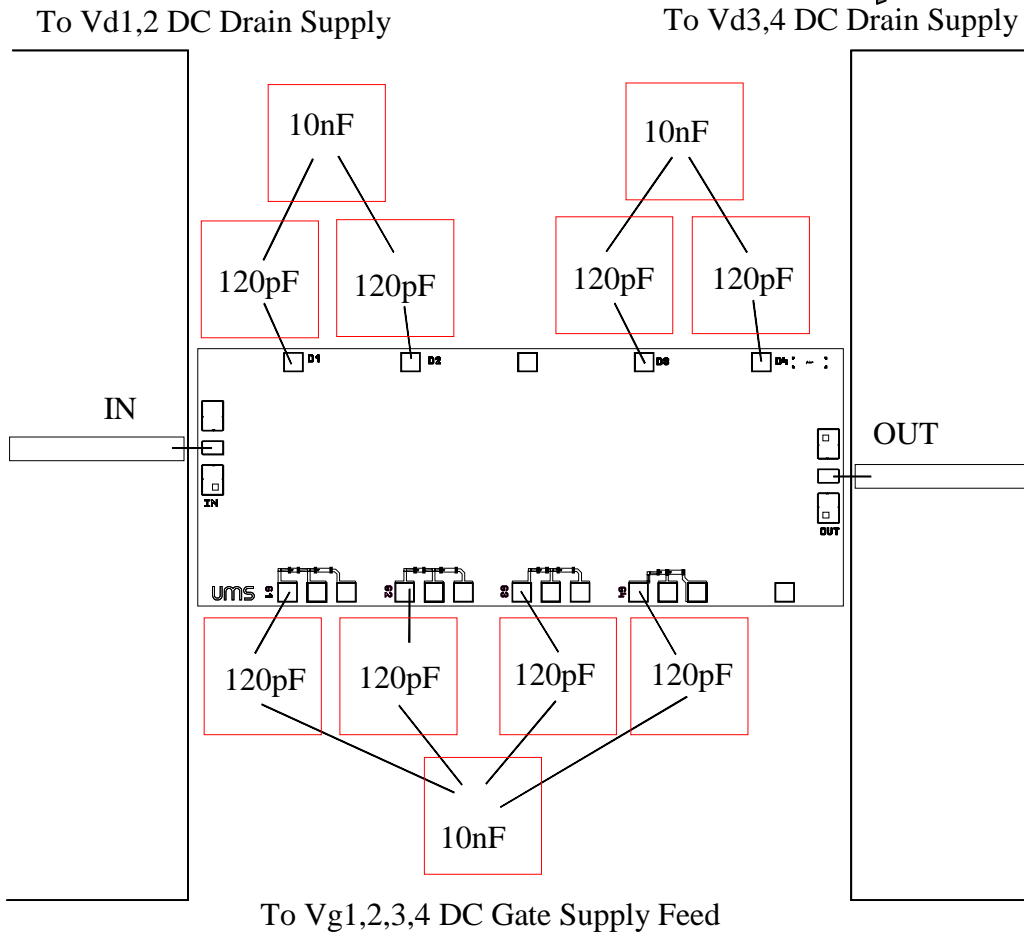
Linear Gain & Output power at 1dB compression versus frequency

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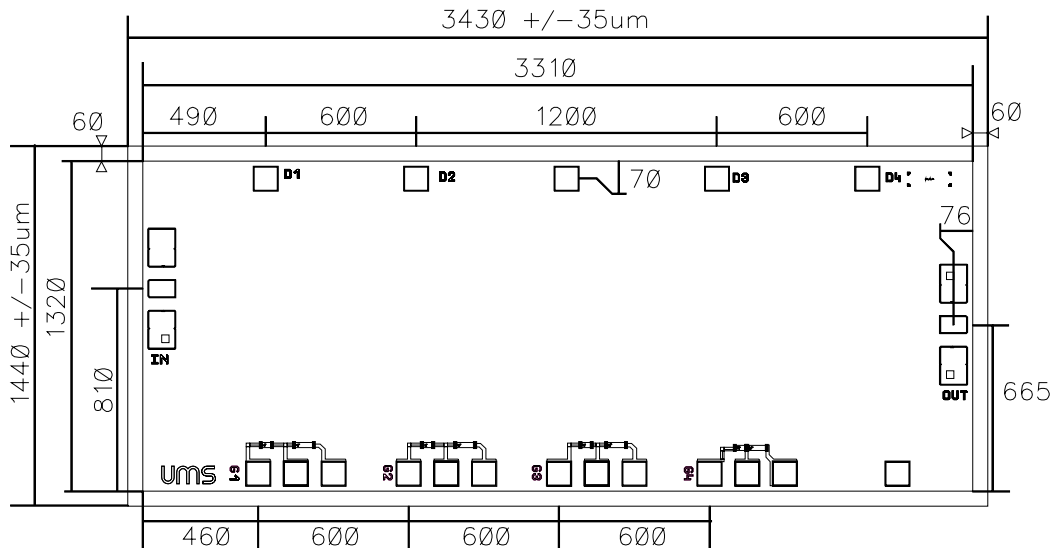


C/I3 versus total output power ($\Delta F = 10\text{MHz}$)

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.



Bonding pad positions.
(Chip thickness : 70µm. All dimensions are in micrometers)

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Application note

Bias operation sequence:

ON: Supply Gate voltage
Supply Drain voltage
OFF: Cut off Drain voltage
Cut off Gate voltage

Due to 70 μ m thickness, specific care is requested for the handling and assembly.

Ordering Information

Chip form : CHA5292a-99F/00

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