# 256MB – 32M x 72 DDR2 SDRAM 208 PBGA Multi-Chip Package

## FEATURES

- Data rate = 667, 533, 400
- Package:
  - 208 Plastic Ball Grid Array (PBGA), 16 x 20mm
  - 1.0mm pitch
- Differential data strobe (DQS, DQS#) per byte
- Internal, pipelined, double data rate architecture
- 4-bit prefetch architecture
- DLL for alignment of DQ and DQS transitions with clock signal
- Four internal banks for concurrent operation (Per DDR2 SDRAM Die)
- Programmable Burst lengths:  4 or 8
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT)
- Adjustable data – output drive strength
- Single 1.8V ±0.1V supply
- Programmable CAS latency:  3, 4, 5, or 6
- Posted CAS additive latency:  0, 1, 2, 3 or 4
- Write latency = Read latency - 1* $t_{CK}$
- Commercial, Industrial and Military Temperature Ranges
- Organized as 32M x 72
- Weight:  W3H32M72E-XSB2X - 2.5 grams typical

## BENEFITS

- 69% space savings vs. FPBGA
- Reduced part count
- 54% I/O reduction vs FPBGA
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Upgradable to 64M x 72 density (contact factory for information)
- Lead free - available (Pb free – component and material are lead free in accordance with IPC-1752)

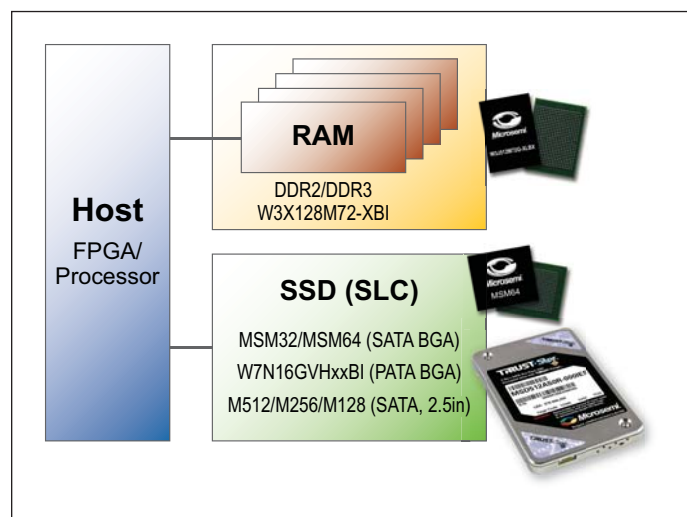\* This product is subject to change without notice.

## TYPICAL APPLICATION



## FIGURE 1 – DENSITY COMPARISONS
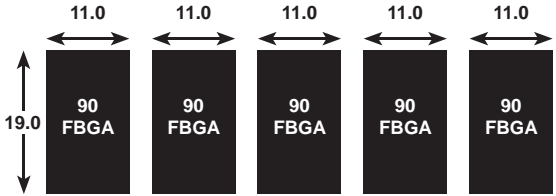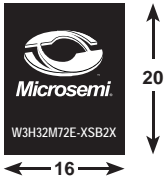


| | CSP Approach (mm) | W3H32M72E-XSB2X | S A V I N G S |
|---|---|---|---|
| **Area** | 5 x 209mm² = 1,045mm² | 320mm² | 69% |
| **I/O Count** | 5 x 90 balls = 450 balls | 208 Balls | 54% |

## FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM



Note: UDQS4 and UDQS4# require a 10 KΩ pull up resistor.
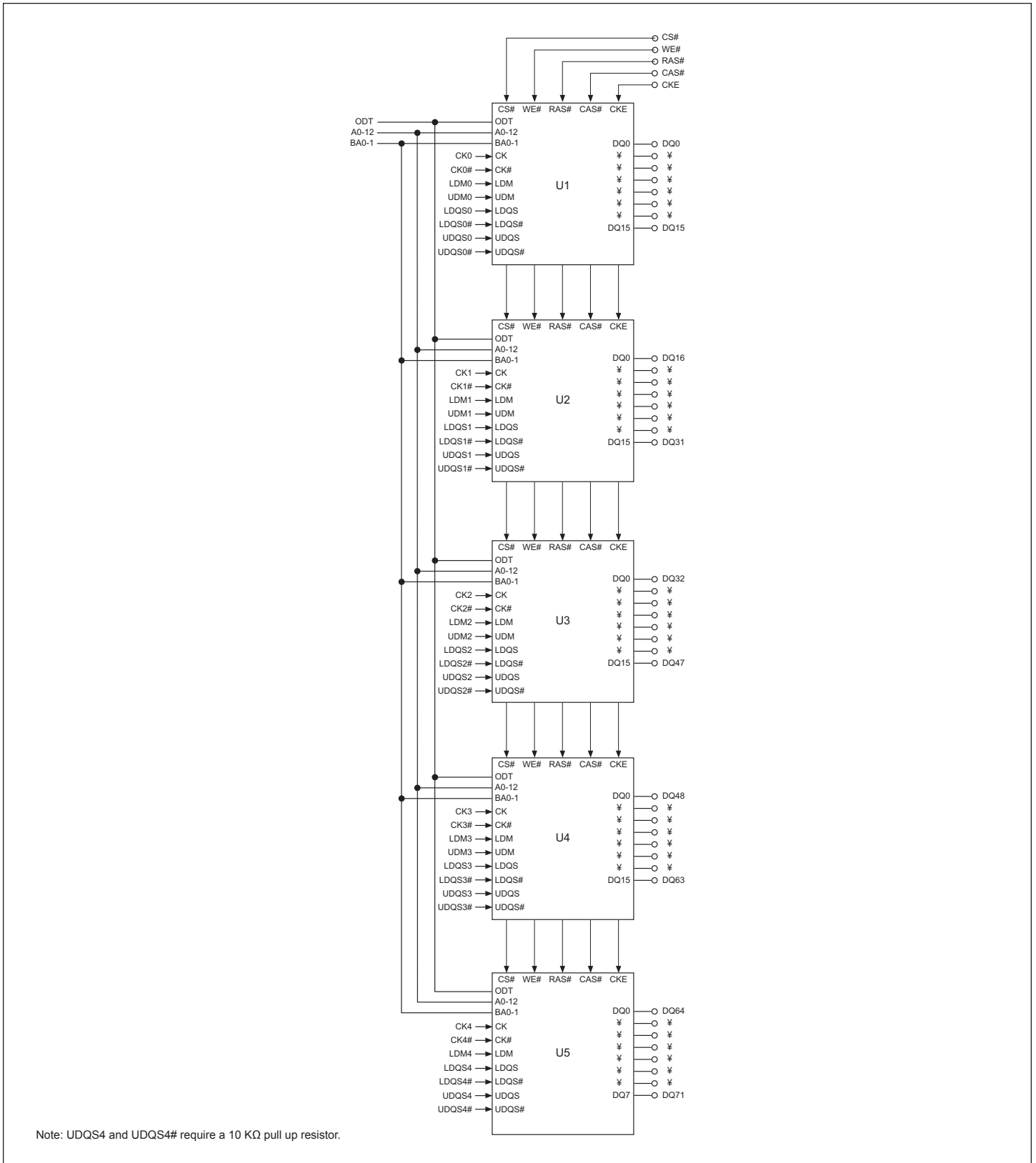
## FIGURE 3 – PIN CONFIGURATION

**TOP VIEW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | Vcc | Vss | Vcc | Vcc | Vss | Vcc | Vcc | Vss | Vcc | Vss | A |
| B | Vcc | Vss | NC | NC | NC | NC | NC | NC | NC | Vss | Vcc | B |
| C | Vss | NC | NC | NC | NC | NC | NC | DQ34 | CK3 | CK3# | Vss | C |
| D | DQ35 | DQ51 | NC | NC | NC | NC | DQ50 | DQ53 | DQ37 | CK2# | CK2 | D |
| E | DQ52 | DQ36 | DQ33 | NC | DNU** | DNU | DQ39 | LDQS2 | LDQS3 | DQ48 | DQ32 | E |
| F | LDM3 | LDM2 | DQ49 | DQ43 | DQ59 | DNU | DQ55 | DQ58 | DQ42 | LDQS2# | LDQS3# | F |
| G | DQ38 | DQ54 | DQ60 | DQ57 | UDM2 | Vss | DQ63 | DQ56 | DQ40 | DQ61 | DQ45 | G |
| H | UDM3 | DQ44 | DQ41 | DQ46 | DQ62 | Vcc | UDQS2# | DQ47 | UDQS2 | UDQS3 | UDQS3# | H |
| J | Vcc | A6 | A10 | A9 | Vcc | Vss | Vcc | A3 | A12 | DNU* | Vcc | J |
| K | Vss | A0 | A11 | Vcc | Vss | VREF | Vss | Vcc | A1 | BA1 | Vss | K |
| L | Vcc | A2 | A4 | A8 | Vcc | Vss | Vcc | BA0 | A5 | A7 | Vcc | L |
| M | UDQS1# | UDQS1 | UDQS0 | DQ15 | UDQS0# | Vcc | DQ30 | DQ14 | DQ9 | DQ12 | UDM1 | M |
| N | DQ13 | DQ29 | DQ8 | DQ24 | DQ31 | Vss | UDM0 | DQ25 | DQ28 | DQ22 | DQ6 | N |
| P | LDQS1# | LDQS0# | DQ10 | DQ26 | DQ23 | ODT | DQ27 | DQ11 | DQ17 | LDM0 | LDM1 | P |
| R | DQ0 | DQ16 | LDQS1 | LDQS0 | DQ7 | LDQS4# | UDQS4 | UDQS4# | DQ1 | DQ4 | DQ20 | R |
| T | CK0 | CK0# | DQ5 | DQ21 | DQ18 | LDQS4 | DQ71 | CKE | WE# | DQ19 | DQ3 | T |
| U | Vss | CK1# | CK1 | DQ2 | RAS# | CAS# | DQ64 | DQ70 | DQ65 | DQ68 | Vss | U |
| V | Vcc | Vss | CK4# | CK4 | CS# | DQ66 | DQ69 | LDM4 | DQ67 | Vss | Vcc | V |
| W | Vss | Vcc | Vss | Vcc | Vcc | Vss | Vcc | Vcc | Vss | Vcc | Vss | W |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

\* Pin J10 is reserved for signal A13 on 128Mx72 and higher densities.
\*\* Pin E5 is reserved for signal BA2 on 64Mx72 and higher densities.
Note:  UDQS4 and UDQS4# require a 10 KΩ pull up resistor.

## TABLE 1 – BALL DESCRIPTIONS

| Symbol | Type | Description |
|---|---|---|
| ODT | Input | On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ71, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS#. The ODT input will be ignored if disabled via the LOAD MODE command. |
| CK, CK# | Input | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQS and DQS/DQS#) is referenced to the crossings of CK and CK#. |
| CKE | Input | Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down mode and SELF-REFRESH action (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for power-down entry, Power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMO SLOW level once $V_{CC}$ is applied during first power-up. After $V_{REF}$ has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, $V_{REF}$ must be maintained. |
| CS# | Input | Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. |
| RAS#, CAS#, WE# | Input | Command inputs: RAS#, CAS#, WE# (along with CS#) define the command being entered. |
| LDM, UDM | Input | Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15, of each of U0-U4 |
| BA0–BA1 | Input | Bank address inputs: BA0–BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command. |
| A0-A12 | Input | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA1–BA0) or all banks (A10 HIGH) The address inputs also provide the op-code during a LOAD MODE command. |
| DQ0-71 | I/O | Data input/output: Bidirectional data bus |
| UDQS, UDQS# | I/O | Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |
| LDQS, LDQS# | I/O | Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |
| $V_{CC}$ | Supply | Power Supply: 1.8V ±0.1V |
| $V_{CCQ}$ | Supply | DQ Power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity |
| $V_{REF}$ | Supply | SSTL_18 reference voltage. |
| $V_{SS}$ | Supply | Ground |
| NC | - | No connect: These balls should be left unconnected. |
| DNU | - | Future use; Row address bits A14 and A15 are reserved for 8Gb and 16Gb densities. BA2 is reserved for 4Gb device. |

## DESCRIPTION

The 2Gb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. Each of the five chips in the MCP are internally configured as 4-bank DRAM. The block diagram of the device is shown in Figure 2. Ball assignments and are shown in Figure 3.

The 2Gb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 2Gb DDR2 SDRAM effectively consists of a single $4n$-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding $n$-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. There are strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 2Gb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

## GENERAL NOTES

The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.

Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, each chip is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS. Note that the there is no upper byte for U4 and therefore no UDM4.

Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

## INITIALIZATION

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for power up and initialization and is shown in Figure 4 on page 8.

1. Applying power; if CKE is maintained below 0.2 x $V_{CCQ}$, outputs remain disabled. To guarantee $R_{TT}$ (ODT resistance) is off, $V_{REF}$ must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than $V_{CCQ}$ during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as $V_{CC}$, $V_{CCQ}$, $V_{REF}$, and $V_{TT}$ are between their minimum and maximum values as stated in Table 20):

A. (single power source) The $V_{CC}$ voltage ramp from 300mV to $V_{CC}$ (MIN) must take no longer than 200ms; during the $V_{CC}$ voltage ramp, $|V_{CC} - V_{CCQ}| \leq 0.3V$. Once supply voltage ramping is complete (when $V_{CCQ}$ crosses $V_{CC}$ (MIN)), Table20 specifications apply.

   • $V_{CC}$, $V_{CCQ}$ are driven from a single power converter output

   • $V_{TT}$ is limited to 0.95V MAX

   • $V_{REF}$ tracks $V_{CCQ/2}$; $V_{REF}$ must be within ±0.3V with respect to $V_{CCQ/2}$ during supply ramp time

   • $V_{CCQ} \geq V_{REF}$ at all times

B. (multiple power sources) $V_{CC} \geq V_{CCQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes ($V_{CCQ}$ crosses $V_{CC}$ [MIN]). Once supply voltage ramping is complete, Table20 specifications apply.

   • Apply $V_{CC}$ before or at the same time as $V_{CCQ}$; $V_{CC}$ voltage ramp time must be ≤ 200ms from when $V_{CC}$ ramps from 300mV to $V_{CC}$ (MIN)

   • Apply $V_{CCQ}$ before or at the same time as $V_{TT}$; the $V_{CCQ}$ voltage ramp time from when $V_{CC}$ (MIN) is achieved to when $V_{CCQ}$ (MIN) is achieved must be ≤ 500ms; while $V_{CC}$ is ramping, current can be supplied from $V_{CC}$ through the device to $V_{CCQ}$

- $V_{REF}$ must track $V_{CCQ/2}$, $V_{REF}$ must be within ±0.3V with respect to $V_{CCQ/2}$ during supply ramp time; $V_{CCQ}$ ≥ $V_{REF}$ must be met at all times

- Apply $V_{TT}$; The $V_{TT}$ voltage ramp time from when $V_{CCQ}$ (MIN) is achieved to when $V_{TT}$ (MIN) is achieved must be no greater than 500ms

2. For a minimum of 200µs after stable power nd clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.

3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.

4. Issue an LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)

5. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)

6. Issue an LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1"; Micron recommends setting them to "0."

7. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1, and BA0.) CKE must be HIGH the entire time.

8. Issue PRECHARGE ALL command.

9. Issue two or more REFRESH commands, followed by a dummy WRITE.

10. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).

11. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters.

12. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters.

13. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).

14. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7,E8, and E9 to "1," and then setting all other desired parameters.

15. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters.

The DDR2 SDRAM is now initialized and ready for normal operation 200 clocks after DLL RESET (in step 7).

## FIGURE 4 – POWER-UP AND INITIALIZATION

Notes appear on page 7
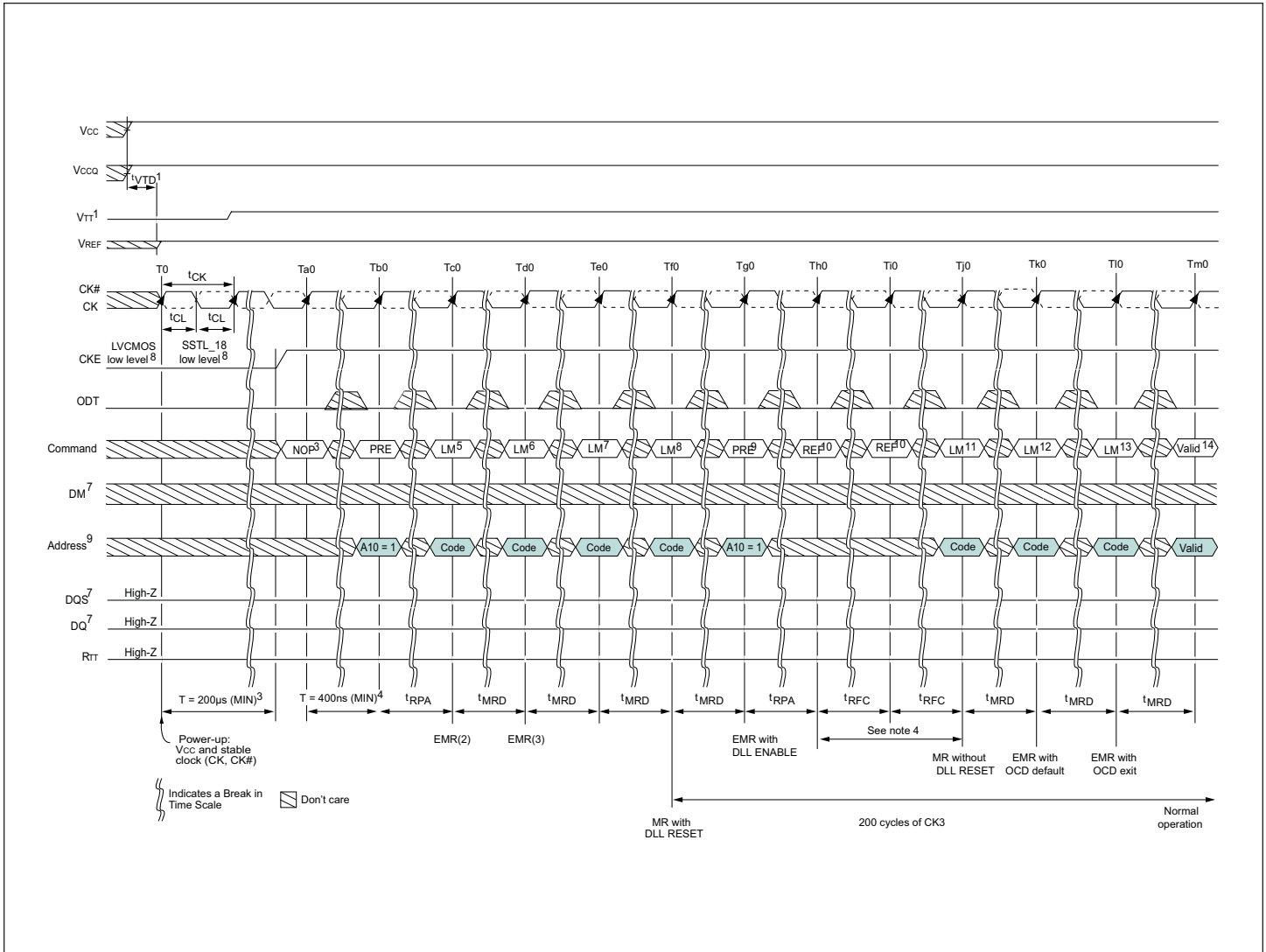
## MODE REGISTER (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CL, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 5. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the command is issued.

The mode register is programmed via the LM command (bits BA1–BA0 = 0, 0) and other bits (M12–M0) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time $t_{MRD}$ before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

## BURST LENGTH

Burst length is defined by bits M0–M3, as shown in Figure 5. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–Ai when BL = 4 and by A3–Ai when BL = 8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

## BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 2. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

## OPERATING MODE

The normal operating mode is selected by issuing a command with bit M7 set to "0," and all other bits set to the desired values, as shown in Figure 5. When bit M7 is "1," no other bits of the mode register are programmed. Programming bit M7 to "1" places the DDR2 SDRAM into a test mode that is only used by the

### FIGURE 5 – MODE REGISTER (MR) DEFINITION



Note: 1. Not used on this part
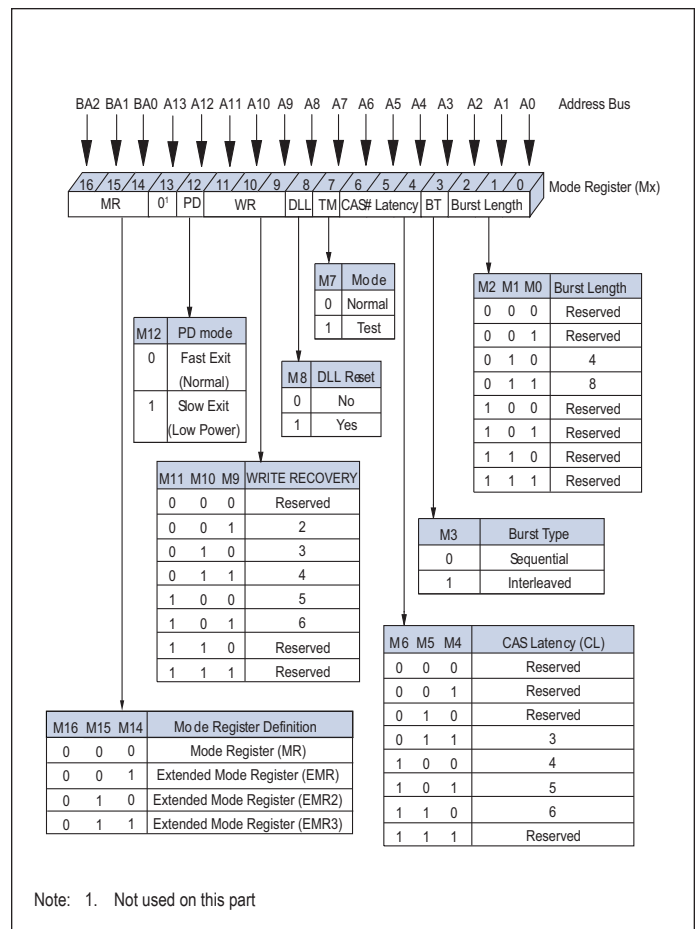
manufacturer and should not be used. No operation or functionality is guaranteed if M7 bit is '1.'

## DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 5. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of "0" after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the $t_{AC}$ or $t_{DQSCK}$ parameters.

## WRITE RECOVERY

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 5. The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst.

## TABLE 2 – BURST DEFINITION

| Burst Length | Starting Column Address | | | Order of Accesses Within a Burst | |
|---|---|---|---|---|---|
| | | | | Type = Sequential | Type = Interleaved |
| | | A1 | A0 | | |
| 4 | | 0 | 0 | 0-1-2-3 | 0-1-2-3 |
| | | 0 | 1 | 1-2-3-0 | 1-0-3-2 |
| | | 1 | 0 | 2-3-0-1 | 2-3-0-1 |
| | | 1 | 1 | 3-0-1-2 | 3-2-1-0 |
| | A2 | A1 | A0 | | |
| 8 | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |

NOTES:
1. For a burst length of two, A1-Ai select two-data-element block; A0 selects the starting column within the block.
2. For a burst length of four, A2-Ai select four-data-element block; A0-1 select the starting column within the block.
3. For a burst length of eight, A3-Ai select eight-data-element block; A0-2 select the starting column within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

WR values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing $t_{WR}$ (in ns) by $t_{CK}$ (in ns) and rounding up a non integer value to the next integer; WR [cycles] = $t_{WR}$ [ns] / $t_{CK}$ [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## POWER-DOWN MODE

Active power-down (PD) mode is defined by bit M12, as shown in Figure 5. PD mode allows the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode or "fast-exit" active PD mode is enabled. The $t_{XARD}$ parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode or "slow-exit" active PD mode is enabled. The $t_{XARD}$ parameter is used for slow-exit active PD exit timing. The DLL can be enabled, but "frozen" during active PD mode since the exit-to-READ command timing is relaxed. The power difference expected between PD normal and PD low-power mode is defined in the $I_{CC}$ table.

## CAS LATENCY (CL)

The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 5. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, or 6 clocks, depending on the speed grade option being used.

## FIGURE 6 – CAS LATENCY (CL)
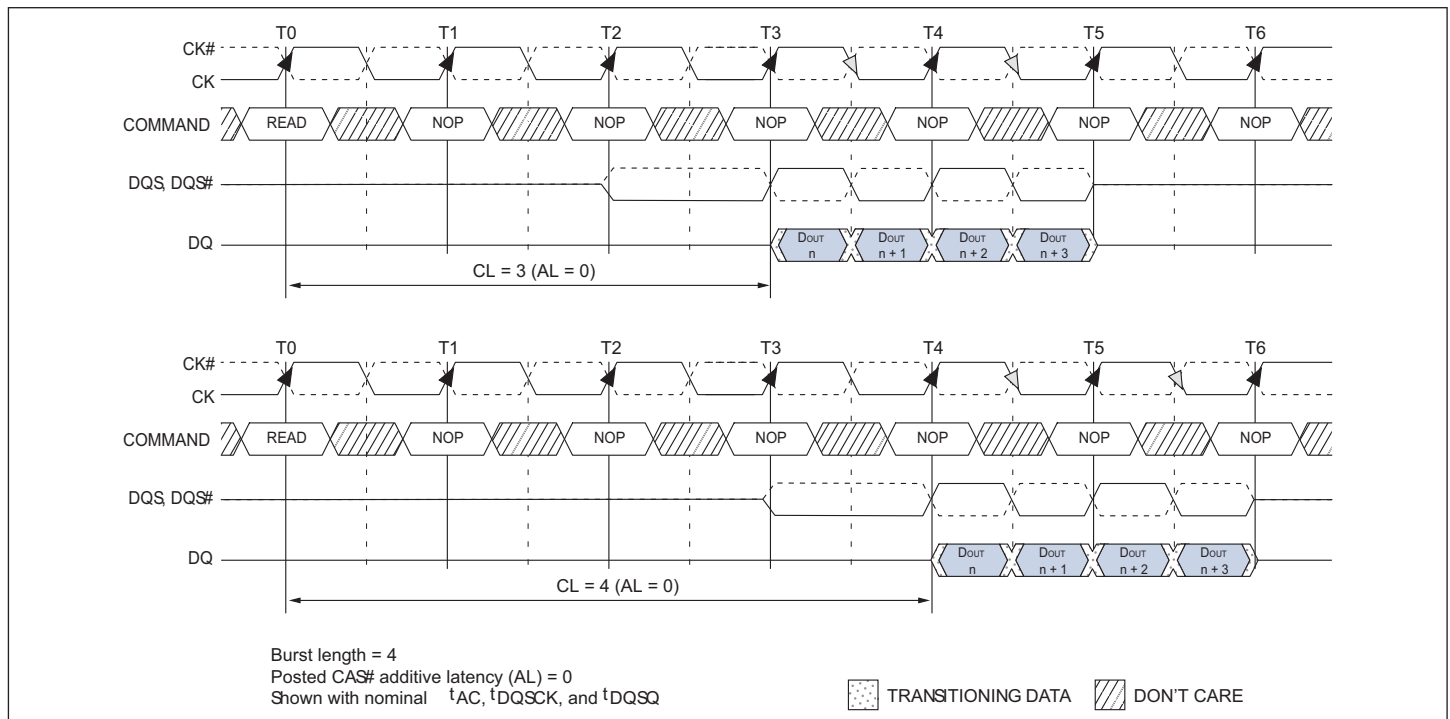
DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.
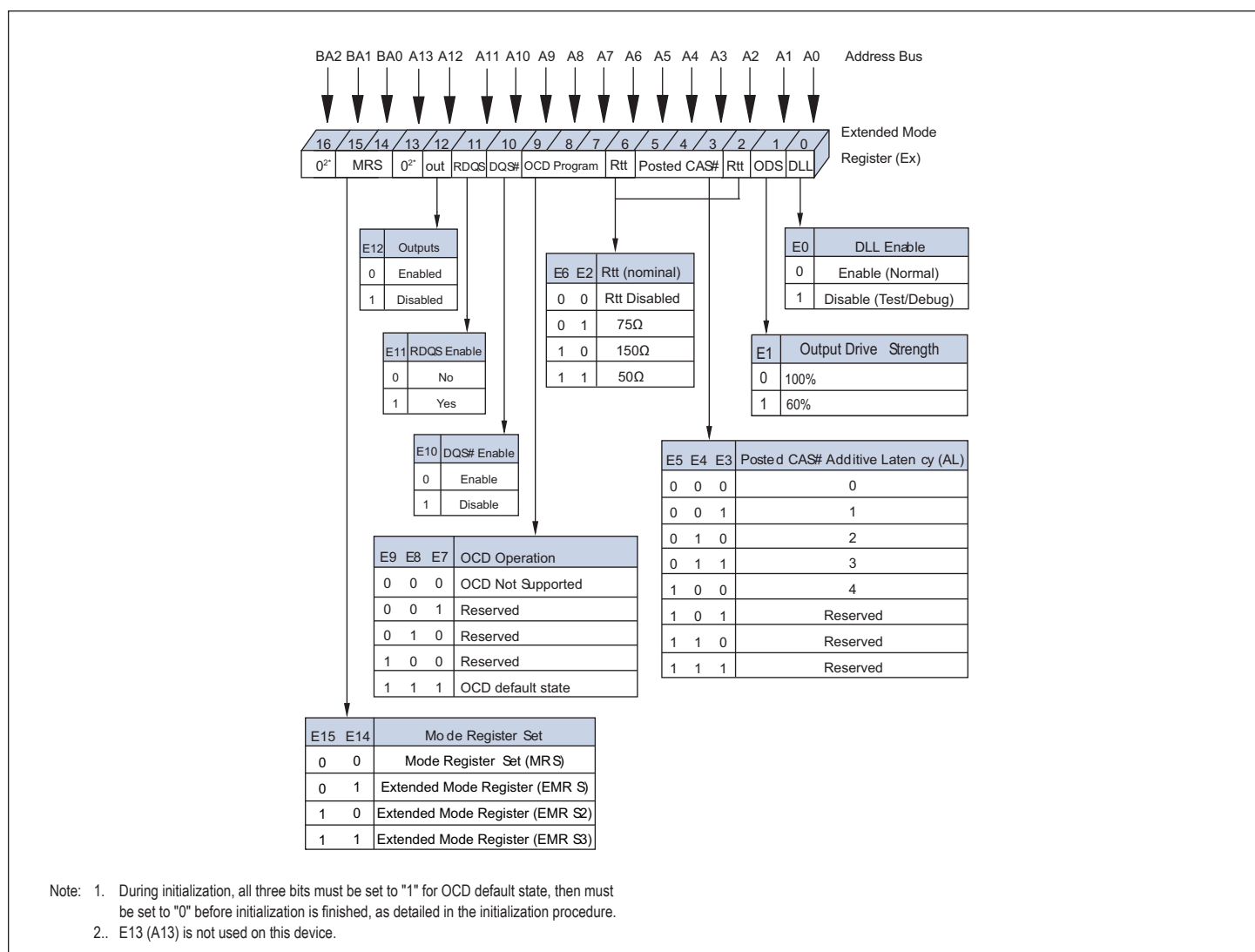
DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to $t_{RCD}$ (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks.

Examples of CL = 3 and CL = 4 are shown in Figure 6; both assume AL = 0. If a READ command is registered at clock edge $n$, and the CL is $m$ clocks, the data will be available nominally coincident with clock edge $n+m$ (this assumes AL = 0).

## EXTENDED MODE REGISTER (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on die termination (ODT) (RTT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 7. The EMR is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

### FIGURE 7 – EXTENDED MODE REGISTER DEFINITION



| E12 | Outputs |
|---|---|
| 0 | Enabled |
| 1 | Disabled |

| E6 | E2 | Rtt (nominal) |
|---|---|---|
| 0 | 0 | Rtt Disabled |
| 0 | 1 | 75Ω |
| 1 | 0 | 150Ω |
| 1 | 1 | 50Ω |

| E0 | DLL Enable |
|---|---|
| 0 | Enable (Normal) |
| 1 | Disable (Test/Debug) |

| E11 | RDQS Enable |
|---|---|
| 0 | No |
| 1 | Yes |

| E1 | Output Drive Strength |
|---|---|
| 0 | 100% |
| 1 | 60% |

| E10 | DQS# Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| E5 | E4 | E3 | Posted CAS# Additive Latency (AL) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| E9 | E8 | E7 | OCD Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD Not Supported |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 1 | 1 | OCD default state |

| E15 | E14 | Mode Register Set |
|---|---|---|
| 0 | 0 | Mode Register Set (MRS) |
| 0 | 1 | Extended Mode Register (EMR S) |
| 1 | 0 | Extended Mode Register (EMR S2) |
| 1 | 1 | Extended Mode Register (EMR S3) |

Note: 1. During initialization, all three bits must be set to "1" for OCD default state, then must be set to "0" before initialization is finished, as detailed in the initialization procedure.
2. E13 (A13) is not used on this device.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time $t_{MRD}$ before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

## DLL ENABLE/DISABLE

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 7. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using an LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued, to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the $t_{AC}$ or $t_{DQSCK}$ parameters.

## OUTPUT DRIVE STRENGTH

The output drive strength is defined by bit E1, as shown in Figure 7. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

## DQS# ENABLE/DISABLE

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#.

When disabled (E10 = 1), DQS is used in a single ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.
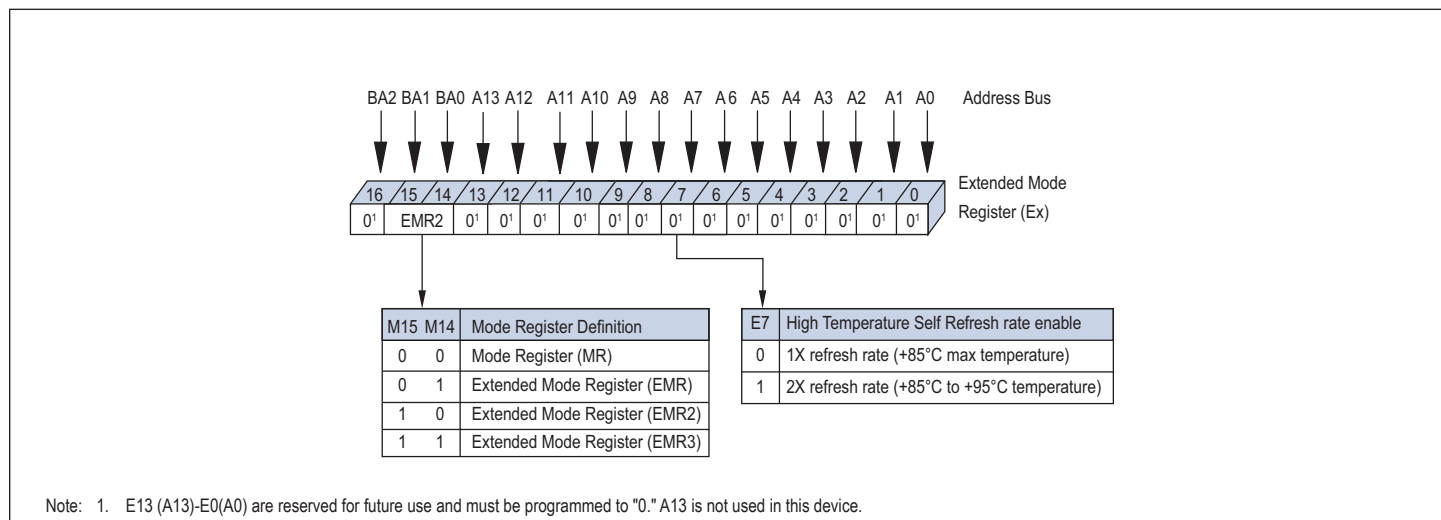
## OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 7. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during $I_{CC}$ characterization of read current.

## ON-DIE TERMINATION (ODT)

ODT effective resistance, $R_{TT}$ (EFF), is defined by bits E2 and E6 of the EMR, as shown in Figure 7. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. $R_{TT}$ effective resistance values of 50Ω ,75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off "sw1," "sw2," or "sw3." The ODT effective resistance value is elected by enabling switch "sw1," which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω ($R_{TT2}$(EFF) = R2/2). Similarly, if "sw2" is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω ($R_{TT2}$(EFF) = R2/2). Switch "sw3" enables R1 values of 100Ω enabling effective resistance of 50Ω Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when $R_{TT}$(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of

### FIGURE 8 – EXTENDED MODE REGISTER 2 (EMR2) DEFINITION



| M15 | M14 | Mode Register Definition |
|-----|-----|--------------------------|
| 0 | 0 | Mode Register (MR) |
| 0 | 1 | Extended Mode Register (EMR) |
| 1 | 0 | Extended Mode Register (EMR2) |
| 1 | 1 | Extended Mode Register (EMR3) |

| E7 | High Temperature Self Refresh rate enable |
|----|-------------------------------------------|
| 0 | 1X refresh rate (+85°C max temperature) |
| 1 | 2X refresh rate (+85°C to +95°C temperature) |

Note: 1. E13 (A13)-E0(A0) are reserved for future use and must be programmed to "0." A13 is not used in this device.

the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. ODT must be turned off prior to entering self refresh. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until issuing the EMR command to enable the ODT feature, at which point the ODT ball will determine the $R_{TT}(EFF)$ value. Any time the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled. See "ODT Timing" section for ODT timing diagrams.

## POSTED CAS ADDITIVE LATENCY (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 7. Bits E3–E5 allow the user to program the DDR2 SDRAM with an inverse AL of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to $t_{RCD}$ (MIN) with the requirement that AL ≤ $t_{RCD}$ (MIN). A typical application using this feature would set AL = $t_{RCD}$ (MIN) - 1x $t_{CK}$. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL+CL. Write latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 x $t_{CK}$.

## EXTENDED MODE REGISTER 2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register (shown in Figure 8). The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time $t_{MRD}$ before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

## EXTENDED MODE REGISTER 3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently, all bits in EMR3 are reserved, as shown in Figure 9. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time $t_{MRD}$ before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

## COMMAND TRUTH TABLES

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.

## DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected.

**FIGURE 9 – EXTENDED MODE REGISTER 3 (EMR3) DEFINITION**



| M15 | M14 | Mode Register Definition |
|-----|-----|--------------------------|
| 0 | 0 | Mode Register (MR) |
| 0 | 1 | Extended Mode Register (EMR) |
| 1 | 0 | Extended Mode Register (EMR2) |
| 1 | 1 | Extended Mode Register (EMR3) |

Note: 1. E13 (A13)-E0 (A0) are reserved for future use and must be programmed to "0." A13 is not used in this device.
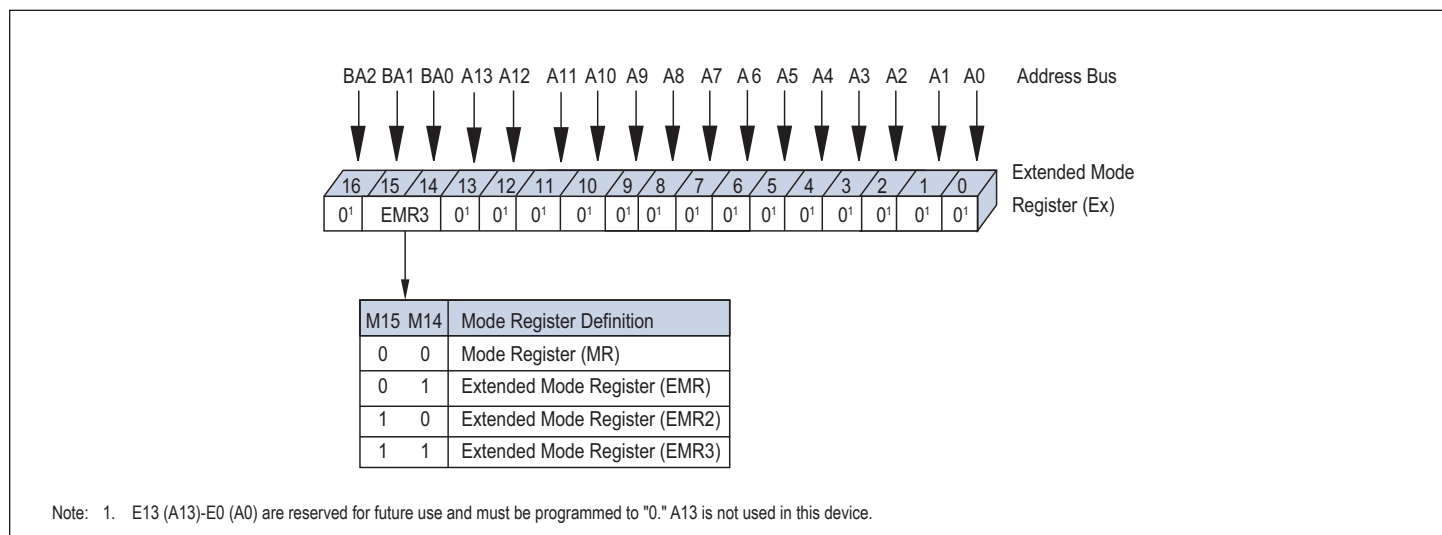
**TABLE 3 – TRUTH TABLE - DDR2 COMMANDS**

| Function | CKE | | CS# | RAS# | CAS# | WE# | BA1 BA0 | A12 A11 | A10 | A9-A0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| LOAD MODE | H | H | L | L | L | L | BA | OP Code | | | 2 |
| REFRESH | H | H | L | L | L | H | X | X | X | X | |
| SELF-REFRESH Entry | H | L | L | L | L | H | X | X | X | X | |
| SELF-REFRESH Exit | L | H | H | X | X | X | X | X | X | X | 7 |
| | | | L | H | H | H | | | | | |
| Single bank precharge | H | H | L | L | H | L | X | X | L | X | 2 |
| All banks PRECHARGE | H | H | L | L | H | L | X | X | H | X | |
| Bank activate | H | H | L | L | H | L | BA | Row Address | | | |
| WRITE | H | H | L | L | H | L | BA | Column Address | L | Column Address | 2, 3 |
| WRITE with auto precharge | H | H | L | H | L | L | BA | Column Address | H | Column Address | 2, 3 |
| READ | H | H | L | H | L | H | BA | Column Address | L | Column Address | 2, 3 |
| READ with auto precharge | H | H | L | H | L | H | BA | Column Address | H | Column Address | 2, 3 |
| NO OPERATION | H | X | L | H | H | H | X | X | X | X | |
| Device DESELECT | H | X | H | X | X | X | X | X | X | X | |
| POWER-DOWN entry | H | L | H | X | X | X | X | X | X | X | 4 |
| | | | L | H | H | H | | | | | |
| POWER-DOWN exit | L | H | H | X | X | X | X | X | X | X | 4 |
| | | | L | H | H | H | | | | | |

Note: 1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.

2. Bank addresses (BA) BA0–BA12 determine which bank is to be operated upon. BA during a LM command selects which mode register is programmed.

3. 3. Burst reads or writes at BL = 4 cannot be terminated or interrupted.

4. The power-down mode does not perform any REFRESH operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.

5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See "On-Die Termination (ODT)" for details.

6. "X" means "H or L" (but a defined logic level).

7. Self refresh exit is asynchronous.

## NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

## LOAD MODE (LM)

The mode registers are loaded via inputs BA1–BA0, and A12–A0. BA1–BA0 determine which mode register will be programmed. See "Mode Register (MR)". The LM command can only be issued when all banks are idle, and a subsequent execute able command cannot be issued until $t_{MRD}$ is met.

## BANK/ROW ACTIVATION

### ACTIVE COMMAND

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A12–A0 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

### ACTIVE OPERATION

Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be

opened (activated), even when additive latency is used. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the $t_{RCD}$ specification. $t_{RCD}$ (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a $t_{RCD}$ (MIN) specification of 20ns with a 266 MHz clock ($t_{CK}$ = 3.75ns) results in 5.3 clocks, rounded up to 6.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by $t_{RC}$.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by $t_{RRD}$

## READ COMMAND

The READ command is used to initiate a burst read access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–i (where i = A9) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end

of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

## READ OPERATION

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL; RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#).

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the read preamble ($t_{RPRE}$). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble ($t_{RPST}$).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z.
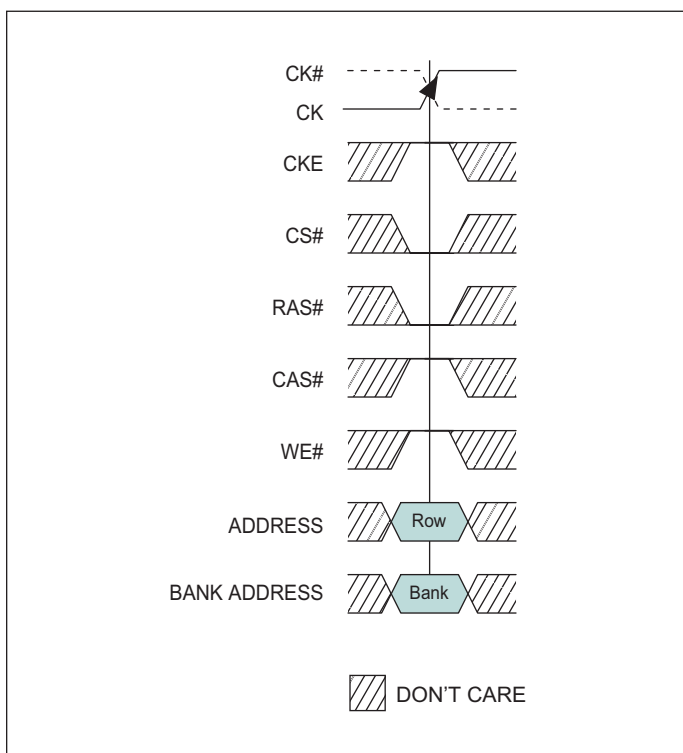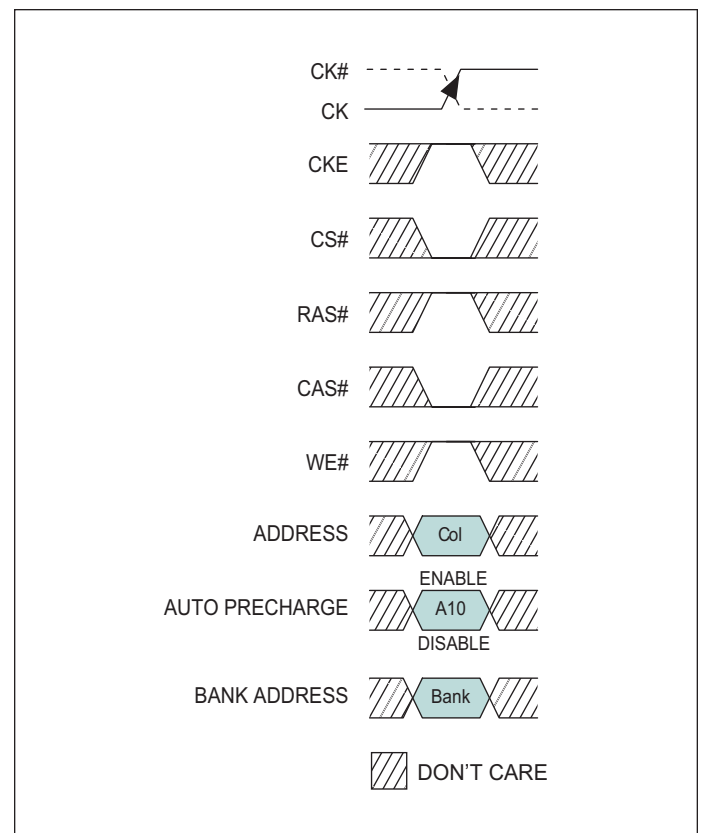
### FIGURE 10 – ACTIVE COMMAND



### FIGURE 11 – READ COMMAND

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL / 2 cycles.

## WRITE COMMAND

The WRITE command is used to initiate a burst write access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

## WRITE OPERATION

WRITE bursts are initiated with a WRITE command, as shown in Figure 12. DDR2 SDRAM uses WL equal to RL minus one clock cycle [WL = RL - 1CK = AL + (CL - 1CK)]. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is WL $\pm$ $t_{DQSS}$. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as $\pm$ $t_{DQSS}$. $t_{DQSS}$ is specified with a relatively wide range (25 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases ($t_{DQSS}$ [MIN] and $t_{DQSS}$ [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 4.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE (with auto precharge disabled) using BL = 8 operation might be interrupted and truncated ONLY by another WRITE burst as long as the interruption occurs on a 4-bit boundary, due to the 4*n* prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may not to be interrupted or truncated with any command except another WRITE command.

Data for any WRITE burst may be followed by a subsequent READ command. The number of clock cycles required to meet $t_{WTR}$ is either 2 or $t_{WTR}/t_{CK}$, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. $t_{WT}$ starts at the end of the data burst, regardless of the data mask condition.
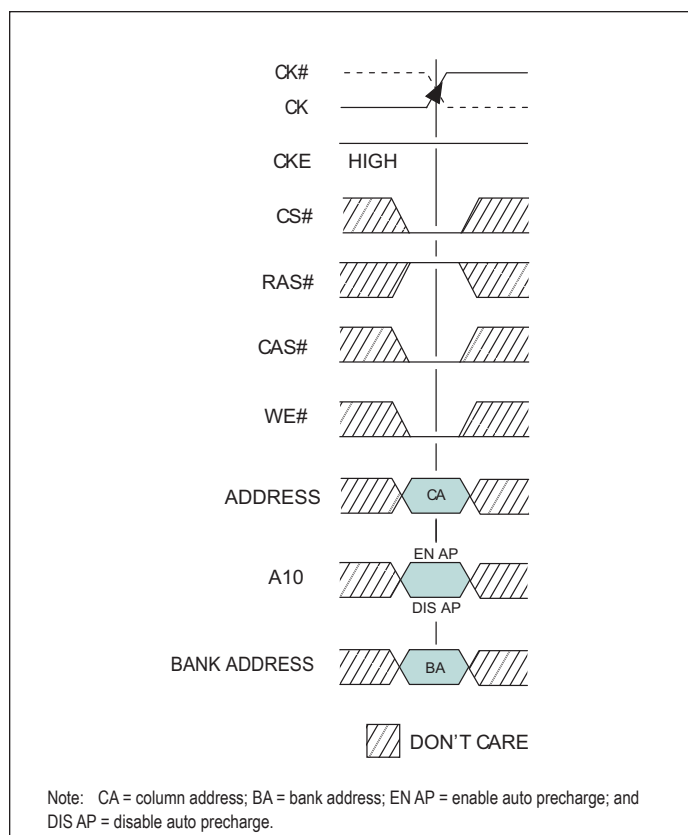
## PRECHARGE COMMAND

The PRECHARGE command, illustrated in Figure 13, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time ($t_{RP}$) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior

### FIGURE 12 – WRITE COMMAND



Note: CA = column address; BA = bank address; EN AP = enable auto precharge; and DIS AP = disable auto precharge.

to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

## PRECHARGE OPERATION

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA1–BA0 select the bank. Otherwise BA1–BA0 are treated as "Don't Care."

When all banks are to be precharged, inputs BA1–BA0 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. $t_{RPA}$ timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, $t_{RP}$ timing applies.

## SELF REFRESH COMMAND

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including $V_{REF}$) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be issued). The differential clock should remain stable and meet $t_{CKE}$ specifications at least 1 x $t_{CK}$ after entering self refresh mode. All command and address input signals except CKE are "Don't Care" during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet $t_{CK}$ specifications at least 1 x $t_{CK}$ prior to CKE going back HIGH. Once CKE is HIGH ($t_{CLE}$(MIN) has been satisfied with four clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for $t_{XSNR}$ because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Note: Self refresh not available at military temperature.

### FIGURE 13 – PRECHARGE COMMAND



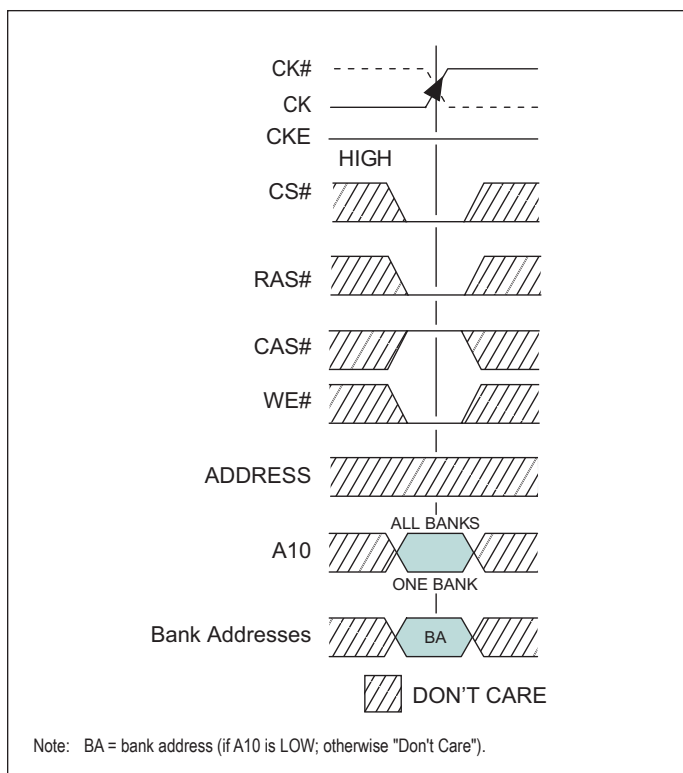Note: BA = bank address (if A10 is LOW; otherwise "Don't Care").

### TABLE 4 – WRITE USING CONCURRENT AUTO PRECHARGE

| From Command (Bank $n$) | To Command (Bank $m$) | Minimum Delay (With Concurrent Auto Precharge) | Units |
|---|---|---|---|
| WRITE with Auto Precharge | READ OR READ w/AP | (CL-1) + (BL/2) + $t_{WTR}$ | $t_{CK}$ |
| | WRITE or WRITE w/AP | (BL/2) | $t_{CK}$ |
| | PRECHARGE or ACTIVE | 1 | $t_{CK}$ |

## DC OPERATING CONDITIONS

All voltages referenced to $V_{SS}$

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 1 .7 | 1 .8 | 1 .9 | V | 1 |
| I/O Supply voltage | $V_{CCQ}$ | 1 .7 | 1 .8 | 1 .9 | V | 4 |
| I/O Reference voltage | $V_{REF}$ | 0.49 x $V_{CCQ}$ | 0.50 x $V_{CCQ}$ | 0.51 x $V_{CCQ}$ | V | 2 |
| I/O Termination voltage | $V_{TT}$ | $V_{REF}$-0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V | 3 |

Notes:

1. $V_{CC}$ $V_{CCQ}$ must track each other. $V_{CCQ}$ must be less than or equal to $V_{CC}$.
2. $V_{REF}$ is expected to equal $V_{CCQ}$/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on $V_{REF}$ may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on $V_{REF}$ may not exceed ±2 percent of $V_{REF}$. This measurement is to be taken at the nearest $V_{REF}$ bypass capacitor.
3. $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$ and must track variations in the DC level of $V_{REF}$.
4. $V_{CCQ}$ tracks with $V_{CC}$ track with $V_{CC}$.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | MIN | MAX | U nit |
|---|---|---|---|---|---|
| $V_{CC}$ | Voltage on $V_{CC}$ pin relative to $V_{SS}$ | | -1.0 | 2.3 | V |
| $V_{CCQ}$ | Voltage on $V_{CCQ}$ pin relative to $V_{SS}$ | | -0.5 | 2.3 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | | -0.5 | 2.3 | V |
| $T_{STG}$ | Storage temperature | | -55 | 125 | °C |
| $I_L$ | Input leakage current; Any input 0V<$V_{IN}$<$V_{CC}$; $V_{REF}$ input 0V<$V_{IN}$<0.95V; Other pins not under test = 0V | Command/Address, RAS#, CAS#, WE#, CS#, CKE | -25 | 25 | µA |
| | | CK, CK# | -5 | 5 | µA |
| | | DM | -5 | 5 | µA |
| $I_{OZ}$ | Output leakage current; 0V<$V_{OUT}$<$V_{CCQ}$; DQs and ODT are disable | DQ, DQS, DQS# | -5 | 5 | µA |
| $I_{VREF}$ | $V_{REF}$ leakage current; $V_{REF}$ = Valid $V_{REF}$ level | | -18 | 18 | µA |

## INPUT/OUTPUT CAPACITANCE

25°C, f = 1MHz, $V_{CC}$ = $V_{CCQ}$ = 1.8V

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Input capacitance (A0 - A12, BA0 - BA1 ,CS#, RAS#,CAS#,WE#, CKE, ODT) | $C_{IN1}$ | 22 | pF |
| Input capacitance CK, CK# | $C_{IN2}$ | 9 | pF |
| Input capacitance DM, DQS, DQS# | $C_{IN3}$ | 9 | pF |
| Input capacitance DQ0 - 71 | $C_{OUT}$ | 10 | pF |

## INPUT DC LOGIC LEVEL

All voltages referenced to $V_{SS}$

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH}(DC)$ | $V_{REF} + 0.125$ | $V_{CCQ} + 0.300$ | V |
| Input Low (Logic 0) Voltage | $V_{IL}(DC)$ | -0.300 | $V_{REF} - 0.125$ | V |

## INPUT AC LOGIC LEVEL

All voltages referenced to $V_{SS}$

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533 | $V_{IH}(AC)$ | $V_{REF} + 0.250$ | — | V |
| AC Input High (Logic 1) Voltage DDR2-667 | $V_{IH}(AC)$ | $V_{REF} + 0.200$ | — | V |
| AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533 | $V_{IL}(AC)$ | — | $V_{REF} - 0.250$ | V |
| AC Input Low (Logic 0) Voltage DDR2-667 | $V_{IL}(AC)$ | — | $V_{REF} - 0.200$ | V |

## ODT DC ELECTRICAL CHARACTERISTICS

All voltages referenced to $V_{SS}$

| Parameter | Symbol | Min | Nom | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{TT}$ effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1 | $R_{TT}1_{(EFF)}$ | 52 | 75 | 97 | Ω | 1 |
| $R_{TT}$ effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0 | $R_{TT}2_{(EFF)}$ | 105 | 150 | 195 | Ω | 1 |
| $R_{TT}$ effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1 | $R_{TT}3_{(EFF)}$ | 35 | 50 | 65 | Ω | 1 |
| Deviation of VM with respect to $V_{CCQ/2}$ | $\Delta VM$ | -6 | | 6 | % | 2 |

Note: 1. $R_{TT}1_{(EFF)}$ and $R_{TT}2_{(EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the ball being tested, and then measuring current, $I(V_{IH(AC)})$, and $I(V_{IL(AC)})$, respectively.

$$RTT(EFF) = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Measure voltage (VM) at tested ball with no load

$$\Delta VM = \left( \frac{2 \times VM}{V_{CCQ}} - 1 \right) \times 100$$

## BGA THERMAL RESISTANCE (BB MARKING CODE)

| Description | Symbol | Typical | Units | Notes |
|---|---|---|---|---|
| Junction to Board | Theta Jb | 4.7 | °C/W | 1 |
| Junction to Case (Top) | Theta Jc | 5.0 | °C/W | 1 |

The JEDEC JESD51 specifications are used as the default modeling environment and boundary conditions. Using still air, horizontal mounting and the 2s2p board. Published material properties are used as input to derive the thermal characteristics of the module. Your application conditions will most likely differ from the JESD51 2s2p board definition specifications; therefore, Microsemi PMG recommends a customized evaluation of thermal resistances based on the actual conditions in thermally-challenged situations. Delphi models are available for most products upon request.

## DDR2 $I_{CC}$ SPECIFICATIONS AND CONDITIONS

| Symbol | Proposed Conditions | | 667 CL5 | 533 CL4 | 400 CL3 | Units |
|---|---|---|---|---|---|---|
| $I_{CC0}$ | Operating one bank active-precharge current;<br>$t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RC}$ = $t_{RC}(I_{CC})$, $t_{RAS}$ = $t_{RAS}min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | 600 | 550 | 550 | mA |
| $I_{CC1}$ | Operating one bank active-read-precharge current;<br>$I_{OUT}$ = 0mA; BL = 4, CL = $CL(I_{CC})$, AL = 0; $t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RC}$ = $t_{RC}$ $(I_{CC})$, $t_{RAS}$ = $t_{RAS}min(I_{CC})$, $t_{RCD}$ = $t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as $I_{DAD6W}$ | | 750 | 675 | 650 | mA |
| $I_{CC2P}$ | Precharge power-down current;<br>All banks idle; $t_{CK}$ = $t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | 35 | 35 | 35 | mA |
| $I_{CC2Q}$ | Precharge quiet standby current;<br>All banks idle; $t_{CK}$ = $t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | 275 | 225 | 200 | mA |
| $I_{CC2N}$ | Precharge standby current;<br>All banks idle; $t_{CK}$ = $t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | 300 | 250 | 225 | mA |
| $I_{CC3P}$ | Active power-down current;<br>All banks open; $t_{CK}$ = $t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0 | 200 | 175 | 150 | mA |
| | | Slow PDN Exit MRS(12) = 1 | 60 | 60 | 60 | mA |
| $I_{CC3N}$ | Active standby current;<br>All banks open; $t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RAS}$ = $t_{RAS}MAX(I_{CC})$, $t_{RP}$ = $t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | 350 | 300 | 250 | mA |
| $I_{CC4W}$ | Operating burst write current;<br>All banks open, Continuous burst writes; BL = 4, CL = $CL(I_{CC})$, AL = 0; $t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RAS}$ = $t_{RAS}MAX(I_{CC})$, $t_{RP}$ = $t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | 1,250 | 1,025 | 800 | mA |
| $I_{CC4R}$ | Operating burst read current;<br>All banks open, Continuous burst reads, $I_{OUT}$ = 0mA; BL = 4, CL = $CL(I_{CC})$, AL = 0; $t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RAS}$ = $t_{RAS}MAX(I_{CC})$, $t_{RP}$ = $t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as $I_{DAD6W}$ | | 1,175 | 975 | 775 | mA |
| $I_{CC5}$ | Burst auto refresh current;<br>$t_{CK}$ = $t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | 1,100 | 1,050 | 1,000 | mA |
| $I_{CC6}$ | Self refresh current;<br>CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | 35 | 35 | 35 | mA |
| $I_{CC7}$ | Operating bank interleave read current;<br>All bank interleaving reads, $I_{OUT}$ = 0mA; BL = 4, CL = $CL(I_{CC})$, AL = $t_{RCD}(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK}$ = $t_{CK}(I_{CC})$, $t_{RC}$ = $t_{RC}(I_{CC})$, $t_{RRD}$ = $t_{RRD}(I_{CC})$, $t_{RCD}$ = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as $I_{DAD6R}$; Refer to the following page for detailed timing conditions | | 1,700 | 1,700 | 1,700 | mA |

## AC TIMING PARAMETERS

| Parameter | | | Symbol | 667Mbs CL5 | | 533Mbs CL4 | | 400Mbs CL3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| Clock | Clock cycle time | CL=5 | $t_{CK}(5)$ | 3,000 | 8,000 | | | | | ps |
| | | CL=4 | $t_{CK}(4)$ | 3,750 | 8,000 | 3,750 | 8,000 | 5,000 | 8,000 | ps |
| | | CL=3 | $t_{CK}(3)$ | 5,000 | 8,000 | 5,000 | 8,000 | 5,000 | 8,000 | ps |
| | CK high-level width | | $t_{CH}$ | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK}$ |
| | CK low-level width | | $t_{CL}$ | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK}$ |
| | Half clock period | | $t_{HP}$ | MIN ($t_{CH}$, $t_{CL}$) | | MIN ($t_{CH}$, $t_{CL}$) | | MIN ($t_{CH}$, $t_{CL}$) | | ps |
| Data | DQ output access time from CK/CK# | | $t_{AC}$ | -550 | +650 | -550 | +650 | -600 | +600 | ps |
| | Data-out high impedance window from CK/CK# | | $t_{HZ}$ | | $t_{AC(MAX)}$ | | $t_{AC(MAX)}$ | | $t_{AC(MAX)}$ | ps |
| | Data-out low-impedance window from CK/CK# | | $t_{LZ}$ | $t_{AC(MN)}$ | $t_{AC(MAX)}$ | $t_{AC(MN)}$ | $t_{AC(MAX)}$ | $t_{AC(MN)}$ | $t_{AC(MAX)}$ | ps |
| | DQ and DM input setup time relative to DQS | | $t_{DS}$ | 400 | | 400 | | 450 | | ps |
| | DQ and DM input hold time relative to DQS | | $t_{DH}$ | 500 | | 500 | | 450 | | ps |
| | DQ and DM input pulse width (for each input) | | $t_{DIPW}$ | 0.35 | | 0.35 | | 0.35 | | $t_{CK}$ |
| | Data hold skew factor | | $t_{QHS}$ | | 400 | | 400 | | 450 | ps |
| | DQ-DQS hold, DQS to first DQ to go nonvalid, per access | | $t_{QH}$ | $t_{HP}$ - $t_{QHS}$ | | $t_{HP}$ - $t_{QHS}$ | | $t_{HP}$ - $t_{QHS}$ | | ps |
| | Data valid output window (DVW) | | $t_{DVW}$ | $t_{QH}$ - $t_{DQSQ}$ | | $t_{QH}$ - $t_{DQSQ}$ | | $t_{QH}$ - $t_{DQSQ}$ | | ns |
| Data Strobe | DQS input high pulse width | | $t_{DQSH}$ | 0.35 | | 0.35 | | 0.35 | | $t_{CK}$ |
| | DQS input low pulse width | | $t_{DQSL}$ | 0.35 | | 0.35 | | 0.35 | | $t_{CK}$ |
| | DQS output access time fromCK/CK# | | $t_{DQSCK}$ | -550 | +650 | -550 | +650 | -600 | +600 | Ps |
| | DQS falling edge to CK rising - setup time | | $t_{DSS}$ | 0.2 | | 0.2 | | 0.2 | | $t_{CK}$ |
| | DQS falling edge from CK rising - hold time | | $t_{DSH}$ | 0.2 | | 0.2 | | 0.2 | | $t_{CK}$ |
| | O DQS-DQ skew, DOS to last DQ valid, per group, per access | | $t_{DQSQ}$ | 300 | | | 300 | | 350 | ps |
| | DQS read preamble | | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ |
| | DQS read postamble | | $t_{RPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ |
| | DQS write preamble setup time | | $t_{WPRES}$ | 0 | | 0 | | 0 | | ps |
| | DQS write preamble | | $t_{WPRE}$ | 0.25 | | 0.25 | | 0.25 | | $t_{CK}$ |
| | DQS write postamble | | $t_{WPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ |
| | Write command to first DQS latching transition | | | WL-$T_{DQSS}$ | WL+$T_{DQSS}$ | WL-$T_{DQSS}$ | WL+$T_{DQSS}$ | WL-$T_{DQSS}$ | WL+$T_{DQSS}$ | $t_{CK}$ |
| | Positive DQs latch edge to associated edge | | $t_{DQSS}$ | -0.18 | +0.18 | -0.25 | +0.25 | -0.25 | +0.25 | $t_{CK}$ |

## AC TIMING PARAMETERS (continued)

| Parameter | | Symbol | 667Mbs CL5 | | 533Mbs CL4 | | 400Mbs CL3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Command and Address | Address and control input pulse width for each input | $t_{IPW}$ | 0.6 | | 0.6 | | 0.6 | | $t_{CK}$ |
| | Address and control input setup time | $t_{ISa}$ | 400 | | 500 | | 600 | | ps |
| | | $t_{ISb}$ | 200 | | 250 | | 350 | | ps |
| | Address and control input hold time | $t_{IHa}$ | 400 | | 500 | | 600 | | ps |
| | | $t_{IHb}$ | 275 | | 375 | | 475 | | ps |
| | CAS# to CAS# command delay | $t_{CCD}$ | 2 | | 2 | | 2 | | $t_{CK}$ |
| | ACTIVE to ACTIVE (same bank) command | $t_{RC}$ | 55 | | 55 | | 55 | | ns |
| | ACTIVE bank a to ACTIVE bank b command | $t_{RRD}$ | 10 | | 10 | | 10 | | ns |
| | ACTIVE to READ or WRITE delay | $t_{RCD}$ | 15 | | 15 | | 15 | | ns |
| | Four Bank Activate period | $t_{FAW}$ | 50 | | 50 | | 50 | | ns |
| | ACTIVE to PRECHARGE command | $t_{RAS}$ | 40 | 70,000 | 40 | 70,000 | 40 | 70,000 | ns |
| | Internal READ to precharge command delay | $t_{RTP}$ | 7.5 | | 7.5 | | 7.5 | | ns |
| | Write recovery time | $t_{WR}$ | 15 | | 15 | | 15 | | ns |
| | Auto precharge write recovery + precharge time | $t_{DAL}$ | $t_{WR} + t_{RP}$ | | $t_{WR} + t_{RP}$ | | $t_{WR} + t_{RP}$ | | ns |
| | Internal WRITE to READ command delay | $t_{WTR}$ | 7.5 | | 7.5 | | 10 | | ns |
| | PRECHARGE command period | $t_{RP}$ | 15 | | 15 | | 15 | | ns |
| | PRECHARGE ALL command period | $t_{RPA}$ | $t_{RP} + t_{CK}$ | | $t_{RP} + t_{CK}$ | | $t_{RP} + t_{CK}$ | | ns |
| | LOAD MODE command cycle time | $t_{MRD}$ | 2 | | 2 | | 2 | | $t_{CK}$ |
| | CKE low to CK, CK# uncertainty | $t_{DELAY}$ | $t_{IS} + t_{IH} + t_{CK}$ | | $t_{IS} + t_{IH} + t_{CK}$ | | $t_{IS} + t_{IH} + t_{CK}$ | | ns |
| Refresh | REFRESH to Active or Refresh to Refresh command interval | $t_{RFC}$ | 105 | 70,000 | 105 | 70,000 | 105 | 70,000 | ns |
| | Average periodic refresh interval (Comm + Ind Temp) | $t_{REFI}$ | | 7.8 | | 7.8 | | 7.8 | µs |
| | Average periodic refresh interval (Military Temp) | $t_{REFI}$ | | 1.9 | | 1.9 | | 1.9 | µs |
| Self Refresh | Exit self refresh to non-READ command | $t_{XSNR}$ | $t_{RFC(MIN)} + 10$ | | $t_{RFC(MIN)} + 10$ | | $t_{RFC(MIN)} + 10$ | | ns |
| | Exit self refresh to READ | $t_{XSRD}$ | 200 | | 200 | | 200 | | $t_{CK}$ |
| | Exit self refresh timing reference | $t_{ISXR}$ | $t_{IS}$ | | $t_{IS}$ | | $t_{IS}$ | | ps |

## AC TIMING PARAMETERS (continued)

| Parameter | | Symbol | 667Mbs CL5 | | 533Mbs CL4 | | 400Mbs CL3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| ODT | ODT turn-on delay | $t_{AOND}$ | 2 | 2 | 2 | 2 | 2 | 2 | $t_{CK}$ |
| | ODT turn-on | $t_{AON}$ | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 1000 | ps |
| | ODT turn-off delay | $t_{AOFD}$ | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | $t_{CK}$ |
| | ODT turn-off | $t_{AOF}$ | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 600 | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 600 | $t_{AC(MIN)}$ | $t_{AC(MAX)}$ + 600 | ps |
| | ODT turn-on (power-down mode) | $t_{AONPD}$ | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | ps |
| | ODT turn-off (power-down mode) | $t_{AOFPD}$ | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | $t_{AC(MIN)}$ + 2000 | $2 \times t_{CK}$ + $t_{AC(MAX)}$ + 1000 | ps |
| | ODT to power-down entry latency | $t_{ANPD}$ | 3 | | 3 | | 3 | | $t_{CK}$ |
| | ODT power-down exit latency | $t_{AXPD}$ | 8 | | 8 | | 8 | | $t_{CK}$ |
| Power-Down | Exit active power-down to READ command, MR[bit12=0] | $t_{XARD}$ | 2 | | 2 | | 2 | | $t_{CK}$ |
| | Exit active power-down to READ command, MR[bit12=1] | $t_{XARDS}$ | 7-AL | | 6-AL | | 6-AL | | $t_{CK}$ |
| | Exit precharge power-down to any non-READ command | $t_{XP}$ | 2 | | 2 | | 2 | | $t_{CK}$ |
| | CKE minimum high/low time | $t_{CKE}$ | 3 | | 3 | | 3 | | $t_{CK}$ |

## PACKAGE DIMENSION: 208 PLASTIC BALL GRID ARRAY (PBGA)

**BOTTOM VIEW**



208 x Ø 0.60 (0.024) NOM

20.10 (0.791) MAX

18.0 (0.709) NOM

1.0 (0.039) NOM

1.0 (0.039) NOM

10.0 (0.394) NOM

16.10 (0.634) MAX
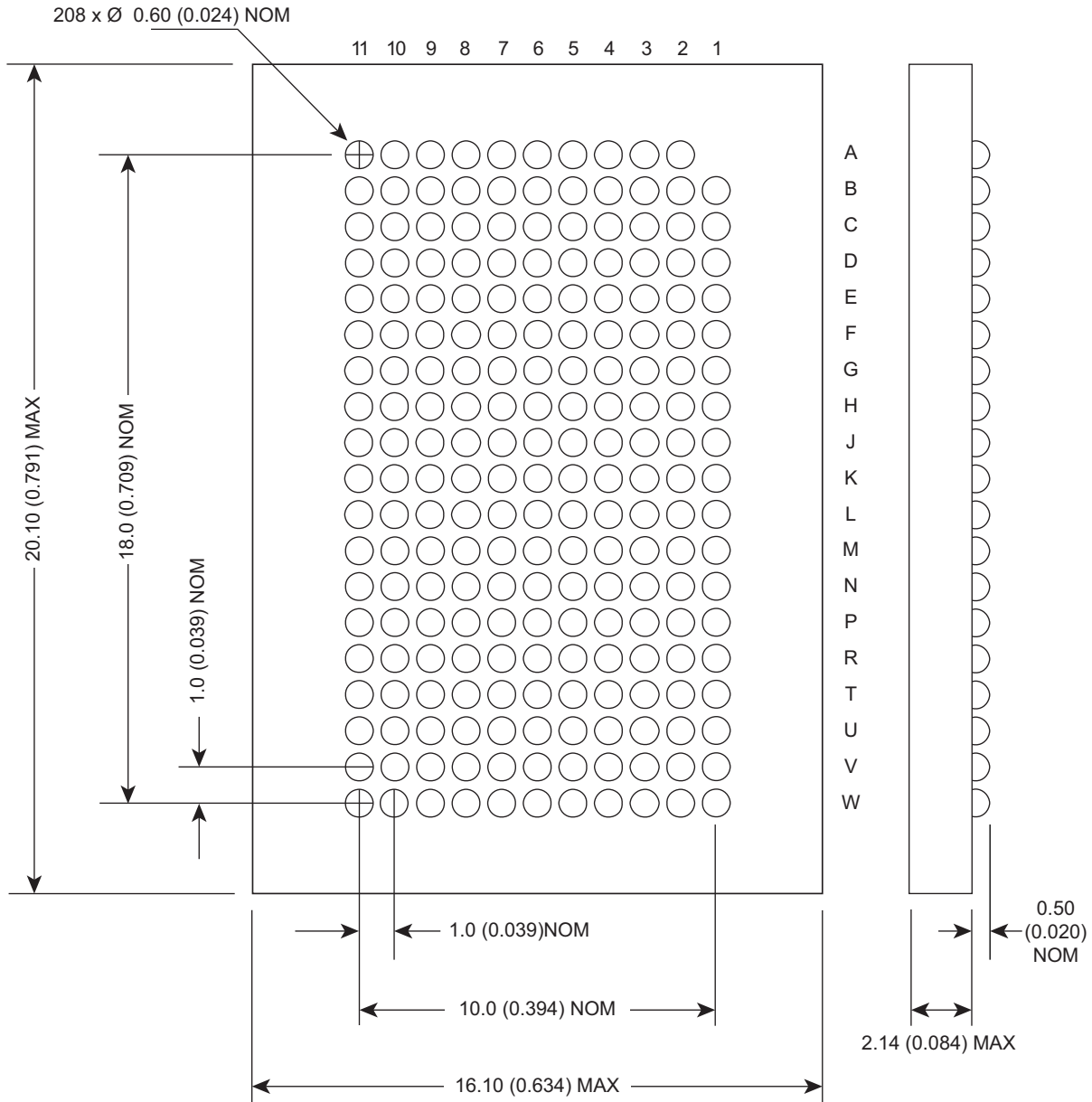
0.50 (0.020) NOM

3.08 (0.121) MAX
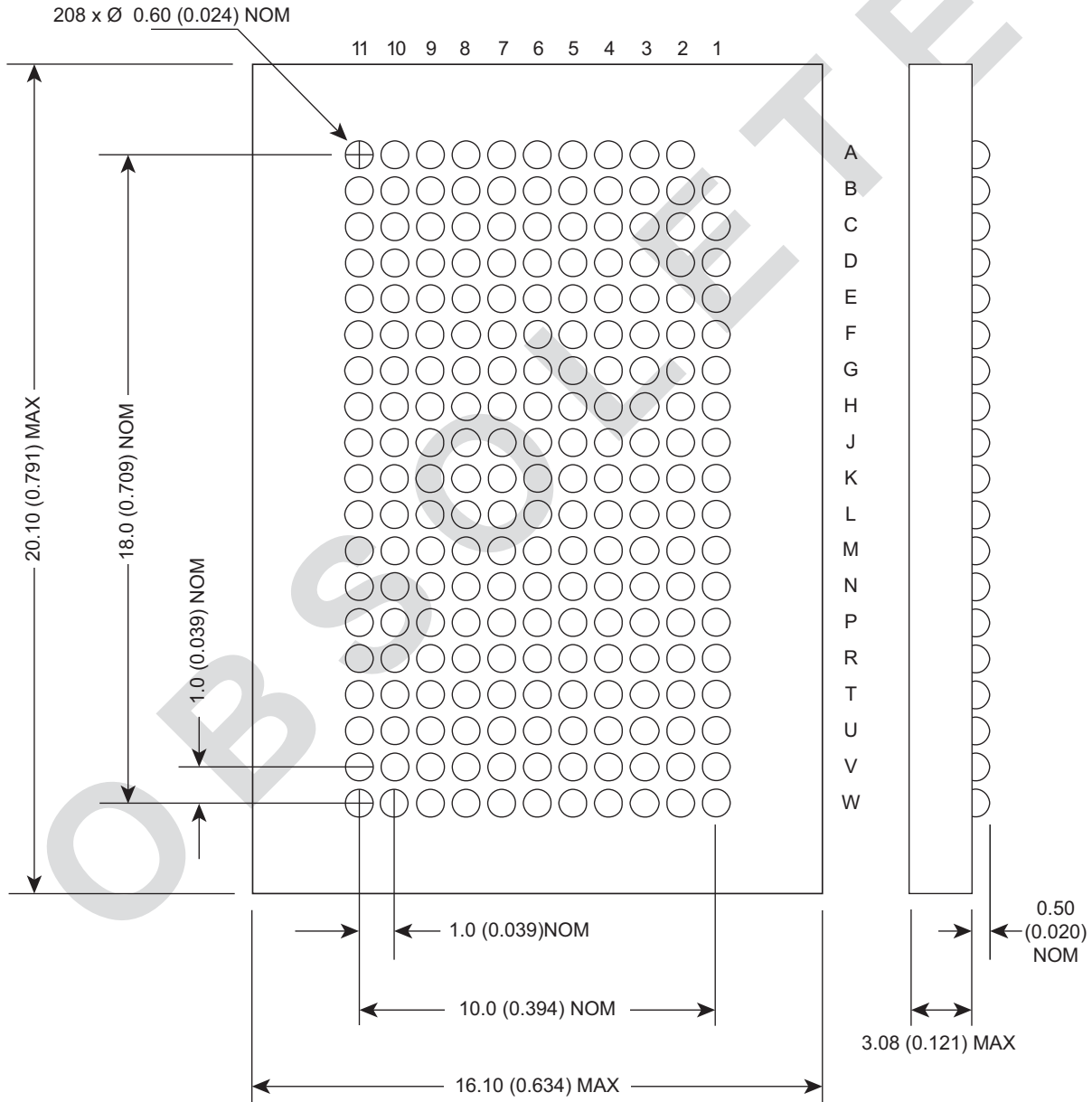
- Pads are solder mask defined, pad opening = 0.48mm
- "AA" used or internal reference

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES
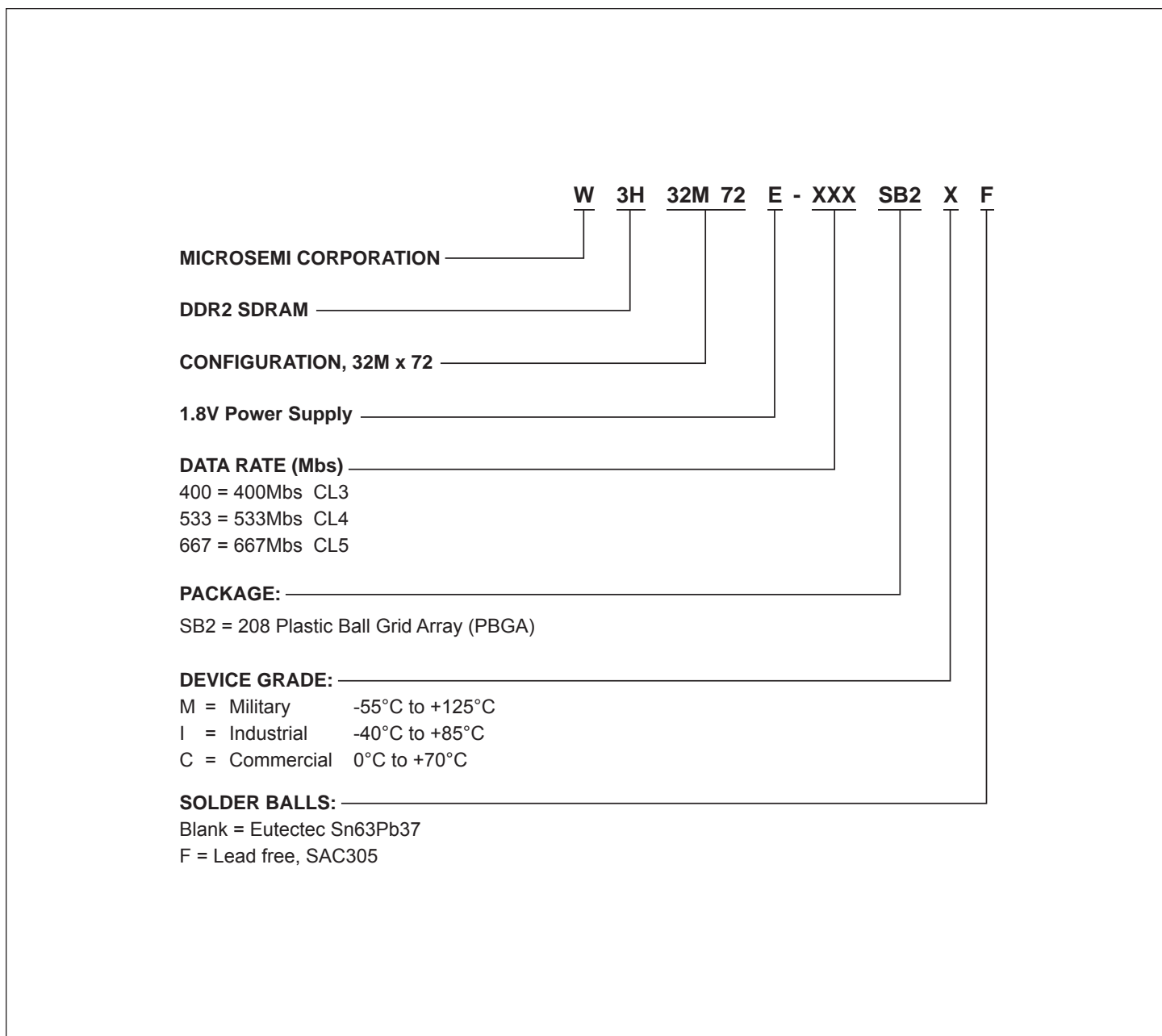
## PACKAGE DIMENSION: 208 PLASTIC BALL GRID ARRAY (PBGA)

**BOTTOM VIEW**

208 x Ø 0.60 (0.024) NOM



- Pads are solder mask defined, pad opening = 0.48mm
- Marking Code = BB

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## ORDERING INFORMATION

W   3H   32M 72   E - XXX   SB2   X   F

**MICROSEMI CORPORATION**

**DDR2 SDRAM**

**CONFIGURATION, 32M x 72**

**1.8V Power Supply**

**DATA RATE (Mbs)**
400 = 400Mbs  CL3
533 = 533Mbs  CL4
667 = 667Mbs  CL5

**PACKAGE:**
SB2 = 208 Plastic Ball Grid Array (PBGA)

**DEVICE GRADE:**
M = Military        -55°C to +125°C
I  = Industrial     -40°C to +85°C
C = Commercial   0°C to +70°C

**SOLDER BALLS:**
Blank = Eutectec Sn63Pb37
F = Lead free, SAC305

## Document Title

256MB – 32M x 72 DDR2 SDRAM 208 PBGA Multi-Chip Package

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Initial Release | November 2009 | Preliminary |
| Rev 1 | Change (Pg. 23)<br>1.1 Set BGA Thermal Resistance to TBD | November 2009 | Preliminary |
| Rev 2 | Change (Pg. 28)<br>2.1 Update MO drawing thickness to 3.08 (0.121) max, length to 20.10 (0.791) max and width to 16.10 (0.634) max<br>2.2 Remove note from BGA thermal resistance | March 2010 | Preliminary |
| Rev 3 | Change (Pg. 17, 18)<br>3.1 Updated capacitance measurements in input/output capacitance table<br>3.2 Updated BGA thermal resistance table | November 2010 | Final |
| Rev 4 | Change (Pg 18)<br>4.1 Remove note 1 from BGA thremal resistance | December 2010 | Final |
| Rev 5 | Changes (Pg. 1, 30)<br>5.1 Ad Pb free part option, W3H64M72E-XSBXF - "F" denotes the part is lead free<br>5.2 Under Ordering Information added SOLDER BALLS - Blank = Eutectic SN63Pb37 and F = Lead free, SAC305 | February 2011 | Final |
| Rev 6 | Changes (Pg.1, 25)<br>6.1 Add "256MB" to doc title<br>6.2 Add "Typical Applications" diagram | August 2011 | Final |
| Rev 7 | Changes (Pg. 11, 16, 17, 19-23)<br>7.1 Spell out "temperature" in E7-1 discription<br>7.2 Delete note under Self Refresh Command paragraphs<br>7.3 Delete T$_{CASE}$ from Absolute Maximum Ratings chart<br>7.4 Delete "T$_A$ =" from subtitle of Input/Output Capacitance chart<br>7.5 Delete subtitle from DDR2 L$_{CC}$ Specifications and Conditions chart<br>7.6 Delete subtitle from AC Timing Parameters charts<br>7.7 Change maximum thickness value of Package Dimension diagram | December 2012 | Final |
| Rev 8 | Change (Pg 18)<br>8.1 Added Theta Jb and Theta Jc | October 2013 | Final |
| Rev 9 | Change (Pg 2)<br>9.1 Renumbered die on functional block diagram from U0 - U4 to U1 - U5.<br>9.2 Corrected DQ8 on die U5 to DQ7 on the functional block diagram. | December 2013 | Final |